AMD Xilinx - XC2VP70-6FF1517C Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8272
Number of Logic Elements/Cells	74448
Total RAM Bits	6045696
Number of I/O	964
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp70-6ff1517c

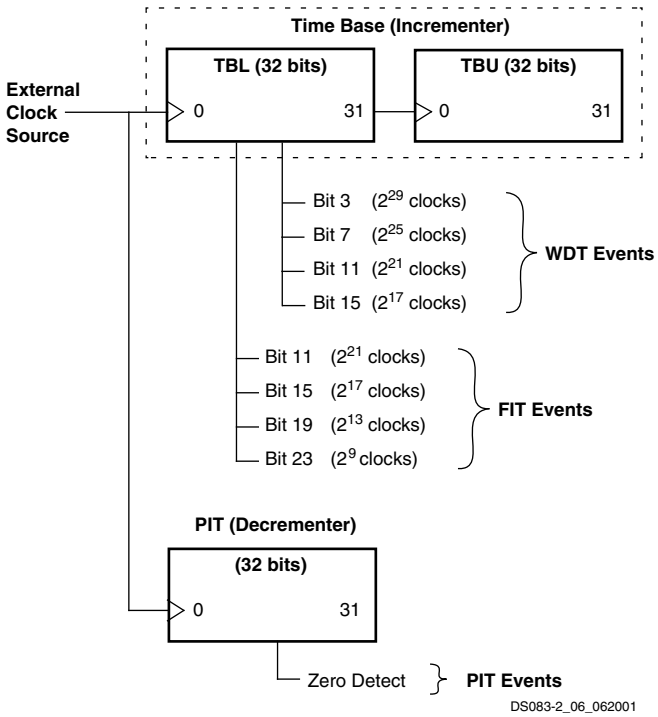


Figure 17: **Relationship of Timer Facilities to Base Clock**

Interrupts

The PPC405 provides an interface to an interrupt controller that is logically outside the PPC405 core. This controller combines the asynchronous interrupt inputs and presents them to the embedded core as a single interrupt signal. The sources of asynchronous interrupts are external signals, the JTAG/debug unit, and any implemented peripherals.

Debug Logic

All architected resources on the embedded PPC405 core can be accessed through the debug logic. Upon a debug event, the PPC405 core provides debug information to an external debug tool. Three different types of tools are supported depending on the debug mode: ROM monitors, JTAG debuggers, and instruction trace tools.

In internal debug mode, a debug event enables exception-handling software at a dedicated interrupt vector to take over the CPU core and communicate with a debug tool. The debug tool has read-write access to all registers and can set hardware or software breakpoints. ROM monitors typically use the internal debug mode.

In external debug mode, the CPU core enters stop state (stops instruction execution) when a debug event occurs. This mode offers a debug tool read-write access to all registers in the PPC405 core. Once the CPU core is in stop state, the debug tool can start the CPU core, step an instruction, freeze the timers, or set hardware or software break points. In addition to CPU core control, the debug logic is capable of writing instructions into the instruction cache, eliminating the need for external memory during initial board bring-up. Communication to a debug tool using external debug mode is through the JTAG port.

Debug wait mode offers the same functionality as external debug mode with one exception. In debug wait mode, the CPU core goes into wait state instead of stop state after a debug event. Wait state is identical to stop state until an interrupt occurs. In wait state, the PPC405 core can vector to an exception handler, service an interrupt and return to wait state. This mode is particularly useful when debugging real time control systems.

Real-time trace debug mode is always enabled. The debug logic continuously broadcasts instruction trace information to the trace port. When a debug event occurs, the debug logic signals an external debug tool to save instruction trace information before and after the event. The number of instructions traced depends on the trace tool.

Debug events signal the debug logic to stop the CPU core, put the CPU core in debug wait state, cause a debug exception or save instruction trace information.

Big Endian and Little Endian Support

The embedded PPC405 core supports big endian or little endian byte ordering for instructions stored in external memory. Since the PowerPC architecture is big endian internally, the ICU rearranges the instructions stored as little endian into the big endian format. Therefore, the instruction cache always contains instructions in big endian format so that the byte ordering is correct for the execution unit. This feature allows the 405 core to be used in systems designed to function in a little endian environment.

Date	Version	Revision
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s.
03/05/07	4.6	*No changes in Module 2 for this revision.*
11/05/07	4.7	• Updated copyright notice and legal disclaimer. • Debug Interface, page 19, and Boundary-Scan (JTAG, IEEE 1532) Mode, page 57: Updated IEEE 1149.1 compliance statement.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner.

Notice of Disclaimer

Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)

Table 36: **IOB Input Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
HSLVDCI, 1.8V	HSLVDCI_18	$T_{IHSLVDCI\_18}$	0.59	0.68	0.75	ns
HSLVDCI, 2.5V	HSLVDCI_25	$T_{IHSLVDCI\_25}$	0.59	0.68	0.75	ns
HSLVDCI, 3.3V	HSLVDCI_33	$T_{IHSLVDCI\_33}$	0.59	0.68	0.75	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T_{IGTL_DCI}	0.49	0.57	0.62	ns
GTL Plus with DCI	GTLP_DCI	T_{IGTLP_DCI}	0.27	0.31	0.35	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	$T_{IHSTL\_I\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class II, with DCI	HSTL_II_DCI	$T_{IHSTL\_II\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class III, with DCI	HSTL_III_DCI	$T_{IHSTL\_III\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	$T_{IHSTL\_IV\_DCI}$	0.27	0.31	0.35	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	$T_{IHSTL\_I\_DCI\_18}$	0.27	0.31	0.35	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	$T_{IHSTL\_II\_DCI\_18}$	0.27	0.31	0.35	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	$T_{IHSTL\_III\_DCI\_18}$	0.27	0.31	0.35	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	$T_{IHSTL\_IV\_DCI\_18}$	0.27	0.31	0.35	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	$T_{ISSTL18\_I\_DCI}$	0.62	0.72	0.79	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	$T_{ISSTL18\_II\_DCI}$	0.64	0.73	0.81	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	$T_{ISSTL2\_I\_DCI}$	0.17	0.20	0.22	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	$T_{ISSTL2\_II\_DCI}$	0.17	0.20	0.22	ns
LVDS, 2.5V, with DCI	LVDS_25_DCI	$T_{ILVDS\_25\_DCI}$	0.31	0.36	0.40	ns
LVDSEXT, 2.5V, with DCI	LVDSEXT_25_DCI	$T_{ILVDSEXT\_25\_DCI}$	0.33	0.37	0.41	ns
LVDS, 2.5V, with Differential Termination (DT)	LVDS_25_DT	$T_{ILVDS\_25\_DT}$	0.31	0.36	0.40	ns
LVDSEXT, 2.5V, with DT	LVDSEXT_25_DT	$T_{ILVDSEXT\_25\_DT}$	0.33	0.37	0.41	ns
ULVDS, 2.5V, with DT	ULVDS_25_DT	$T_{IULVDS\_25\_DT}$	0.31	0.36	0.40	ns
LDT, 2.5V, with DT	LDT_25_DT	$T_{ILDT\_25\_DT}$	0.31	0.36	0.40	ns

CLB Distributed RAM Switching Characteristics

Table 43: **CLB Distributed RAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Sequential Delays					
Clock CLK to X/Y outputs (WE active) in 16 x 1 mode	$T_{SHCKO16}$	1.25	1.38	1.54	ns, max
Clock CLK to X/Y outputs (WE active) in 32 x 1 mode	$T_{SHCKO32}$	1.57	1.75	1.95	ns, max
Clock CLK to F5 output	$T_{SHCKOF5}$	1.52	1.68	1.88	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.38/–0.07	0.41/–0.07	0.46/–0.08	ns, min
F/G address inputs	T_{AS}/T_{AH}	0.42/ 0.00	0.47/ 0.00	0.52/ 0.00	ns, min
SR input	T_{WES}/T_{WEH}	0.22/ 0.04	0.24/ 0.05	0.26/ 0.05	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}	0.63	0.72	0.79	ns, min
Minimum Pulse Width, Low	T_{WPL}	0.63	0.72	0.79	ns, min
Minimum clock period to meet address write cycle time	T_{WC}	1.25	1.44	1.58	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Shift Register Switching Characteristics

Table 44: **CLB Shift Register Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Sequential Delays					
Clock CLK to X/Y outputs	T_{REG}	2.78	3.12	3.49	ns, max
Clock CLK to X/Y outputs	T_{REG32}	3.10	3.49	3.90	ns, max
Clock CLK to XB output via MC15 LUT output	T_{REGXB}	2.84	3.18	3.55	ns, max
Clock CLK to YB output via MC15 LUT output	T_{REGYB}	2.55	2.88	3.21	ns, max
Clock CLK to Shiftout	T_{CKSH}	2.50	2.83	3.15	ns, max
Clock CLK to F5 output	T_{REGF5}	3.05	3.42	3.83	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{SRLDS}/T_{SRLDH}	0.70/–0.16	0.77/–0.18	0.98/–0.21	ns, min
SR input	T_{WSS}/T_{WSH}	0.27/ 0.01	0.34/ 0.01	0.47/ 0.01	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{SRPH}	0.63	0.72	0.79	ns, min
Minimum Pulse Width, Low	T_{SRPL}	0.63	0.72	0.79	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Virtex-II Pro Receiver Data-Valid Window (R_X)

R_X is the required minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$R_X = [TSAMP^{(1)} + TCKSKEW^{(2)} + TPKGSKEW^{(3)}]$$

Notes:

1. This parameter indicates the total sampling error of Virtex-II Pro DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter in a quiet system
   - Worst-case duty-cycle distortion
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
3. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/17/02	2.0	• Added new Virtex-II Pro family members. • Added timing parameters from speedsfile **v1.62**. • Added Table 46, Pipelined Multiplier Switching Characteristics. • Added 3.3V-vs-2.5V table entries for some parameters.
09/03/02	2.1	• Added Source-Synchronous Switching Characteristics section. • Added absolute max ratings for 3.3V-vs-2.5V parameters in Table 1. • Added recommended operating conditions for V_{IN} and RocketIO footnote to Table 2. • Updated SSTL2 values in Table 6. Added SSTL18 values: Table 6, Table 39, Table 32. [Table 32 removed in v2.8.] • Added Table 10, which contains LVPECL DC specifications.
09/27/02	2.2	Added section General Power Supply Requirements.
11/20/02	2.3	Updated parametric information in: • Table 1: Increase Absolute Max Rating for V_{CCO}, V_{REF}, V_{IN}, and V_{TS} from 3.6V to 3.75V. Delete cautionary footnotes related to voltage overshoot/undershoot. • Table 2: Delete V_{CCO} specifications for 2.5V and below operation. Delete footnote referencing special information for 3.3V operation. Add footnote for PCI/PCI-X. • Table 3: Add I_{BATT}. Delete I_L specifications for 2.5V and below operation. • Table 4: Add Typical Quiescent Supply Currents for XC2VP4 and XC2VP7 only • Table 6: Correct I_{OL} and I_{OH} for SSTL2 I. Add rows for LVTTL, LVCMOS33, and PCI-X. Correct max V_{IH} from V_{CCO} to 3.6V. • Table 7: Correct Min/Max V_{OD}, V_{OCM}, and V_{ICM} • Table 10: Reformat LVPECL DC Specifications to match Virtex-II data sheet format • Table 12: Correct parameter name from Differential Output Voltage to Single-Ended Output Voltage Swing. • Table 16: Add CPMC405CLOCK max frequencies • Table 27: Add footnote regarding serial data rate limitation in -5 part. • Table 39: Add rows for LVTTL, LVCMOS33, and PCI-X. • Table 32: Add LVTTL, LVCMOS33, and PCI-X. Correct all capacitive load values (except PCI/PCI-X) to 0 pF. [Table 32 removed in v2.8.] • Table 51: Correct CCLK max frequencies
11/25/02	2.4	Table 1: Correct lower limit of voltage range of V_{IN} and V_{TS} from –0.3V to –0.5V for 3.3V.

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
3	IO_L05P_3	L13
3	IO_L03N_3/VREF_3	L12
3	IO_L03P_3	M13
3	IO_L02N_3	M16
3	IO_L02P_3	N16
3	IO_L01N_3/VRP_3	M15
3	IO_L01P_3/VRN_3	M14
4	IO_L01N_4/BUSY/DOUT(1)	P15
4	IO_L01P_4/INIT_B	P14
4	IO_L02N_4/D0/DIN(1)	R14
4	IO_L02P_4/D1	P13
4	IO_L03N_4/D2	T15
4	IO_L03P_4/D3	T14
4	IO_L06N_4/VRP_4	N12
4	IO_L06P_4/VRN_4	P12
4	IO_L07P_4/VREF_4	N11
4	IO_L09N_4	M11
4	IO_L09P_4/VREF_4	M10
4	IO_L69N_4	N10
4	IO_L69P_4/VREF_4	P10
4	IO_L74N_4/GCLK3S	N9
4	IO_L74P_4/GCLK2P	P9
4	IO_L75N_4/GCLK1S	R9
4	IO_L75P_4/GCLK0P	T9
5	IO_L75N_5/GCLK7S	T8
5	IO_L75P_5/GCLK6P	R8
5	IO_L74N_5/GCLK5S	P8
5	IO_L74P_5/GCLK4P	N8
5	IO_L69N_5/VREF_5	P7
5	IO_L69P_5	N7
5	IO_L09N_5/VREF_5	M7
5	IO_L09P_5	M6
5	IO_L07N_5/VREF_5	N6

FG456/FGG456 Fine-Pitch BGA Package

As shown in Table 6, XC2VP2, XC2VP4, and XC2VP7 Virtex-II Pro devices are available in the FG456/FGG456 fine-pitch BGA package. The pins in these devices are same, except for the differences shown in the "No Connects" column. Following this table are the FG456/FGG456 Fine-Pitch BGA Package Specifications (1.00mm pitch).

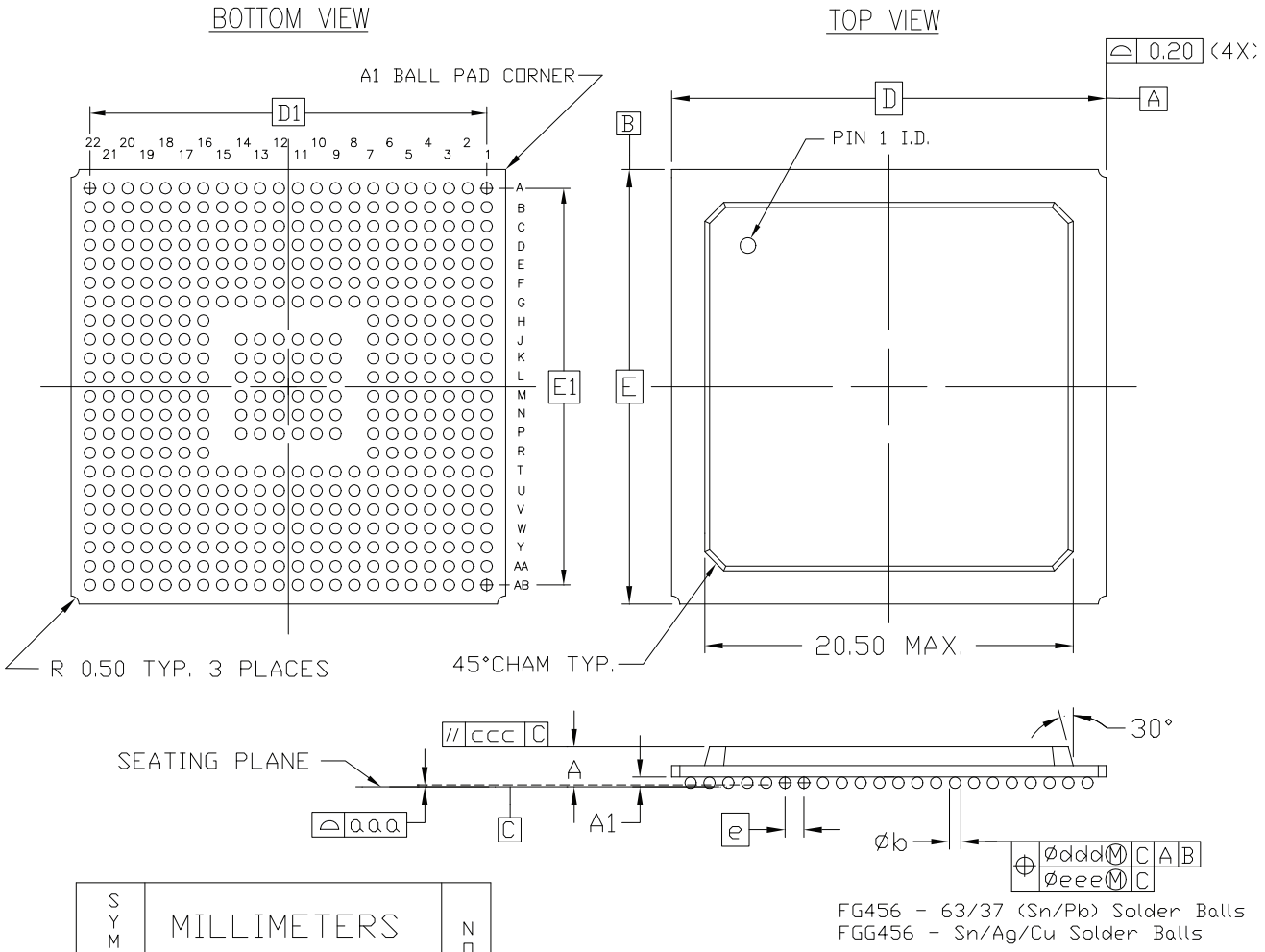
Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L01N_0/VRP_0	D5			
0	IO_L01P_0/VRN_0	D6			
0	IO_L02N_0	E6			
0	IO_L02P_0	E7			
0	IO_L03N_0	D7			
0	IO_L03P_0/VREF_0	C7			
0	IO_L05_0/No_Pair	E8			
0	IO_L06N_0	D8			
0	IO_L06P_0	C8			
0	IO_L07N_0	F9			
0	IO_L07P_0	E9			
0	IO_L09N_0	D9			
0	IO_L09P_0/VREF_0	D10			
0	IO_L67N_0	F10			
0	IO_L67P_0	E10			
0	IO_L69N_0	C10			
0	IO_L69P_0/VREF_0	B11			
0	IO_L74N_0/GCLK7P	F11			
0	IO_L74P_0/GCLK6S	E11			
0	IO_L75N_0/GCLK5P	D11			
0	IO_L75P_0/GCLK4S	C11			
1	IO_L75N_1/GCLK3P	C12			
1	IO_L75P_1/GCLK2S	D12			
1	IO_L74N_1/GCLK1P	E12			
1	IO_L74P_1/GCLK0S	F12			
1	IO_L69N_1/VREF_1	B12			
1	IO_L69P_1	C13			
1	IO_L67N_1	E13			
1	IO_L67P_1	F13			
1	IO_L09N_1/VREF_1	D13			
1	IO_L09P_1	D14			
1	IO_L07N_1	E14			

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	VCCO_7	K7			
7	VCCO_7	J7			
7	VCCO_7	H6			
7	VCCO_7	G6			
N/A	CCLK	W20			
N/A	PROG_B	B1			
N/A	DONE	Y18			
N/A	M0	Y4			
N/A	M1	W3			
N/A	M2	Y5			
N/A	TCK	B22			
N/A	TDI	D3			
N/A	TDO	D20			
N/A	TMS	A21			
N/A	PWRDWN_B	Y19			
N/A	HSWAP_EN	A2			
N/A	RSVD	C18			
N/A	VBATT	C19			
N/A	DXP	C4			
N/A	DXN	C5			
N/A	AVCCAUXTX4	B4	NC	NC	
N/A	VTTXPAD4	B3	NC	NC	
N/A	TXNPAD4	A3	NC	NC	
N/A	TXPPAD4	A4	NC	NC	
N/A	GNDA4	C6	NC	NC	
N/A	RXPPAD4	A5	NC	NC	
N/A	RXNPAD4	A6	NC	NC	
N/A	VTRXPAD4	B5	NC	NC	
N/A	AVCCAUXRX4	B6	NC	NC	
N/A	AVCCAUXTX6	B8			
N/A	VTTXPAD6	B7			
N/A	TXNPAD6	A7			
N/A	TXPPAD6	A8			
N/A	GNDA6	C9			
N/A	RXPPAD6	A9			
N/A	RXNPAD6	A10			

FG456/FGG456 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A			2.60	3
A_1	0.35	0.50	0.60	
D/E	23.00 BSC			
D_1/E_1	21.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	22			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. NOMINAL 'A' DIMENSION IS TYPICALLY 2.20mm.
4. CONFORMS TO JEDEC MS-034-AAJ-1 (DEPOPULATED)

Figure 2: **FG456/FGG456 Fine-Pitch BGA Package Specifications**

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
3	IO_L03P_3	AC25			
3	IO_L02N_3	AC24			
3	IO_L02P_3	AD25			
3	IO_L01N_3/VRP_3	AD26			
3	IO_L01P_3/VRN_3	AE26			
4	IO_L01N_4/BUSY/DOUT(1)	AB22			
4	IO_L01P_4/INIT_B	AC22			
4	IO_L02N_4/D0/DIN(1)	AB21			
4	IO_L02P_4/D1	AC21			
4	IO_L03N_4/D2	Y20			
4	IO_L03P_4/D3	AA20			
4	IO_L05_4/No_Pair	AB20			
4	IO_L06N_4/VRP_4	AC20			
4	IO_L06P_4/VRN_4	AD20			
4	IO_L07N_4	W19			
4	IO_L07P_4/VREF_4	Y19			
4	IO_L09N_4	AA19			
4	IO_L09P_4/VREF_4	AB19			
4	IO_L37N_4	AE19			
4	IO_L37P_4	AF19			
4	IO_L39N_4	W18			
4	IO_L39P_4	Y18			
4	IO_L43N_4	AA18			
4	IO_L43P_4	AB18			
4	IO_L45N_4	AC18			
4	IO_L45P_4/VREF_4	AD18			
4	IO_L46N_4	W17			
4	IO_L46P_4	W16			
4	IO_L48N_4	AB17			
4	IO_L48P_4	AB16			
4	IO_L49N_4	AC17			
4	IO_L49P_4	AD17			
4	IO_L50_4/No_Pair	Y16			
4	IO_L53_4/No_Pair	AA16			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	AVCCAUXRX21	AE7			
N/A	VTRXPAD21	AE6			
N/A	RXNPAD21	AF7			
N/A	RXPPAD21	AF6			
N/A	GNDA21	AD6			
N/A	TXPPAD21	AF5			
N/A	TXNPAD21	AF4			
N/A	VTTXPAD21	AE4			
N/A	AVCCAUXTX21	AE5			
N/A	M2	AD4			
N/A	M0	AF3			
N/A	M1	AE3			
N/A	TDI	D3			
N/A	VCCINT	G10			
N/A	VCCINT	G13			
N/A	VCCINT	G14			
N/A	VCCINT	G17			
N/A	VCCINT	J9			
N/A	VCCINT	J18			
N/A	VCCINT	K7			
N/A	VCCINT	K10			
N/A	VCCINT	K11			
N/A	VCCINT	K16			
N/A	VCCINT	K17			
N/A	VCCINT	K20			
N/A	VCCINT	L10			
N/A	VCCINT	L17			
N/A	VCCINT	N7			
N/A	VCCINT	N20			
N/A	VCCINT	P7			
N/A	VCCINT	P20			
N/A	VCCINT	T10			
N/A	VCCINT	T17			
N/A	VCCINT	U7			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	GND	K15			
N/A	GND	K17			
N/A	GND	L11			
N/A	GND	L12			
N/A	GND	L13			
N/A	GND	L14			
N/A	GND	L15			
N/A	GND	L16			
N/A	GND	M10			
N/A	GND	M11			
N/A	GND	M12			
N/A	GND	M13			
N/A	GND	M14			
N/A	GND	M15			
N/A	GND	M16			
N/A	GND	M17			
N/A	GND	N10			
N/A	GND	N11			
N/A	GND	N12			
N/A	GND	N13			
N/A	GND	N14			
N/A	GND	N15			
N/A	GND	N16			
N/A	GND	N17			
N/A	GND	P10			
N/A	GND	P11			
N/A	GND	P12			
N/A	GND	P13			
N/A	GND	P14			
N/A	GND	P15			
N/A	GND	P16			
N/A	GND	P17			
N/A	GND	R10			
N/A	GND	R11			
N/A	GND	R12			
N/A	GND	R13			
N/A	GND	R14			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
1	IO_L37N_1	G13				
1	IO_L37P_1	H13				
1	IO_L27N_1/VREF_1	J13	NC	NC		
1	IO_L27P_1	K13	NC	NC		
1	IO_L26N_1	D8	NC	NC		
1	IO_L26P_1	E8	NC	NC		
1	IO_L25N_1	F12	NC	NC		
1	IO_L25P_1	G12	NC	NC		
1	IO_L21N_1	G11	NC	NC		
1	IO_L21P_1	H11	NC	NC		
1	IO_L20N_1	C7	NC	NC		
1	IO_L20P_1	D7	NC	NC		
1	IO_L19N_1	E11	NC	NC		
1	IO_L19P_1	F11	NC	NC		
1	IO_L09N_1/VREF_1	J12				
1	IO_L09P_1	K12				
1	IO_L08N_1	D6				
1	IO_L08P_1	D5				
1	IO_L07N_1	E9				
1	IO_L07P_1	F9				
1	IO_L06N_1	J11				
1	IO_L06P_1	K11				
1	IO_L05_1/No_Pair	J10				
1	IO_L03N_1/VREF_1	G10				
1	IO_L03P_1	H10				
1	IO_L02N_1	G9				
1	IO_L02P_1	H9				
1	IO_L01N_1/VRP_1	E7				
1	IO_L01P_1/VRN_1	E6				
2	IO_L01N_2/VRP_2	D2				
2	IO_L01P_2/VRN_2	D1				
2	IO_L02N_2	F8				
2	IO_L02P_2	F7				
2	IO_L03N_2	E4				
2	IO_L03P_2	E3				
2	IO_L04N_2/VREF_2	E2				
2	IO_L04P_2	E1				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
6	IO_L34P_6	AE30				
6	IO_L34N_6	AE31				
6	IO_L35P_6	AD27				
6	IO_L35N_6	AD28				
6	IO_L36P_6	AF33				
6	IO_L36N_6	AE33				
6	IO_L37P_6	AD29				
6	IO_L37N_6	AD30				
6	IO_L38P_6	AB25				
6	IO_L38N_6	AB26				
6	IO_L39P_6	AD31				
6	IO_L39N_6/VREF_6	AD32				
6	IO_L40P_6	AC28				
6	IO_L40N_6	AC29				
6	IO_L41P_6	AB27				
6	IO_L41N_6	AB28				
6	IO_L42P_6	AE34				
6	IO_L42N_6	AD34				
6	IO_L43P_6	AC31				
6	IO_L43N_6	AC32				
6	IO_L44P_6	AA25				
6	IO_L44N_6	AA26				
6	IO_L45P_6	AD33				
6	IO_L45N_6/VREF_6	AC33				
6	IO_L46P_6	AB29				
6	IO_L46N_6	AB30				
6	IO_L47P_6	AA27				
6	IO_L47N_6	AA28				
6	IO_L48P_6	AB31				
6	IO_L48N_6	AB32				
6	IO_L49P_6	AA29				
6	IO_L49N_6	AA30				
6	IO_L50P_6	Y25				
6	IO_L50N_6	Y26				
6	IO_L51P_6	AC34				
6	IO_L51N_6/VREF_6	AB34				
6	IO_L52P_6	AA31				
6	IO_L52N_6	AA32				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
2	IO_L59P_2	U11		
2	IO_L60N_2	R1		
2	IO_L60P_2	R2		
2	IO_L85N_2	T3		
2	IO_L85P_2	T4		
2	IO_L86N_2	U8		
2	IO_L86P_2	U9		
2	IO_L87N_2	U2		
2	IO_L87P_2	T2		
2	IO_L88N_2/VREF_2	U4		
2	IO_L88P_2	U5		
2	IO_L89N_2	U6		
2	IO_L89P_2	U7		
2	IO_L90N_2	V3		
2	IO_L90P_2	U3		
3	IO_L90N_3	V6		
3	IO_L90P_3	V7		
3	IO_L89N_3	V10		
3	IO_L89P_3	V11		
3	IO_L88N_3	V4		
3	IO_L88P_3	V5		
3	IO_L87N_3/VREF_3	V2		
3	IO_L87P_3	W2		
3	IO_L86N_3	V8		
3	IO_L86P_3	V9		
3	IO_L85N_3	W6		
3	IO_L85P_3	W7		
3	IO_L60N_3	W3		
3	IO_L60P_3	W4		
3	IO_L59N_3	W10		
3	IO_L59P_3	W11		
3	IO_L58N_3	Y5		
3	IO_L58P_3	Y6		
3	IO_L57N_3/VREF_3	Y3		
3	IO_L57P_3	AA3		
3	IO_L56N_3	W8		
3	IO_L56P_3	Y7		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L86N_7	W28		
7	IO_L85P_7	W34		
7	IO_L85N_7	W35		
7	IO_L60P_7	W32		
7	IO_L60N_7	W33		
7	IO_L59P_7	W29		
7	IO_L59N_7	W30		
7	IO_L58P_7	V38		
7	IO_L58N_7/VREF_7	V39		
7	IO_L57P_7	V36		
7	IO_L57N_7	V37		
7	IO_L56P_7	V28		
7	IO_L56N_7	V29		
7	IO_L55P_7	V34		
7	IO_L55N_7	V35		
7	IO_L54P_7	V32		
7	IO_L54N_7	V33		
7	IO_L53P_7	V30		
7	IO_L53N_7	V31		
7	IO_L52P_7	U38		
7	IO_L52N_7/VREF_7	U39		
7	IO_L51P_7	T36		
7	IO_L51N_7	U36		
7	IO_L50P_7	V27		
7	IO_L50N_7	U27		
7	IO_L49P_7	U34		
7	IO_L49N_7	U35		
7	IO_L48P_7	T37		
7	IO_L48N_7	T38		
7	IO_L47P_7	U30		
7	IO_L47N_7	U31		
7	IO_L46P_7	T33		
7	IO_L46N_7/VREF_7	T34		
7	IO_L45P_7	R38		
7	IO_L45N_7	R39		
7	IO_L44P_7	T32		
7	IO_L44N_7	U32		
7	IO_L43P_7	R36		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L82N_7/VREF_7	G37	NC	
7	IO_L81P_7	G33	NC	
7	IO_L81N_7	G34	NC	
7	IO_L79P_7	F38	NC	
7	IO_L79N_7	F39	NC	
7	IO_L78P_7	F36	NC	
7	IO_L78N_7	F37	NC	
7	IO_L76P_7	G35	NC	
7	IO_L76N_7/VREF_7	F35	NC	
7	IO_L75P_7	E37	NC	
7	IO_L75N_7	E38	NC	
7	IO_L73P_7	D38	NC	
7	IO_L73N_7	D39	NC	
7	IO_L06P_7	F33		
7	IO_L06N_7	E33		
7	IO_L05P_7	J31		
7	IO_L05N_7	H32		
7	IO_L04P_7	E34		
7	IO_L04N_7/VREF_7	D34		
7	IO_L03P_7	D35		
7	IO_L03N_7	C35		
7	IO_L02P_7	H31		
7	IO_L02N_7	G31		
7	IO_L01P_7/VRN_7	D33		
7	IO_L01N_7/VRP_7	C33		
7	VCCO_7	E39		
7	VCCO_7	U37		
7	VCCO_7	N36		
7	VCCO_7	J36		
7	VCCO_7	E36		
7	VCCO_7	Y35		
7	VCCO_7	U33		
7	VCCO_7	N32		
7	VCCO_7	J32		
7	VCCO_7	F32		
7	VCCO_7	U29		
7	VCCO_7	N28		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		E22		
N/A	GND		E21		
N/A	GND		E5		
N/A	GND		D39		
N/A	GND		D32		
N/A	GND		D28		
N/A	GND		D15		
N/A	GND		D11		
N/A	GND		D4		
N/A	GND		C42		
N/A	GND		C41		
N/A	GND		C40		
N/A	GND		C3		
N/A	GND		C2		
N/A	GND		C1		
N/A	GND		B42		
N/A	GND		B1		
N/A	GND		N14		
N/A	GND		N29		
N/A	GND		AK14		
N/A	GND		AK29		
N/A	GND		P13		
N/A	GND		P30		
N/A	GND		AJ13		
N/A	GND		AJ30		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L56N_3	AC11	
3	IO_L56P_3	AC12	
3	IO_L55N_3	AD3	
3	IO_L55P_3	AE3	
3	IO_L54N_3	AE1	
3	IO_L54P_3	AE2	
3	IO_L53N_3	AC6	
3	IO_L53P_3	AC7	
3	IO_L52N_3	AF2	
3	IO_L52P_3	AF3	
3	IO_L51N_3/VREF_3	AF6	
3	IO_L51P_3	AG6	
3	IO_L50N_3	AD10	
3	IO_L50P_3	AD11	
3	IO_L49N_3	AG4	
3	IO_L49P_3	AG5	
3	IO_L48N_3	AF4	
3	IO_L48P_3	AG3	
3	IO_L47N_3	AC10	
3	IO_L47P_3	AD9	
3	IO_L46N_3	AG1	
3	IO_L46P_3	AG2	
3	IO_L45N_3/VREF_3	AG7	
3	IO_L45P_3	AH7	
3	IO_L44N_3	AC8	
3	IO_L44P_3	AD7	
3	IO_L43N_3	AH4	
3	IO_L43P_3	AH5	
3	IO_L42N_3	AH1	
3	IO_L42P_3	AH2	
3	IO_L41N_3	AE10	
3	IO_L41P_3	AE11	
3	IO_L40N_3	AJ6	
3	IO_L40P_3	AJ7	
3	IO_L39N_3/VREF_3	AH6	
3	IO_L39P_3	AJ5	
3	IO_L38N_3	AE8	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	M2	AM33	
N/A	TCK	K10	
N/A	TDI	M32	
N/A	TDO	M11	
N/A	TMS	L10	
N/A	PWRDWN_B	AP10	
N/A	HSWAP_EN	K33	
N/A	RSVD	J10	
N/A	VBATT	M12	
N/A	DXP	M31	
N/A	DXN	L33	
N/A	VCCINT	AK30	
N/A	VCCINT	N30	
N/A	VCCINT	AJ29	
N/A	VCCINT	P29	
N/A	VCCINT	AJ28	
N/A	VCCINT	AH28	
N/A	VCCINT	R28	
N/A	VCCINT	P28	
N/A	VCCINT	AJ27	
N/A	VCCINT	AH27	
N/A	VCCINT	AG27	
N/A	VCCINT	AF27	
N/A	VCCINT	AE27	
N/A	VCCINT	AD27	
N/A	VCCINT	AC27	
N/A	VCCINT	AB27	
N/A	VCCINT	AA27	
N/A	VCCINT	Y27	
N/A	VCCINT	W27	
N/A	VCCINT	V27	
N/A	VCCINT	U27	
N/A	VCCINT	T27	
N/A	VCCINT	R27	
N/A	VCCINT	P27	
N/A	VCCINT	AH26	