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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8272
Number of Logic Elements/Cells	74448
Total RAM Bits	6045696
Number of I/O	996
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1704-BBGA, FCBGA
Supplier Device Package	1704-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp70-6ff1704c

Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview

DS083 (v5.0) June 21, 2011 **Product Specification**

Summary of Virtex-II Pro™ / Virtex-II Pro X Features

- High-Performance Platform FPGA Solution, Including
  - Up to twenty RocketIO™ or RocketIO X embedded Multi-Gigabit Transceivers (MGTs)
  - Up to two IBM PowerPC™ RISC processor blocks
- Based on Virtex-II™ Platform FPGA Technology
  - Flexible logic resources
  - SRAM-based in-system configuration
  - Active Interconnect technology
  - SelectRAM™+ memory hierarchy
  - Dedicated 18-bit x 18-bit multiplier blocks
  - High-performance clock management circuitry
  - SelectI/O™-Ultra technology
  - XCITE Digitally Controlled Impedance (DCI) I/O

Virtex-II Pro / Virtex-II Pro X family members and resources are shown in Table 1.

Table 1: **Virtex-II Pro / Virtex-II Pro X FPGA Family Members**

Device(1)	RocketIO Transceiver Blocks	PowerPC Processor Blocks	Logic Cells(2)	CLB (1 = 4 slices = max 128 bits)		18 X 18 Bit Multiplier Blocks	Block SelectRAM+		DCMs	Maximum User I/O Pads
				Slices	Max Distr RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)		
XC2VP2	4	0	3,168	1,408	44	12	12	216	4	204
XC2VP4	4	1	6,768	3,008	94	28	28	504	4	348
XC2VP7	8	1	11,088	4,928	154	44	44	792	4	396
XC2VP20	8	2	20,880	9,280	290	88	88	1,584	8	564
XC2VPX20	8(4)	1	22,032	9,792	306	88	88	1,584	8	552
XC2VP30	8	2	30,816	13,696	428	136	136	2,448	8	644
XC2VP40	0(3), 8, or 12	2	43,632	19,392	606	192	192	3,456	8	804
XC2VP50	0(3) or 16	2	53,136	23,616	738	232	232	4,176	8	852
XC2VP70	16 or 20	2	74,448	33,088	1,034	328	328	5,904	8	996
XC2VPX70	20(4)	2	74,448	33,088	1,034	308	308	5,544	8	992
XC2VP100	0(3) or 20	2	99,216	44,096	1,378	444	444	7,992	12	1,164

Notes:
1. -7 speed grade devices are not available in Industrial grade.
2. Logic Cell ≈ (1) 4-input LUT + (1)FF + Carry Logic
3. These devices can be ordered in a configuration without RocketIO transceivers. See Table 3 for package configurations.
4. Virtex-II Pro X devices equipped with RocketIO X transceiver cores.

RocketIO X Transceiver Features (XC2VPX20 and XC2VPX70 Only)

- Variable-Speed Full-Duplex Transceiver (XC2VPX20) Allowing 2.488 Gb/s to 6.25 Gb/s Baud Transfer Rates.
  - Includes specific baud rates used by various standards, as listed in Table 4, Module 2.
- Fixed-Speed Full-Duplex Tranceiver (XC2VPX70) Operating at 4.25 Gb/s Baud Transfer Rate.
- Eight or Twenty Transceiver Modules on an FPGA, Depending upon Device
- Monolithic Clock Synthesis and Clock Recovery
  - Eliminates the need for external components
- Automatic Lock-to-Reference Function
- Programmable Serial Output Differential Swing
  - 200 mV to 1600 mV, peak-peak
  - Allows compatibility with other serial system voltage levels
- Programmable Pre-emphasis Levels 0 to 500%
- Telecom/Datacom Support Modes
  - "x8" and "x10" clocking/data paths
  - 64B/66B clocking support

- HSTL (1.5V and 1.8V, Class I, II, III, and IV)
- SSTL (1.8V and 2.5V, Class I and II)

The DCI I/O feature automatically provides on-chip termination for each single-ended I/O standard.

The IOB elements also support the following differential signaling I/O standards:

- LVDS and Extended LVDS (2.5V)
- BLVDS (Bus LVDS)
- ULVDS
- LDT
- LVPECL (2.5V)

Two adjacent pads are used for each differential pair. Two or four IOBs connect to one switch matrix to access the routing resources. On-chip differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards.

Configurable Logic Blocks (CLBs)

CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains:

- Two function generators (F & G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Wide function capability
- Fast carry look-ahead chain
- Horizontal cascade chain (OR gate)

The function generators F & G are configurable as 4-input look-up tables (LUTs), as 16-bit shift registers, or as 16-bit distributed SelectRAM+ memory.

In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

Block SelectRAM+ Memory

The block SelectRAM+ memory resources are 18 Kb of True Dual-Port RAM, programmable from 16K x 1 bit to 512 x 36 bit, in various depth and width configurations. Each port is totally synchronous and independent, offering three "read-during-write" modes. Block SelectRAM+ memory is cascadable to implement large embedded storage blocks. Supported memory configurations for dual-port and single-port modes are shown in Table 2.

Table 2: **Dual-Port and Single-Port Configurations**

16K x 1 bit	4K x 4 bits	1K x 18 bits
8K x 2 bits	2K x 9 bits	512 x 36 bits

18 X 18 Bit Multipliers

A multiplier block is associated with each SelectRAM+ memory block. The multiplier block is a dedicated 18 x 18-bit 2s complement signed multiplier, and is optimized for operations based on the block SelectRAM+ content on one port. The 18 x 18 multiplier can be used independently of the block SelectRAM+ resource. Read/multiply/accumulate operations and DSP filter structures are extremely efficient.

Both the SelectRAM+ memory and the multiplier resource are connected to four switch matrices to access the general routing resources.

Global Clocking

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clock schemes.

Up to twelve DCM blocks are available. To generate deskewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90-, 180-, and 270-degree phase-shifted versions of its output clocks. Fine-grained phase shifting offers high-resolution phase adjustments in increments of $^1/_{256}$ of the clock period. Very flexible frequency synthesis provides a clock output frequency equal to a fractional or integer multiple of the input clock frequency. For exact timing parameters, see Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics.

Virtex-II Pro devices have 16 global clock MUX buffers, with up to eight clock nets per quadrant. Each clock MUX buffer can select one of the two clock inputs and switch glitch-free from one clock to the other. Each DCM can send up to four of its clock outputs to global clock buffers on the same edge. Any global clock pin can drive any DCM on the same edge.

Routing Resources

The IOB, CLB, block SelectRAM+, multiplier, and DCM elements all use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance of high-speed designs.

There are a total of 16 global clock lines, with eight available per quadrant. In addition, 24 vertical and horizontal long lines per row or column, as well as massive secondary and local routing resources, provide fast interconnect. Virtex-II Pro buffered interconnects are relatively unaffected by net fanout, and the interconnect layout is designed to minimize crosstalk.

Horizontal and vertical routing resources for each row or column include:

- 24 long lines
- 120 hex lines
- 40 double lines
- 16 direct connect lines (total in all four directions)

Boundary Scan

Boundary-scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-II Pro devices, complying with IEEE standards 1149.1 and 1532. A system mode and a test mode are

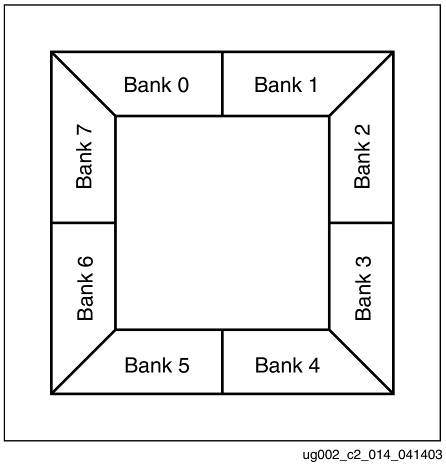

Figure 24: **I/O Banks: Wire-Bond Packages (FG) Top View**

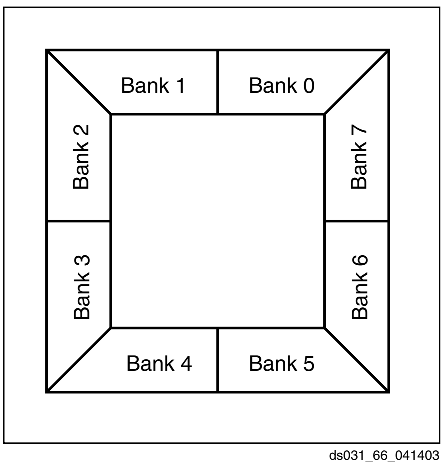

Figure 25: **I/O Banks: Flip-Chip Packages (FF) Top View**

Some input standards require a user-supplied threshold voltage (V_{REF}), and certain user-I/O pins are automatically configured as V_{REF} inputs. Approximately one in six of the I/O pins in the bank assume this role.

V_{REF} pins within a bank are interconnected internally, thus only one V_{REF} voltage can be used within each bank. However, for correct operation, all V_{REF} pins in the bank must be connected to the external reference voltage source.

The V_{CCO} and the V_{REF} pins for each bank appear in the device pinout tables. Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary.

All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage and not used for I/O. In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or, if necessary, they can be connected to V_{CCO} to permit migration to a larger device.

Rules for Combining I/O Standards in the Same Bank

The following rules must be obeyed to combine different input, output, and bi-directional standards in the same bank:

1. **Combining output standards only.** Output standards with the same output V_{CCO} requirement can be combined in the same bank.
   Compatible example:
   SSTL2_I and LVDS_25 outputs
   Incompatible example:
   SSTL2_I (output V_{CCO} = 2.5V) and
   LVCMOS33 (output V_{CCO} = 3.3V) outputs
2. **Combining input standards only.** Input standards with the same input V_{CCO} and input V_{REF} requirements can be combined in the same bank.
   Compatible example:
   LVCMOS15 and HSTL_IV inputs
   Incompatible example:
   LVCMOS15 (input V_{CCO} = 1.5V) and
   LVCMOS18 (input V_{CCO} = 1.8V) inputs
   Incompatible example:
   HSTL_I_DCI_18 (V_{REF} = 0.9V) and
   HSTL_IV_DCI_18 (V_{REF} = 1.1V) inputs
3. **Combining input standards and output standards.** Input standards and output standards with the same input V_{CCO} and output V_{CCO} requirement can be combined in the same bank.
   Compatible example:
   LVDS_25 output and HSTL_I input
   Incompatible example:
   LVDS_25 output (output V_{CCO} = 2.5V) and
   HSTL_I_DCI_18 input (input V_{CCO} = 1.8V)
4. **Combining bi-directional standards with input or output standards.** When combining bi-directional I/O with other standards, make sure the bi-directional standard can meet rules 1 through 3 above.
5. **Additional rules for combining DCI I/O standards.**
   a. No more than one Single Termination type (input or output) is allowed in the same bank.
      Incompatible example:
      HSTL_IV_DCI input and HSTL_III_DCI input
   b. No more than one Split Termination type (input or output) is allowed in the same bank.
      Incompatible example:
      HSTL_I_DCI input and HSTL_II_DCI input

The implementation tools will enforce the above design rules.

Table 12, page 30, summarizes all standards and voltage supplies.

Multiplexers

Virtex-II Pro function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II Pro slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in Figure 41. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II Pro Platform FPGA User Guide*. Any LUT can implement a 2:1 multiplexer.

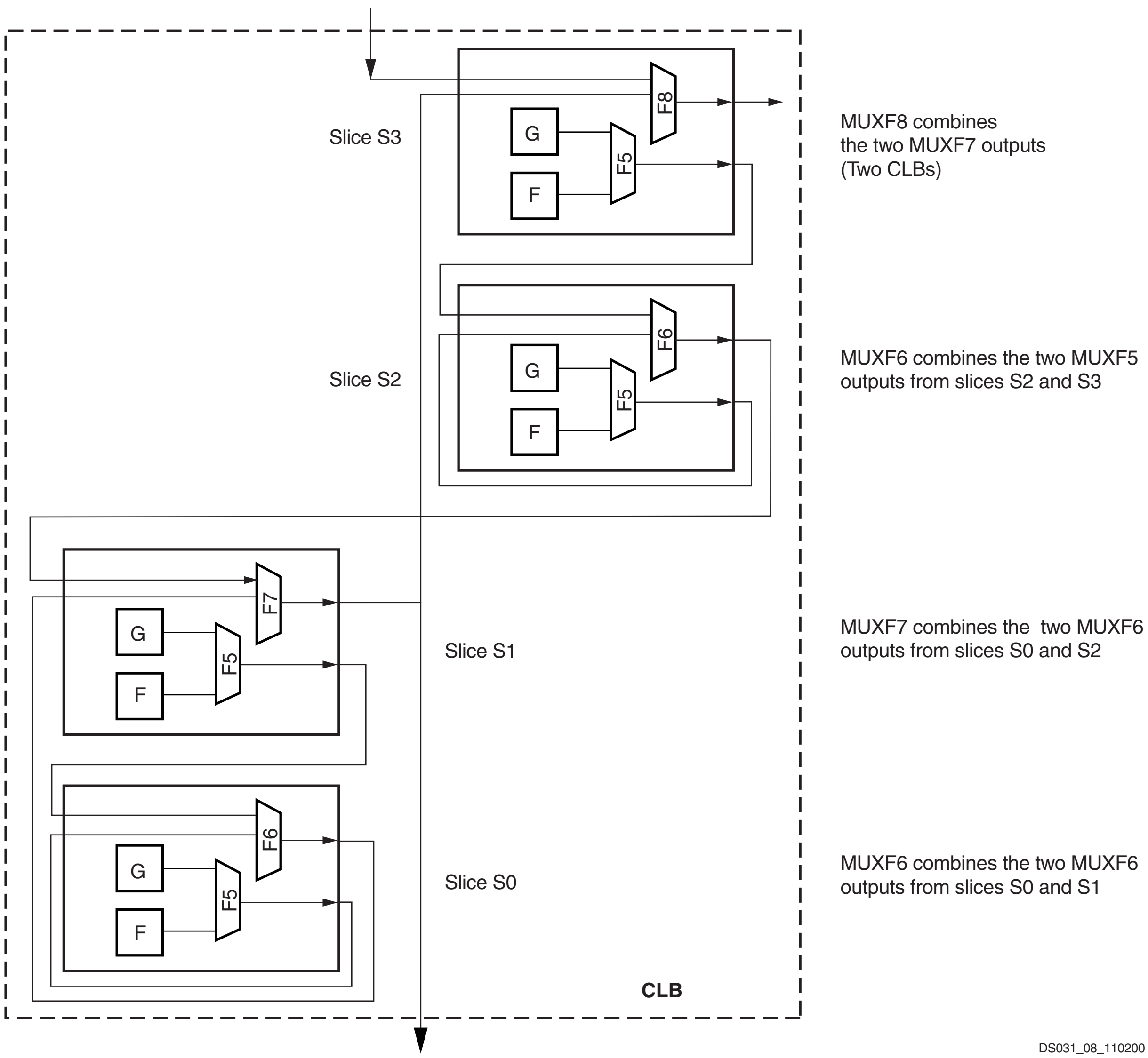

Figure 41: **MUXF5 and MUXFX multiplexers**

Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II Pro CLB has two separate carry chains, as shown in the Figure 42.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II Pro device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also be used to cascade function generators for implementing wide logic functions.

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in Figure 34) improves the efficiency of multiplier implementation.

CLB/Slice Configurations

Table 19 summarizes the logic resources in one CLB. All of the CLBs are identical and each CLB or slice can be implemented in one of the configurations listed. Table 20 shows the available resources in all CLBs.

Table 19: **Logic Resources in One CLB**

Slices	LUTs	Flip-Flops	MULT_ANDs	Arithmetic & Carry-Chains	SOP Chains	Distributed SelectRAM+	Shift Registers	TBUF
4	8	8	8	2	2	128 bits	128 bits	2

Table 20: **Virtex-II Pro Logic Resources Available in All CLBs**

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM or Shift Register (bits)	Number of Flip-Flops	Number of Carry-Chains(1)	Number of SOP Chains(1)
XC2VP2	16 x 22	1,408	2,816	45,056	2,816	44	32
XC2VP4	40 x 22	3,008	6,016	96,256	6,016	44	80
XC2VP7	40 x 34	4,928	9,856	157,696	9,856	68	80
XC2VP20	56 x 46	9,280	18,560	296,960	18,560	92	112
XC2VPX20	56 x 46	9,792	19,584	313,334	18,560	92	112
XC2VP30	80 x 46	13,696	27,392	438,272	27,392	92	160
XC2VP40	88 x 58	19,392	38,784	620,544	38,784	116	176
XC2VP50	88 x 70	23,616	47,232	755,712	47,232	140	176
XC2VP70	104 x 82	33,088	66,176	1,058,816	66,176	164	208
XC2VPX70	104 x 82	33,088	66,176	1,058,816	66,176	164	208
XC2VP100	120 x 94	44,096	88,192	1,411,072	88,192	188	240

Notes:
1. The carry-chains and SOP chains can be split or cascaded.

18 Kb Block SelectRAM+ Resources

Introduction

Virtex-II Pro devices incorporate large amounts of 18 Kb block SelectRAM+ resources. These complement the distributed SelectRAM+ resources that provide shallow RAM structures implemented in CLBs. Each Virtex-II Pro block SelectRAM+ resource is an 18 Kb true dual-port RAM with two independently clocked and independently controlled synchronous ports that access a common storage area. Both ports are functionally identical. CLK, EN, WE, and SSR polarities are defined through configuration.

Each port has the following types of inputs: Clock and Clock Enable, Write Enable, Set/Reset, and Address, as well as separate Data/parity data inputs (for write) and Data/parity data outputs (for read).

Operation is synchronous; the block SelectRAM+ behaves like a register. Control, address and data inputs must (and need only) be valid during the set-up time window prior to a rising (or falling, a configuration option) clock edge. Data outputs change as a result of the same clock edge.

Configuration

Virtex-II Pro block SelectRAM+ supports various configurations, including single- and dual-port RAM and various data/address aspect ratios. Supported memory configurations for single- and dual-port modes are shown in Table 21.

Table 21: **Dual- and Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

Single-Port Configuration

As a single-port RAM, the block SelectRAM+ has access to the 18 Kb memory locations in any of the 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations and to 16 Kb memory locations in any of the 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations. The advantage of the 9-bit, 18-bit and 36-bit widths is the ability to store a parity bit for each eight bits. Parity bits must be generated or checked exter-

Table 35: **IOB Input Switching Characteristics *(Continued)***

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All	0.84/–0.61	0.86/–0.63	0.90/–0.67	ns, min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$	XC2VP2	2.28/–1.89	2.60/–2.15	2.95/–2.43	ns, max
		XC2VP4	2.55/–2.10	2.87/–2.36	3.21/–2.65	ns, max
		XC2VP7	2.48/–2.05	2.82/–2.32	3.15/–2.60	ns, max
		XC2VP20	2.63/–2.05	3.02/–2.35	3.40/–2.66	ns, max
		XC2VPX20	2.63/–2.05	3.02/–2.35	3.40/–2.66	ns, max
		XC2VP30	2.67/–2.07	3.09/–2.42	3.49/–2.73	ns, max
		XC2VP40	3.28/–2.56	3.61/–2.83	4.01/–3.15	ns, max
		XC2VP50	3.84/–3.02	4.08/–3.21	4.42/–3.48	ns, max
		XC2VP70	3.98/–3.13	4.23/–3.33	4.55/–3.58	ns, max
		XC2VPX70	3.98/–3.13	4.23/–3.33	4.55/–3.58	ns, max
		XC2VP100	N/A	6.48/–5.13	7.04/–5.57	ns, max
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All	0.39/ 0.01	0.44/ 0.01	0.49/ 0.01	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.52	0.57	0.75	ns, min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	1.13	1.27	1.42	ns, max
GSR to output IQ	T_{GSRQ}	All	5.87	6.75	7.43	ns, max

Notes:
1. Input timing for LVCMOS25 is measured at 1.25V. For other I/O standards, see Table 39.

Table 40: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	C_{REF}[(1)] (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	50	0	V_{REF}	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	50	0	V_{REF}	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	1M	0	1.2	0
LDT (HyperTransport), 2.5V	LDT_25	50	0	V_{REF}	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	1M	0	1.23	0
LVDCI/HSLVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	1M	0	1.65	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III & IV, with DCI	HSTL_III_DCI, HSTL_IV_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III & IV, 1.8V, with DCI	HSTL_III_DCI_18, HSTL_IV_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	50	0	0.8	1.2
GTL Plus with DCI	GTLP_DCI	50	0	1.0	1.5

Notes:
1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Measured as per PCI specification.
3. Measured as per PCI-X specification.

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	GND	R15			
N/A	GND	R16			
N/A	GND	R24			
N/A	GND	T11			
N/A	GND	T12			
N/A	GND	T13			
N/A	GND	T14			
N/A	GND	T15			
N/A	GND	T16			
N/A	GND	U6			
N/A	GND	U21			
N/A	GND	W4			
N/A	GND	W23			
N/A	GND	AA10			
N/A	GND	AA17			
N/A	GND	AC4			
N/A	GND	AC8			
N/A	GND	AC19			
N/A	GND	AC23			
N/A	GND	AD3			
N/A	GND	AD24			
N/A	GND	AE2			
N/A	GND	AE25			
N/A	GND	AF1			
N/A	GND	AF26			

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
1	IO_L06N_1	E9			
1	IO_L06P_1	E8			
1	IO_L05_1/No_Pair	F8			
1	IO_L03N_1/VREF_1	D7			
1	IO_L03P_1	E7			
1	IO_L02N_1	C6			
1	IO_L02P_1	D6			
1	IO_L01N_1/VRP_1	A3			
1	IO_L01P_1/VRN_1	B3			
2	IO_L01N_2/VRP_2	C4			
2	IO_L01P_2/VRN_2	D3			
2	IO_L02N_2	A2			
2	IO_L02P_2	B1			
2	IO_L03N_2	C2			
2	IO_L03P_2	C1			
2	IO_L04N_2/VREF_2	D2			
2	IO_L04P_2	D1			
2	IO_L05N_2	E4			
2	IO_L05P_2	E3			
2	IO_L06N_2	E2			
2	IO_L06P_2	E1			
2	IO_L40N_2/VREF_2	F5	NC	NC	NC
2	IO_L40P_2	F4	NC	NC	NC
2	IO_L42N_2	F3	NC	NC	NC
2	IO_L42P_2	F2	NC	NC	NC
2	IO_L43N_2	G6	NC		
2	IO_L43P_2	G5	NC		
2	IO_L44N_2	G4	NC		
2	IO_L44P_2	G3	NC		
2	IO_L45N_2	F1	NC		
2	IO_L45P_2	G1	NC		
2	IO_L46N_2/VREF_2	H6	NC		
2	IO_L46P_2	H5	NC		
2	IO_L47N_2	H4	NC		
2	IO_L47P_2	H3	NC		
2	IO_L48N_2	H2	NC		

FF1152 Flip-Chip Fine-Pitch BGA Package

As shown in Table 10, XC2VP20, XC2VP30, XC2VP40, and XC2VP50 Virtex-II Pro devices are available in the FF1152 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
0	IO_L01N_0/VRP_0	E29				
0	IO_L01P_0/VRN_0	E28				
0	IO_L02N_0	H26				
0	IO_L02P_0	G26				
0	IO_L03N_0	H25				
0	IO_L03P_0/VREF_0	G25				
0	IO_L05_0/No_Pair	J25				
0	IO_L06N_0	K24				
0	IO_L06P_0	J24				
0	IO_L07N_0	F26				
0	IO_L07P_0	E26				
0	IO_L08N_0	D30				
0	IO_L08P_0	D29				
0	IO_L09N_0	K23				
0	IO_L09P_0/VREF_0	J23				
0	IO_L19N_0	F24	NC	NC		
0	IO_L19P_0	E24	NC	NC		
0	IO_L20N_0	D28	NC	NC		
0	IO_L20P_0	C28	NC	NC		
0	IO_L21N_0	H24	NC	NC		
0	IO_L21P_0	G24	NC	NC		
0	IO_L25N_0	G23	NC	NC		
0	IO_L25P_0	F23	NC	NC		
0	IO_L26N_0	E27	NC	NC		
0	IO_L26P_0	D27	NC	NC		
0	IO_L27N_0	K22	NC	NC		
0	IO_L27P_0/VREF_0	J22	NC	NC		
0	IO_L37N_0	H22				
0	IO_L37P_0	G22				
0	IO_L38N_0	D26				
0	IO_L38P_0	C26				
0	IO_L39N_0	K21				
0	IO_L39P_0	J21				
0	IO_L43N_0	F22				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
1	VCCO_1	L15				
1	VCCO_1	M13				
1	VCCO_1	M14				
1	VCCO_1	M15				
1	VCCO_1	M16				
1	VCCO_1	M17				
2	VCCO_2	F3				
2	VCCO_2	K6				
2	VCCO_2	M11				
2	VCCO_2	N11				
2	VCCO_2	N12				
2	VCCO_2	P11				
2	VCCO_2	P12				
2	VCCO_2	R5				
2	VCCO_2	R11				
2	VCCO_2	R12				
2	VCCO_2	T12				
2	VCCO_2	U12				
3	VCCO_3	V12				
3	VCCO_3	W12				
3	VCCO_3	Y5				
3	VCCO_3	Y11				
3	VCCO_3	Y12				
3	VCCO_3	AA11				
3	VCCO_3	AA12				
3	VCCO_3	AB11				
3	VCCO_3	AB12				
3	VCCO_3	AC11				
3	VCCO_3	AE6				
3	VCCO_3	AJ3				
4	VCCO_4	AC13				
4	VCCO_4	AC14				
4	VCCO_4	AC15				
4	VCCO_4	AC16				
4	VCCO_4	AC17				
4	VCCO_4	AD12				
4	VCCO_4	AD13				
4	VCCO_4	AD14				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
N/A	VCCINT	M23		
N/A	VCCINT	AB22		
N/A	VCCINT	AA22		
N/A	VCCINT	Y22		
N/A	VCCINT	W22		
N/A	VCCINT	V22		
N/A	VCCINT	U22		
N/A	VCCINT	T22		
N/A	VCCINT	R22		
N/A	VCCINT	P22		
N/A	VCCINT	N22		
N/A	VCCINT	AB21		
N/A	VCCINT	N21		
N/A	VCCINT	AB20		
N/A	VCCINT	N20		
N/A	VCCINT	AB19		
N/A	VCCINT	N19		
N/A	VCCINT	AB18		
N/A	VCCINT	N18		
N/A	VCCINT	AB17		
N/A	VCCINT	N17		
N/A	VCCINT	AB16		
N/A	VCCINT	N16		
N/A	VCCINT	AB15		
N/A	VCCINT	N15		
N/A	VCCINT	AB14		
N/A	VCCINT	N14		
N/A	VCCINT	AB13		
N/A	VCCINT	AA13		
N/A	VCCINT	Y13		
N/A	VCCINT	W13		
N/A	VCCINT	V13		
N/A	VCCINT	U13		
N/A	VCCINT	T13		
N/A	VCCINT	R13		
N/A	VCCINT	P13		
N/A	VCCINT	N13		
N/A	VCCINT	AC12		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
0	IO_L34P_0	E27	NC	
0	IO_L35N_0	L26	NC	
0	IO_L35P_0	L25	NC	
0	IO_L36N_0	G26	NC	
0	IO_L36P_0/VREF_0	H26	NC	
0	IO_L37N_0	E26		
0	IO_L37P_0	F26		
0	IO_L38N_0	K25		
0	IO_L38P_0	K24		
0	IO_L39N_0	C26		
0	IO_L39P_0	D26		
0	IO_L43N_0	H25		
0	IO_L43P_0	J25		
0	IO_L44N_0	M25		
0	IO_L44P_0	M24		
0	IO_L45N_0	F25		
0	IO_L45P_0/VREF_0	G25		
0	IO_L46N_0	C25		
0	IO_L46P_0	D25		
0	IO_L47N_0	L23		
0	IO_L47P_0	M22		
0	IO_L48N_0	H24		
0	IO_L48P_0	J24		
0	IO_L49N_0	E25		
0	IO_L49P_0	E24		
0	IO_L50_0/No_Pair	N23		
0	IO_L53_0/No_Pair	M23		
0	IO_L54N_0	H23		
0	IO_L54P_0	J23		
0	IO_L55N_0	F24		
0	IO_L55P_0	G23		
0	IO_L56N_0	K22		
0	IO_L56P_0	L22		
0	IO_L57N_0	C23		
0	IO_L57P_0/VREF_0	D23		
0	IO_L58N_0	H22		
0	IO_L58P_0	J22		
0	IO_L59N_0	N22		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L30N_2	N6		
2	IO_L30P_2	N7		
2	IO_L31N_2	M4		
2	IO_L31P_2	N5		
2	IO_L32N_2	R11		
2	IO_L32P_2	R12		
2	IO_L33N_2	N1		
2	IO_L33P_2	N2		
2	IO_L34N_2/VREF_2	P6		
2	IO_L34P_2	P7		
2	IO_L35N_2	R13		
2	IO_L35P_2	T13		
2	IO_L36N_2	P4		
2	IO_L36P_2	P5		
2	IO_L37N_2	P3		
2	IO_L37P_2	N3		
2	IO_L38N_2	T10		
2	IO_L38P_2	T11		
2	IO_L39N_2	P1		
2	IO_L39P_2	P2		
2	IO_L40N_2/VREF_2	R7		
2	IO_L40P_2	R8		
2	IO_L41N_2	T12		
2	IO_L41P_2	U12		
2	IO_L42N_2	R5		
2	IO_L42P_2	R6		
2	IO_L43N_2	R3		
2	IO_L43P_2	R4		
2	IO_L44N_2	U8		
2	IO_L44P_2	T8		
2	IO_L45N_2	R1		
2	IO_L45P_2	R2		
2	IO_L46N_2/VREF_2	T6		
2	IO_L46P_2	T7		
2	IO_L47N_2	U9		
2	IO_L47P_2	U10		
2	IO_L48N_2	T2		
2	IO_L48P_2	T3		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
5	IO_L57N_5/VREF_5	AT23		
5	IO_L57P_5	AU23		
5	IO_L56N_5	AJ22		
5	IO_L56P_5	AK22		
5	IO_L55N_5	AN23		
5	IO_L55P_5	AP24		
5	IO_L54N_5	AL23		
5	IO_L54P_5	AM23		
5	IO_L53_5/No_Pair	AH23		
5	IO_L50_5/No_Pair	AG23		
5	IO_L49N_5	AR24		
5	IO_L49P_5	AR25		
5	IO_L48N_5	AL24		
5	IO_L48P_5	AM24		
5	IO_L47N_5	AH22		
5	IO_L47P_5	AJ23		
5	IO_L46N_5	AT25		
5	IO_L46P_5	AU25		
5	IO_L45N_5/VREF_5	AN25		
5	IO_L45P_5	AP25		
5	IO_L44N_5	AH24		
5	IO_L44P_5	AH25		
5	IO_L43N_5	AL25		
5	IO_L43P_5	AM25		
5	IO_L39N_5	AT26		
5	IO_L39P_5	AU26		
5	IO_L38N_5	AK24		
5	IO_L38P_5	AK25		
5	IO_L37N_5	AP26		
5	IO_L37P_5	AR26		
5	IO_L36N_5/VREF_5	AM26	NC	
5	IO_L36P_5	AN26	NC	
5	IO_L35N_5	AJ25	NC	
5	IO_L35P_5	AJ26	NC	
5	IO_L34N_5	AR27	NC	
5	IO_L34P_5	AT27	NC	
5	IO_L30N_5	AN27	NC	
5	IO_L30P_5	AP28	NC	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
4	IO_L26P_4	AU12	
4	IO_L27N_4	AR12	
4	IO_L27P_4/VREF_4	AP12	
4	IO_L28N_4	AW13	
4	IO_L28P_4	AW12	
4	IO_L29N_4	BA12	
4	IO_L29P_4	AY12	
4	IO_L30N_4	AN13	
4	IO_L30P_4	AM13	
4	IO_L34N_4	AU13	
4	IO_L34P_4	AT13	
4	IO_L35N_4	BA13	
4	IO_L35P_4	AY13	
4	IO_L36N_4	AM14	
4	IO_L36P_4/VREF_4	AL14	
4	IO_L76N_4	AR15	
4	IO_L76P_4	AT14	
4	IO_L77N_4	AV14	
4	IO_L77P_4	AU14	
4	IO_L78N_4	AP14	
4	IO_L78P_4	AN14	
4	IO_L79N_4	AW15	
4	IO_L79P_4	AY14	
4	IO_L80_4/No_Pair	BB14	
4	IO_L83_4/No_Pair	BA14	
4	IO_L84N_4	AM15	
4	IO_L84P_4	AL15	
4	IO_L85N_4	AT16	
4	IO_L85P_4	AT15	
4	IO_L86N_4	AV15	
4	IO_L86P_4	AU15	
4	IO_L87N_4	AP15	
4	IO_L87P_4/VREF_4	AN15	
4	IO_L37N_4	AY16	
4	IO_L37P_4	AY15	
4	IO_L38N_4	BB15	
4	IO_L38P_4	BA15	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L15P_6	AP39	
6	IO_L15N_6/VREF_6	AP40	
6	IO_L16P_6	AP36	
6	IO_L16N_6	AP37	
6	IO_L17P_6	AH31	
6	IO_L17N_6	AG31	
6	IO_L18P_6	AN41	
6	IO_L18N_6	AN42	
6	IO_L19P_6	AN40	
6	IO_L19N_6	AM40	
6	IO_L20P_6	AG34	
6	IO_L20N_6	AG35	
6	IO_L21P_6	AN37	
6	IO_L21N_6/VREF_6	AN38	
6	IO_L22P_6	AN36	
6	IO_L22N_6	AM36	
6	IO_L23P_6	AG32	
6	IO_L23N_6	AG33	
6	IO_L24P_6	AM41	
6	IO_L24N_6	AM42	
6	IO_L25P_6	AM38	
6	IO_L25N_6	AM39	
6	IO_L26P_6	AF35	
6	IO_L26N_6	AF36	
6	IO_L27P_6	AM37	
6	IO_L27N_6/VREF_6	AL36	
6	IO_L28P_6	AL41	
6	IO_L28N_6	AK41	
6	IO_L29P_6	AF32	
6	IO_L29N_6	AF33	
6	IO_L30P_6	AL39	
6	IO_L30N_6	AL40	
6	IO_L31P_6	AL37	
6	IO_L31N_6	AL38	
6	IO_L32P_6	AF31	
6	IO_L32N_6	AE31	
6	IO_L33P_6	AK39	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L33N_6/VREF_6	AK40	
6	IO_L34P_6	AK36	
6	IO_L34N_6	AK37	
6	IO_L35P_6	AE36	
6	IO_L35N_6	AE37	
6	IO_L36P_6	AJ41	
6	IO_L36N_6	AJ42	
6	IO_L37P_6	AJ40	
6	IO_L37N_6	AH40	
6	IO_L38P_6	AE34	
6	IO_L38N_6	AE35	
6	IO_L39P_6	AJ38	
6	IO_L39N_6/VREF_6	AH37	
6	IO_L40P_6	AJ36	
6	IO_L40N_6	AJ37	
6	IO_L41P_6	AE32	
6	IO_L41N_6	AE33	
6	IO_L42P_6	AH41	
6	IO_L42N_6	AH42	
6	IO_L43P_6	AH38	
6	IO_L43N_6	AH39	
6	IO_L44P_6	AD36	
6	IO_L44N_6	AC35	
6	IO_L45P_6	AH36	
6	IO_L45N_6/VREF_6	AG36	
6	IO_L46P_6	AG41	
6	IO_L46N_6	AG42	
6	IO_L47P_6	AD34	
6	IO_L47N_6	AC33	
6	IO_L48P_6	AG40	
6	IO_L48N_6	AF39	
6	IO_L49P_6	AG38	
6	IO_L49N_6	AG39	
6	IO_L50P_6	AD32	
6	IO_L50N_6	AD33	
6	IO_L51P_6	AG37	
6	IO_L51N_6/VREF_6	AF37	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L26P_7	V31	
7	IO_L26N_7	U31	
7	IO_L25P_7	L41	
7	IO_L25N_7	L42	
7	IO_L24P_7	K40	
7	IO_L24N_7	L40	
7	IO_L23P_7	T34	
7	IO_L23N_7	T35	
7	IO_L22P_7	L38	
7	IO_L22N_7/VREF_7	L39	
7	IO_L21P_7	K36	
7	IO_L21N_7	L36	
7	IO_L20P_7	T32	
7	IO_L20N_7	T33	
7	IO_L19P_7	K41	
7	IO_L19N_7	K42	
7	IO_L18P_7	K37	
7	IO_L18N_7	K38	
7	IO_L17P_7	R34	
7	IO_L17N_7	R35	
7	IO_L16P_7	H42	
7	IO_L16N_7/VREF_7	J41	
7	IO_L15P_7	J39	
7	IO_L15N_7	J40	
7	IO_L14P_7	R32	
7	IO_L14N_7	R33	
7	IO_L13P_7	J36	
7	IO_L13N_7	J37	
7	IO_L12P_7	H40	
7	IO_L12N_7	H41	
7	IO_L11P_7	T31	
7	IO_L11N_7	R31	
7	IO_L10P_7	H38	
7	IO_L10N_7/VREF_7	H39	
7	IO_L09P_7	H36	
7	IO_L09N_7	H37	
7	IO_L08P_7	P34	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L79P_7	D41	
7	IO_L79N_7	D42	
7	IO_L78P_7	C39	
7	IO_L78N_7	C40	
7	IO_L77P_7	H34	
7	IO_L77N_7	H35	
7	IO_L76P_7	C37	
7	IO_L76N_7/VREF_7	D36	
7	IO_L75P_7	B38	
7	IO_L75N_7	C38	
7	IO_L74P_7	F34	
7	IO_L74N_7	G34	
7	IO_L73P_7	C35	
7	IO_L73N_7	C36	
7	IO_L06P_7	A39	
7	IO_L06N_7	B39	
7	IO_L05P_7	D34	
7	IO_L05N_7	D35	
7	IO_L04P_7	A37	
7	IO_L04N_7/VREF_7	B37	
7	IO_L03P_7	A36	
7	IO_L03N_7	B36	
7	IO_L02P_7	B34	
7	IO_L02N_7	C34	
7	IO_L01P_7/VRN_7	A35	
7	IO_L01N_7/VRP_7	B35	
7	VCCO_7	W39	
7	VCCO_7	P39	
7	VCCO_7	K39	
7	VCCO_7	F39	
7	VCCO_7	D37	
7	VCCO_7	W35	
7	VCCO_7	P35	
7	VCCO_7	K35	
7	VCCO_7	M33	
7	VCCO_7	H33	