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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8272
Number of Logic Elements/Cells	74448
Total RAM Bits	6045696
Number of I/O	964
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp70-6ffg1517c

Functional Description: Processor Block

This section briefly describes the interfaces and components of the Processor Block. The subsequent section, Functional Description: Embedded PowerPC 405 Core beginning on page 20, offers a summary of major PPC405 core features. For an in-depth discussion on both the Processor Block and PPC405, see tthe **PowerPC Processor Reference Guide** and the **PowerPC 405 Processor Block Reference Guide** available on the Xilinx website at **http://www.xilinx.com**.

Processor Block Overview

Figure 14 shows the internal architecture of the Processor Block.

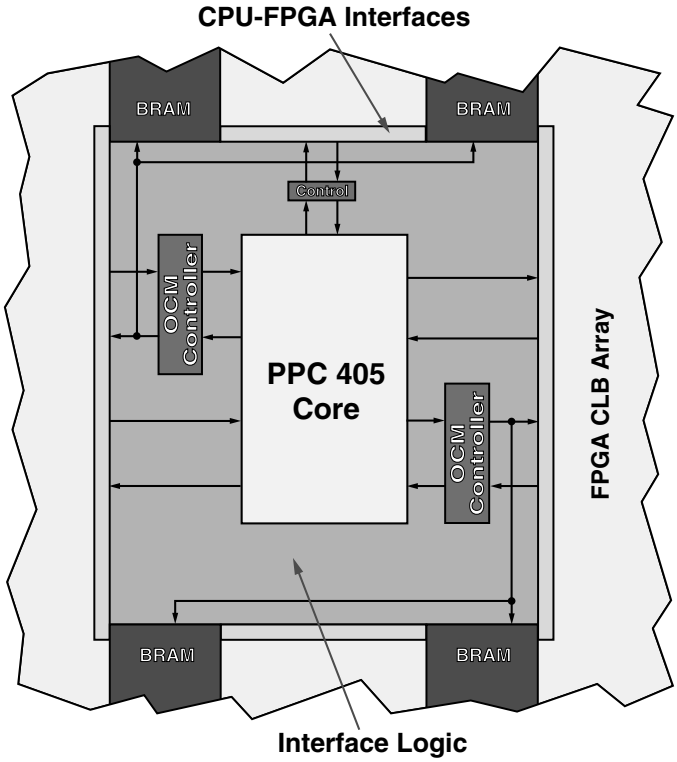

Figure 14: **Processor Block Architecture**

Within the Virtex-II Pro Processor Block, there are four components:

- Embedded IBM PowerPC 405-D5 RISC CPU core
- On-Chip Memory (OCM) controllers and interfaces
- Clock/control interface logic
- CPU-FPGA Interfaces

Embedded PowerPC 405 RISC Core

The PowerPC 405D5 core is a 0.13 µm implementation of the IBM PowerPC 405D4 core. The advanced process technology enables the embedded PowerPC 405 (PPC405) core to operate at 300+ MHz while maintaining low power consumption. Specially designed interface logic integrates the core with the surrounding CLBs, block RAMs, and general routing resources. Up to four Processor Blocks can be available in a single Virtex-II Pro device.

The embedded PPC405 core implements the PowerPC User Instruction Set Architecture (UISA), user-level registers, programming model, data types, and addressing modes for 32-bit fixed-point operations. 64-bit operations, auxiliary processor operations, and floating-point operations are trapped and can be emulated in software.

Most of the PPC405 core features are compatible with the specifications for the PowerPC Virtual Environment Architecture (VEA) and Operating Environment Architecture (OEA). They also provide a number of optimizations and extensions to the lower layers of the PowerPC Architecture. The full architecture of the PPC405 is defined by the PowerPC Embedded Environment and PowerPC UISA documentation, available from IBM.

On-Chip Memory (OCM) Controllers

Introduction

The OCM controllers serve as dedicated interfaces between the block RAMs in the FPGA fabric (see 18 Kb Block SelectRAM+ Resources, page 44) and OCM signals available on the embedded PPC405 core. The OCM signals on the PPC405 core are designed to provide very quick access to a fixed amount of instruction and data memory space. The OCM controller provides an interface to both the 64-bit Instruction-Side Block RAM (ISBRAM) and the 32-bit Data-Side Block RAM (DSBRAM). The designer can choose to implement:

- ISBRAM only
- DSBRAM only
- Both ISBRAM and DSBRAM
- No ISBRAM and no DSBRAM

One of OCM's primary advantages is that it guarantees a fixed latency of execution for a higher level of determinism. Additionally, it reduces cache pollution and thrashing, since the cache remains available for caching code from other memory resources.

Typical applications for DSOCM include scratch-pad memory, as well as use of the dual-port feature of block RAM to enable bidirectional data transfer between processor and FPGA. Typical applications for ISOCM include storage of interrupt service routines.

Functional Features

Common Features

- Separate Instruction and Data memory interface between processor core and BRAMs in FPGA
- Dedicated interface to Device Control Register (DCR) bus for ISOCM and DSOCM

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in Figure 39. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous; however, the storage element or flip-flop is available to implement a synchronous read. Any of the 16 bits can be read out asynchronously by varying the address. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

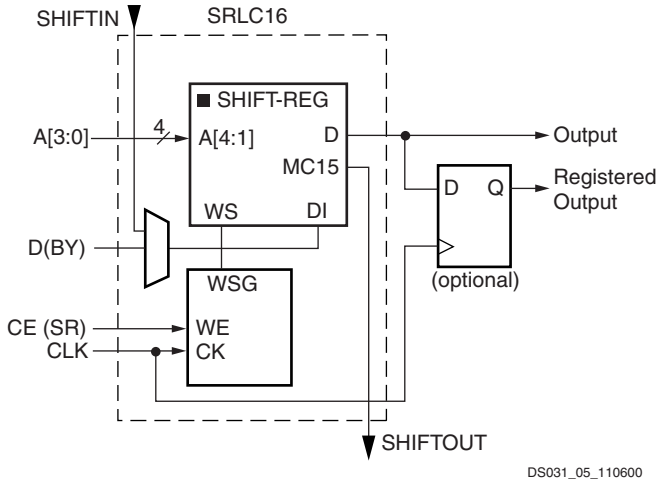

Figure 39: **Shift Register Configurations**

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See Figure 40.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

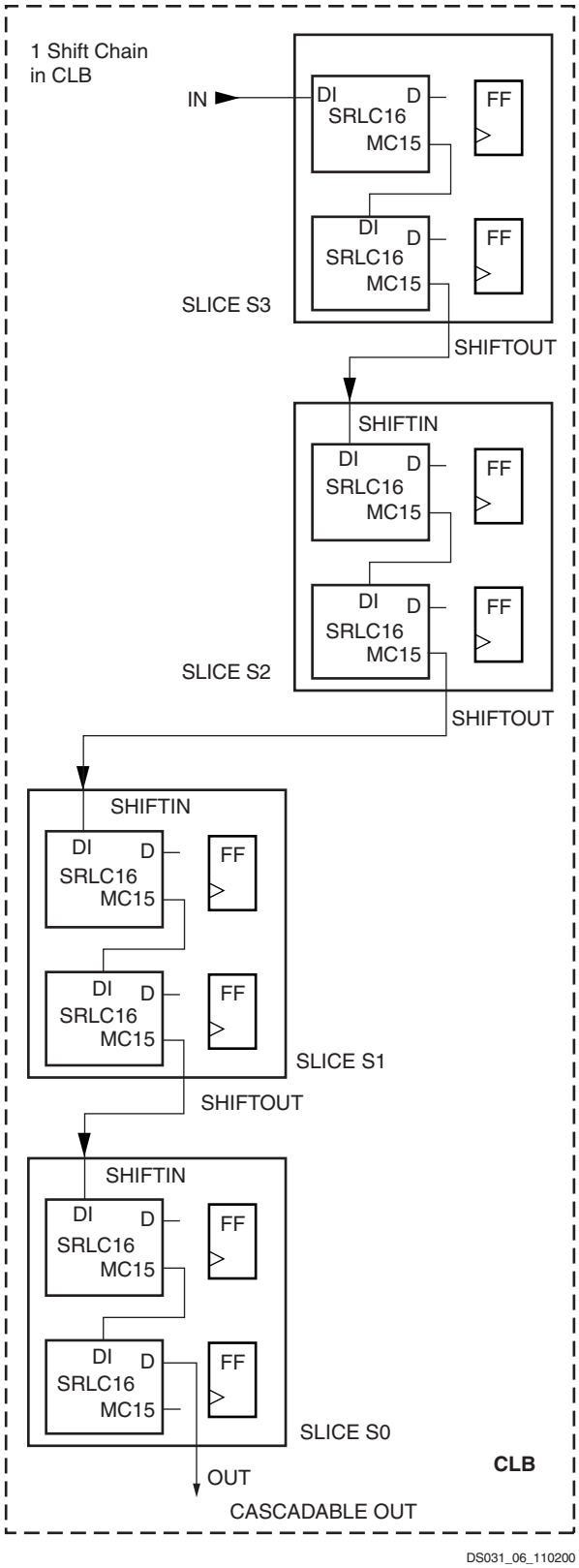

Figure 40: **Cascadable Shift Register**

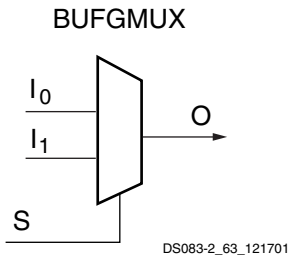

Figure 60: **Virtex-II Pro BUFGMUX Function**

If the presently selected clock is Low while S changes, or if it goes Low after S has changed, the output is kept Low until the other ("to-be-selected") clock has made a transition from High to Low. At that instant, the new clock starts driving the output.

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

All Virtex-II Pro devices have 16 global clock multiplexer buffers.

Figure 61 shows a switchover from I0 to I1.

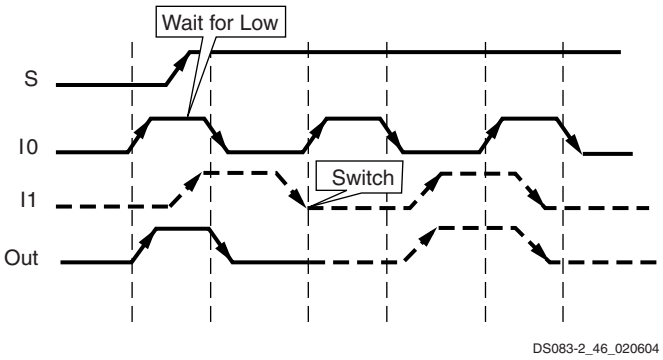

Figure 61: **Clock Multiplexer Waveform Diagram**

- The current clock is CLK0.
- S is activated High.
- If CLK0 is currently High, the multiplexer waits for CLK0 to go Low.
- Once CLK0 is Low, the multiplexer output stays Low until CLK1 transitions High to Low.
- When CLK1 transitions from High to Low, the output switches to CLK1.
- No glitches or short pulses can appear on the output.

Local Clocking

In addition to global clocks, there are local clock resources in the Virtex-II Pro devices. There are more than 72 local clocks in the Virtex-II Pro family. These resources can be used for many different applications, including but not limited to memory interfaces. For example, even using only the left and right I/O banks, Virtex-II Pro FPGAs can support up to 50 local clocks for DDR SDRAM. These interfaces can operate beyond 200 MHz on Virtex-II Pro devices.

Digital Clock Manager (DCM)

The Virtex-II Pro DCM offers a wide range of powerful clock management features.

- **Clock De-skew**: The DCM generates new system clocks (either internally or externally to the FPGA), which are phase-aligned to the input clock, thus eliminating clock distribution delays.
- **Frequency Synthesis**: The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- **Phase Shifting**: The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.

The DCM utilizes fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also utilizes fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four of the nine DCM clock outputs can drive inputs to global clock buffers or global clock multiplexer buffers simultaneously (see Figure 62). All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers.

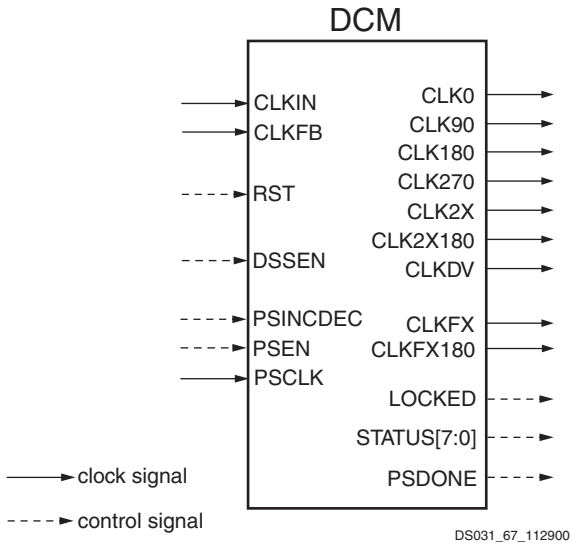

Figure 62: **Digital Clock Manager**

The DCM can be configured to delay the completion of the Virtex-II Pro configuration process until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

Virtex-II Pro Switching Characteristics

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Note that Virtex-II Pro Performance Characteristics are subject to these guidelines, as well. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 15 correlates the current status of each Virtex-II Pro device with a corresponding speed file designation.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Table 15: **Virtex-II Pro Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC2VP2			-7, -6, -5
XC2VP4			-7, -6, -5
XC2VP7			-7, -6, -5
XC2VP20			-7, -6, -5
XC2VPX20		-6, -5	
XC2VP30			-7, -6, -5
XC2VP40			-7, -6, -5
XC2VP50			-7, -6, -5
XC2VP70			-7, -6, -5
XC2VPX70		-6, -5	
XC2VP100			-6, -5

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II Pro devices.

PowerPC Switching Characteristics

Table 16: **Processor Clocks Absolute AC Characteristics**

Description	Speed Grade						Units
	-7		-6		-5		
	Min	Max	Min	Max	Min	Max	
CPMC405CLOCK frequency	0	400(1)	0	350(1)	0	300	MHz
JTAGC405TCK frequency(2)	0	200	0	175	0	150	MHz
PLBCLK(3)	0	400	0	350	0	300	MHz
BRAMDSOCMCLK(3)	0	400	0	350	0	300	MHz
BRAMISOCMCLK(3)	0	400	0	350	0	300	MHz

Notes:

1. **IMPORTANT!** When CPMC405CLOCK runs at speeds greater than 350 MHz in -7 Commercial grade dual-processor devices, or greater than 300 MHz in -6 Industrial grade dual-processor devices, users must implement the technology presented in **XAPP755**, "PowerPC 405 Clock Macro for -7(C) and -6(I) Speed Grade Dual-Processor Devices." Refer to Table 1, Module 1 to identify dual-processor devices.
2. The theoretical maximum frequency of this clock is one-half the CPMC405CLOCK. However, the achievable maximum is dependent on the system, and will be much less.
3. The theoretical maximum frequency of these clocks is equal to the CPMC405CLOCK. However, the achievable maximum is dependent on the system. Please see ***PowerPC 405 Processor Block Reference Guide*** and **XAPP640** for more information.

Date	Version	Revision
12/03/02	2.5	Updated parametric information in: • Table 1: Correct lower limit of voltage range of V_{IN} and V_{TS} from –0.5V to –0.3V for 3.3V. • Table 2: Add footnote (2) regarding V_{CCAUX} voltage droop. Renumbered other notes. • Table 12: Add waveform diagrams (Figure 1 and Figure 2) illustrating DV_{OUT} (single-ended) and DV_{PPOUT} (differential). • Table 23: Indicate REFCLK upper frequency limitation; relate REFCLK parameters to REFCLK2, BREFCLK, and BREFCLK2; correct T_{RCLK} and T_{FCLK} values and unit of measurement. • Table 60: Add qualifying footnote to CLKOUT_DUTY_CYCLE_DLL.
01/20/03	2.6	Updated parametric information in: • Table 12: Correct DV_{IN} Min (200 mV to 175 mV) and DV_{IN} Max (1000 mV to 2000 mV). • Table 23: Correct T_{RCLK} /T_{FCLK} Typ (400 ps to 600 ps) and Max (600 ps to 1000 ps). Add footnote (2) to qualify Max T_{GJTT} parameter. • Table 59: Correct hyperlink in footnote (1) to point directly to Answer Record 13645. • Move clock parameters from Table 18, Table 19, Table 20, and Table 21 to Table 16.
03/24/03	2.7	• Added/updated timing parameters from speedsfile **v1.76**. • Table 2: Delete first table footnote and renumber all others. • Table 3: Add "sample-tested" to I_L. Remove "Device" column, unnecessary. • Table 8: Update V_{OCM} (Typ) to 1.250V. • Table 10: Update LVPECL_25 DC parameters. • Table 23: Update F_{GCLK} frequency ranges. Break out T_{GJTT} by operating speed. • Table 27: Update F_{GTX} frequency ranges. Correct T_{DJ} to 0.17 UI, T_{RJ} to o.18 UI. • Table 39: Update V_{REF} (Typ) for HSTL Class I/II from 1.08V to 0.90V. • Table 43, Table 44: Correct parameter name "CE input (WS)" to "SR input". • Table 64: Break out T_{DCD_CLK0} by device type.
05/27/03	2.8	• Updated time and frequency parameters as per speedsfile **v1.78**. • Table 3: Added values for I_{REF}, I_L, I_{RPU}, I_{RPD} • Corrected I_{CCINTQ} (Table 4) and $I_{CCINTMIN}$ (Table 5) for XC2VP20 to 600 mA. • Table 4: Updated/Added Typ and Max quiescent current values for XC2VP7 and XC2VP20. Added footnote specifying parameters are for Commercial Grade parts. • Table 5: Added footnote specifying parameters are for Commercial Grade parts. • Table 6: Corrected V_{IH} (Max) for LVTTL and LVCMOS33 standards from 3.6V to 3.45V. Changed V_{IL} (Min) for all standards to –0.2V. Corrected V_{IL} (Max) for LVCMOS15 and LVCMOS18 from 20% V_{CCO} to 30% V_{CCO}. • Table 10: Corrected LVPECL_25 Min and Max values for V_{IH} and V_{IL}. Added explanatory text above table. • Table 13 and Table 14 (pin-pin and reg-reg performance): Changed device specified from XC2VP7FF672-6 to XC2VP20FF1152-6. • Table 15: Updated to show devices XC2VP7 and XC2VP20 as Preliminary for the -6 speed grade and Production for the -5 speed grade. • Removed former Table 32, Standard Capacitive Loads. • Table 52: Updated T_{TAPTCK} from 4.0 ns to 5.5 ns. • Table 59: Modified footnote referenced at CLKFX/CLKFX180 to point to the online Jitter Calculator. • Added Figure 6 and accompanying procedure for measuring standard adjustments.
05/27/03 (cont'd)	2.8 (cont'd)	• Table 1: Footnote (2) rewritten to specify “one or more banks.” • Table 57: Some DCM parameters were erroneously missing from v2.8 (single-module version) due to a document compilation error. The concatenated full data sheet version was not affected. These parameters have been restored.

Table 3: **Virtex-II Pro Available I/Os and RocketIO MGT Pins per Device/Package Combination**

Virtex-II Pro Device	User I/Os & RocketIO MGT Pins	Virtex-II Pro Package[1]									
		FG256/ FGG256	FG456/ FGG456	FG676/ FGG456	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
XC2VP2	Available User I/Os	140	156	-	204	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	76	-	100	-	-	-	-	-	-
XC2VP4	Available User I/Os	140	248	-	348	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	122	-	172	-	-	-	-	-	-
XC2VP7	Available User I/Os	-	248	-	396	396	-	-	-	-	-
	RocketIO MGT Pins	-	72	-	72	72	-	-	-	-	-
	Differential I/O Pairs	-	122	-	196	196	-	-	-	-	-
XC2VP20	Available User I/Os	-	-	404	-	556	564	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	196	-	272	276	-	-	-	-
XC2VPX20	**Available User I/Os**	**-**	**-**	**-**	**-**	**552**	**-**	**-**	**-**	**-**	**-**
	RocketIO X MGT Pins	**-**	**-**	**-**	**-**	**72**	**-**	**-**	**-**	**-**	**-**
	Differential I/O Pairs	**-**	**-**	**-**	**-**	**270**	**-**	**-**	**-**	**-**	**-**
XC2VP30	Available User I/Os	-	-	416	-	556	644	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	202	-	272	316	-	-	-	-
XC2VP40	Available User I/Os	-	-	416	-	-	692	804	-	-	-
	RocketIO MGT Pins	-	-	72	-	-	108	0	-	-	-
	Differential I/O Pairs	-	-	202	-	-	340	396	-	-	-
XC2VP50	Available User I/Os	-	-		-	-	692	812	852	-	-
	RocketIO MGT Pins	-	-		-	-	144	0	144	-	-
	Differential I/O Pairs	-	-		-	-	340	400	420	-	-

Virtex-II Pro Pin Definitions

This section describes the pinouts for Virtex-II Pro devices in the following packages:

- FG256/FGG256, FG456/FGG456, and FG676/FGG676: wire-bond fine-pitch BGA of 1.00 mm pitch
- FF672, FF896, FF1148, FF1152, FF1517, FF1696, and FF1704: flip-chip fine-pitch BGA of 1.00 mm pitch

All of the devices supported in a particular package are pin-out-compatible and are listed in the same table (one table per package). Pins that are not available for smaller devices are listed in right-hand columns.

Each device is split into eight I/O banks to allow for flexibility in the choice of I/O standards. Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. Table 4 provides definitions for all pin types.

All Virtex-II Pro pinout tables are available on the distribution CD-ROM, or on the web (at http://www.xilinx.com).

Pin Definitions

Table 4 provides a description of each pin type listed in Virtex-II Pro pinout tables.

Table 4: **Virtex-II Pro Pin Definitions**

Pin Name	Direction	Description
User I/O Pins:		
IO_LXXY_#	Input/Output/ Bidirectional	All user I/O pins are capable of differential signalling and can implement LVDS, ULVDS, BLVDS, LVPECL, or LDT pairs. Each user I/O is labeled "**IO_LXXY_#**", where: **IO** indicates a user I/O pin. **LXXY** indicates a differential pair, with **XX** a unique pair in the bank and **Y = P/N** for the positive and negative sides of the differential pair. **#** indicates the bank number (0 through 7)
Dual-Function Pins:		
IO_LXXY_#/ZZZ	The *dual-function pins* are labelled "**IO_LXXY_#/ZZZ**", where "**ZZZ**" can be one of the following pins: Per Bank - **VRP, VRN,** or **VREF** Globally - **GCLKX(S/P), BUSY/DOUT, INIT_B, D0/DIN – D7, RDWR_B,** or **CS_B** These dual functions are defined in the following section:	
"ZZZ" (Dual Function) Definitions:		
D0/DIN, D1, D2, D3, D4, D5, D6, D7	Input/Output	• *In SelectMAP mode,* D0 through D7 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. • *In bit-serial modes,* DIN (D0) is the single-data input. This pin becomes a user I/O after configuration.
CS_B	Input	In SelectMAP mode, this is the active-low Chip Select signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
RDWR_B	Input	In SelectMAP mode, this is the active-low Write Enable signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
BUSY/DOUT	Output	• *In SelectMAP mode,* BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained. • *In bit-serial modes,* DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. The pin becomes a user I/O after configuration.

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
4	IO_L69P_4/VREF_4	AA12			
4	IO_L74N_4/GCLK3S	U12			
4	IO_L74P_4/GCLK2P	V12			
4	IO_L75N_4/GCLK1S	W12			
4	IO_L75P_4/GCLK0P	Y12			
5	IO_L75N_5/GCLK7S	Y11			
5	IO_L75P_5/GCLK6P	W11			
5	IO_L74N_5/GCLK5S	V11			
5	IO_L74P_5/GCLK4P	U11			
5	IO_L69N_5/VREF_5	AA11			
5	IO_L69P_5	Y10			
5	IO_L67N_5	V10			
5	IO_L67P_5	U10			
5	IO_L09N_5/VREF_5	W10			
5	IO_L09P_5	W9			
5	IO_L07N_5/VREF_5	V9			
5	IO_L07P_5	U9			
5	IO_L06N_5/VRP_5	Y8			
5	IO_L06P_5/VRN_5	W8			
5	IO_L05_5/No_Pair	V8			
5	IO_L03N_5/D4	Y7			
5	IO_L03P_5/D5	W7			
5	IO_L02N_5/D6	V7			
5	IO_L02P_5/D7	V6			
5	IO_L01N_5/RDWR_B	W6			
5	IO_L01P_5/CS_B	W5			
6	IO_L01P_6/VRN_6	AB2			
6	IO_L01N_6/VRP_6	AA1			
6	IO_L02P_6	Y2			
6	IO_L02N_6	Y1			
6	IO_L03P_6	W2			
6	IO_L03N_6/VREF_6	W1			
6	IO_L05P_6	V4			
6	IO_L05N_6	V3			
6	IO_L06P_6	V2			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
4	IO_L54N_4	V15			
4	IO_L54P_4	W15			
4	IO_L55N_4	Y15			
4	IO_L55P_4	AA15			
4	IO_L57N_4	AB15			
4	IO_L57P_4/VREF_4	AA14			
4	IO_L67N_4	AC15			
4	IO_L67P_4	AD15			
4	IO_L69N_4	V14			
4	IO_L69P_4/VREF_4	W14			
4	IO_L74N_4/GCLK3S	AB14			
4	IO_L74P_4/GCLK2P	AC14			
4	IO_L75N_4/GCLK1S	AD14			
4	IO_L75P_4/GCLK0P	AE14			
5	IO_L75N_5/GCLK7S	AE13			
5	IO_L75P_5/GCLK6P	AD13			
5	IO_L74N_5/GCLK5S	AC13			
5	IO_L74P_5/GCLK4P	AB13			
5	IO_L69N_5/VREF_5	W13			
5	IO_L69P_5	V13			
5	IO_L67N_5	AD12			
5	IO_L67P_5	AC12			
5	IO_L57N_5/VREF_5	AA13			
5	IO_L57P_5	AB12			
5	IO_L55N_5	AA12			
5	IO_L55P_5	Y12			
5	IO_L54N_5	W12			
5	IO_L54P_5	V12			
5	IO_L53_5/No_Pair	AA11			
5	IO_L50_5/No_Pair	Y11			
5	IO_L49N_5	AD10			
5	IO_L49P_5	AC10			
5	IO_L48N_5	AB11			
5	IO_L48P_5	AB10			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	AVCCAUXRX19	AE15			
N/A	VTRXPAD19	AE16			
N/A	RXNPAD19	AF15			
N/A	RXPPAD19	AF16			
N/A	GNDA19	AD16			
N/A	TXPPAD19	AF17			
N/A	TXNPAD19	AF18			
N/A	VTTXPAD19	AE18			
N/A	AVCCAUXTX19	AE17			
N/A	AVCCAUXRX21	AE20	NC	NC	
N/A	VTRXPAD21	AE21	NC	NC	
N/A	RXNPAD21	AF20	NC	NC	
N/A	RXPPAD21	AF21	NC	NC	
N/A	GNDA21	AD22	NC	NC	
N/A	TXPPAD21	AF22	NC	NC	
N/A	TXNPAD21	AF23	NC	NC	
N/A	VTTXPAD21	AE23	NC	NC	
N/A	AVCCAUXTX21	AE22	NC	NC	
N/A	VCCINT	H8			
N/A	VCCINT	J9			
N/A	VCCINT	K9			
N/A	VCCINT	U9			
N/A	VCCINT	V9			
N/A	VCCINT	W8			
N/A	VCCINT	H19			
N/A	VCCINT	J10			
N/A	VCCINT	J17			
N/A	VCCINT	J18			
N/A	VCCINT	K11			
N/A	VCCINT	K16			
N/A	VCCINT	K18			
N/A	VCCINT	L10			
N/A	VCCINT	L17			
N/A	VCCINT	T10			
N/A	VCCINT	T17			
N/A	VCCINT	U11			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
7	IO_L54N_7		L26			
7	IO_L53P_7		N26			
7	IO_L53N_7		N25			
7	IO_L52P_7		M30			
7	IO_L52N_7/VREF_7		L30			
7	IO_L51P_7		K28			
7	IO_L51N_7		K27			
7	IO_L50P_7		N24			
7	IO_L50N_7		N23			
7	IO_L49P_7		L29			
7	IO_L49N_7		K29			
7	IO_L48P_7		J28			
7	IO_L48N_7		J27			
7	IO_L47P_7		M26			
7	IO_L47N_7		M25			
7	IO_L46P_7		K30			
7	IO_L46N_7/VREF_7		J30			
7	IO_L45P_7		K26			
7	IO_L45N_7		K25			
7	IO_L44P_7		M24			
7	IO_L44N_7		M23			
7	IO_L43P_7		J29			
7	IO_L43N_7		H29			
7	IO_L42P_7		H28	NC		
7	IO_L42N_7		H27	NC		
7	IO_L41P_7		L24	NC		
7	IO_L41N_7		L23	NC		
7	IO_L40P_7		G30	NC		
7	IO_L40N_7/VREF_7		G29	NC		
7	IO_L39P_7		G28	NC		
7	IO_L39N_7		G27	NC		
7	IO_L38P_7		J26	NC		
7	IO_L38N_7		J25	NC		
7	IO_L37P_7		F30	NC		
7	IO_L37N_7		F29	NC		
7	IO_L36P_7		F28	NC		

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
3	IO_L39P_3	AD4				
3	IO_L38N_3	AB9				
3	IO_L38P_3	AB10				
3	IO_L37N_3	AD5				
3	IO_L37P_3	AD6				
3	IO_L36N_3	AE2				
3	IO_L36P_3	AF2				
3	IO_L35N_3	AD7				
3	IO_L35P_3	AD8				
3	IO_L34N_3	AE4				
3	IO_L34P_3	AE5				
3	IO_L33N_3/VREF_3	AG1				
3	IO_L33P_3	AG2				
3	IO_L32N_3	AC9				
3	IO_L32P_3	AC10				
3	IO_L31N_3	AF3				
3	IO_L31P_3	AF4				
3	IO_L24N_3	AH1	NC			
3	IO_L24P_3	AH2	NC			
3	IO_L23N_3	AE7	NC			
3	IO_L23P_3	AE8	NC			
3	IO_L22N_3	AF5	NC			
3	IO_L22P_3	AF6	NC			
3	IO_L21N_3/VREF_3	AG3	NC			
3	IO_L21P_3	AG4	NC			
3	IO_L20N_3	AD9	NC			
3	IO_L20P_3	AD10	NC			
3	IO_L19N_3	AH3	NC			
3	IO_L19P_3	AH4	NC			
3	IO_L18N_3	AJ1	NC			
3	IO_L18P_3	AJ2	NC			
3	IO_L17N_3	AF7	NC			
3	IO_L17P_3	AF8	NC			
3	IO_L16N_3	AK1	NC			
3	IO_L16P_3	AK2	NC			
3	IO_L15N_3/VREF_3	AG5	NC			
3	IO_L15P_3	AG6	NC			
3	IO_L06N_3	AL1				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
7	IO_L18N_7	L25	NC			
7	IO_L17P_7	F34	NC			
7	IO_L17N_7	F33	NC			
7	IO_L16P_7	G30	NC			
7	IO_L16N_7/VREF_7	G29	NC			
7	IO_L15P_7	G32	NC			
7	IO_L15N_7	G31	NC			
7	IO_L06P_7	F31				
7	IO_L06N_7	F30				
7	IO_L05P_7	J28				
7	IO_L05N_7	J27				
7	IO_L04P_7	E34				
7	IO_L04N_7/VREF_7	E33				
7	IO_L03P_7	E32				
7	IO_L03N_7	E31				
7	IO_L02P_7	F28				
7	IO_L02N_7	F27				
7	IO_L01P_7/VRN_7	D34				
7	IO_L01N_7/VRP_7	D33				
0	VCCO_0	C29				
0	VCCO_0	E20				
0	VCCO_0	F25				
0	VCCO_0	L20				
0	VCCO_0	L21				
0	VCCO_0	L22				
0	VCCO_0	L23				
0	VCCO_0	M18				
0	VCCO_0	M19				
0	VCCO_0	M20				
0	VCCO_0	M21				
0	VCCO_0	M22				
1	VCCO_1	C6				
1	VCCO_1	E15				
1	VCCO_1	F10				
1	VCCO_1	L12				
1	VCCO_1	L13				
1	VCCO_1	L14				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
2	IO_L40P_2	K3		
2	IO_L41N_2	R9		
2	IO_L41P_2	P9		
2	IO_L42N_2	K1		
2	IO_L42P_2	K2		
2	IO_L43N_2	L5		
2	IO_L43P_2	L6		
2	IO_L44N_2	P7		
2	IO_L44P_2	P8		
2	IO_L45N_2	L1		
2	IO_L45P_2	L2		
2	IO_L46N_2/VREF_2	M5		
2	IO_L46P_2	M6		
2	IO_L47N_2	R10		
2	IO_L47P_2	R11		
2	IO_L48N_2	M3		
2	IO_L48P_2	M4		
2	IO_L49N_2	M1		
2	IO_L49P_2	M2		
2	IO_L50N_2	R7		
2	IO_L50P_2	T8		
2	IO_L51N_2	P4		
2	IO_L51P_2	N4		
2	IO_L52N_2/VREF_2	N2		
2	IO_L52P_2	N3		
2	IO_L53N_2	T10		
2	IO_L53P_2	T11		
2	IO_L54N_2	P5		
2	IO_L54P_2	P6		
2	IO_L55N_2	R3		
2	IO_L55P_2	P3		
2	IO_L56N_2	T6		
2	IO_L56P_2	T7		
2	IO_L57N_2	P1		
2	IO_L57P_2	P2		
2	IO_L58N_2/VREF_2	R5		
2	IO_L58P_2	R6		
2	IO_L59N_2	U10		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
6	IO_L87N_6/VREF_6	V33		
6	IO_L88P_6	V30		
6	IO_L88N_6	V31		
6	IO_L89P_6	V24		
6	IO_L89N_6	V25		
6	IO_L90P_6	V28		
6	IO_L90N_6	V29		
7	IO_L90P_7	U32		
7	IO_L90N_7	V32		
7	IO_L89P_7	U28		
7	IO_L89N_7	U29		
7	IO_L88P_7	U30		
7	IO_L88N_7/VREF_7	U31		
7	IO_L87P_7	T33		
7	IO_L87N_7	U33		
7	IO_L86P_7	U26		
7	IO_L86N_7	U27		
7	IO_L85P_7	T31		
7	IO_L85N_7	T32		
7	IO_L60P_7	R33		
7	IO_L60N_7	R34		
7	IO_L59P_7	U24		
7	IO_L59N_7	U25		
7	IO_L58P_7	R29		
7	IO_L58N_7/VREF_7	R30		
7	IO_L57P_7	P33		
7	IO_L57N_7	P34		
7	IO_L56P_7	T28		
7	IO_L56N_7	T29		
7	IO_L55P_7	P32		
7	IO_L55N_7	R32		
7	IO_L54P_7	P29		
7	IO_L54N_7	P30		
7	IO_L53P_7	T24		
7	IO_L53N_7	T25		
7	IO_L52P_7	N32		
7	IO_L52N_7/VREF_7	N33		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L11N_2	L9		
2	IO_L11P_2	M10		
2	IO_L12N_2	H4		
2	IO_L12P_2	J5		
2	IO_L13N_2	J1		
2	IO_L13P_2	J2		
2	IO_L14N_2	M8		
2	IO_L14P_2	N9		
2	IO_L15N_2	K6		
2	IO_L15P_2	K7		
2	IO_L16N_2/VREF_2	K4		
2	IO_L16P_2	K5		
2	IO_L17N_2	P10		
2	IO_L17P_2	N10		
2	IO_L18N_2	K3		
2	IO_L18P_2	J3		
2	IO_L19N_2	K1		
2	IO_L19P_2	K2		
2	IO_L20N_2	M11		
2	IO_L20P_2	N11		
2	IO_L21N_2	L7		
2	IO_L21P_2	L8		
2	IO_L22N_2/VREF_2	L5		
2	IO_L22P_2	L6		
2	IO_L23N_2	P8		
2	IO_L23P_2	P9		
2	IO_L24N_2	L3		
2	IO_L24P_2	L4		
2	IO_L25N_2	L1		
2	IO_L25P_2	L2		
2	IO_L26N_2	P11		
2	IO_L26P_2	P12		
2	IO_L27N_2	M6		
2	IO_L27P_2	M7		
2	IO_L28N_2/VREF_2	M2		
2	IO_L28P_2	M3		
2	IO_L29N_2	R9		
2	IO_L29P_2	R10		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
0	IO_L34N_0		E30		
0	IO_L34P_0		F30		
0	IO_L35N_0		D30		
0	IO_L35P_0		C30		
0	IO_L36N_0		M28		
0	IO_L36P_0/VREF_0		M29		
0	IO_L78N_0		K29	NC	
0	IO_L78P_0		L29	NC	
0	IO_L83_0/No_Pair		H29	NC	
0	IO_L84N_0		F29	NC	
0	IO_L84P_0		G29	NC	
0	IO_L85N_0		D29	NC	
0	IO_L85P_0		E29	NC	
0	IO_L86N_0		L28	NC	
0	IO_L86P_0		K28	NC	
0	IO_L87N_0		H28	NC	
0	IO_L87P_0/VREF_0		J28	NC	
0	IO_L37N_0		E28		
0	IO_L37P_0		F28		
0	IO_L38N_0		C29		
0	IO_L38P_0		C28		
0	IO_L39N_0		L27		
0	IO_L39P_0		M27		
0	IO_L43N_0		J27		
0	IO_L43P_0		K27		
0	IO_L44N_0		H27		
0	IO_L44P_0		G27		
0	IO_L45N_0		E27		
0	IO_L45P_0/VREF_0		F27		
0	IO_L46N_0		M25		
0	IO_L46P_0		M26		
0	IO_L47N_0		L26		
0	IO_L47P_0		K26		
0	IO_L48N_0		H26		
0	IO_L48P_0		J26		
0	IO_L49N_0		F26		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L08P_2		K5		
2	IO_L09N_2		K8		
2	IO_L09P_2		K7		
2	IO_L10N_2/VREF_2		K2		
2	IO_L10P_2		K1		
2	IO_L11N_2		L8		
2	IO_L11P_2		L9		
2	IO_L12N_2		L6		
2	IO_L12P_2		L7		
2	IO_L13N_2		K3		
2	IO_L13P_2		L3		
2	IO_L14N_2		L5		
2	IO_L14P_2		L4		
2	IO_L15N_2		L1		
2	IO_L15P_2		L2		
2	IO_L16N_2/VREF_2		M7		
2	IO_L16P_2		M8		
2	IO_L17N_2		M11		
2	IO_L17P_2		M12		
2	IO_L18N_2		M9		
2	IO_L18P_2		M10		
2	IO_L19N_2		M2		
2	IO_L19P_2		M3		
2	IO_L20N_2		M4		
2	IO_L20P_2		M5		
2	IO_L21N_2		N7		
2	IO_L21P_2		N8		
2	IO_L22N_2/VREF_2		N5		
2	IO_L22P_2		N6		
2	IO_L23N_2		N9		
2	IO_L23P_2		N10		
2	IO_L24N_2		N3		
2	IO_L24P_2		N4		
2	IO_L25N_2		N1		
2	IO_L25P_2		N2		
2	IO_L26N_2		N11		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		V6		
N/A	GND		U25		
N/A	GND		U24		
N/A	GND		U23		
N/A	GND		U22		
N/A	GND		U21		
N/A	GND		U20		
N/A	GND		U19		
N/A	GND		U18		
N/A	GND		T42		
N/A	GND		T1		
N/A	GND		R39		
N/A	GND		R36		
N/A	GND		R7		
N/A	GND		R4		
N/A	GND		M42		
N/A	GND		M1		
N/A	GND		L22		
N/A	GND		L21		
N/A	GND		K39		
N/A	GND		K4		
N/A	GND		J34		
N/A	GND		J9		
N/A	GND		H42		
N/A	GND		H35		
N/A	GND		H22		
N/A	GND		H21		
N/A	GND		H8		
N/A	GND		H1		
N/A	GND		G36		
N/A	GND		G7		
N/A	GND		F37		
N/A	GND		F25		
N/A	GND		F18		
N/A	GND		F6		
N/A	GND		E38		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD22	
N/A	GND	AC22	
N/A	GND	AB22	
N/A	GND	AA22	
N/A	GND	Y22	
N/A	GND	W22	
N/A	GND	V22	
N/A	GND	U22	
N/A	GND	AF21	
N/A	GND	AE21	
N/A	GND	AD21	
N/A	GND	AC21	
N/A	GND	AB21	
N/A	GND	AA21	
N/A	GND	Y21	
N/A	GND	W21	
N/A	GND	V21	
N/A	GND	U21	
N/A	GND	BB20	
N/A	GND	AV20	
N/A	GND	AP20	
N/A	GND	AF20	
N/A	GND	AE20	
N/A	GND	AD20	
N/A	GND	AC20	
N/A	GND	AB20	
N/A	GND	AA20	
N/A	GND	Y20	
N/A	GND	W20	
N/A	GND	V20	
N/A	GND	U20	
N/A	GND	J20	
N/A	GND	E20	
N/A	GND	A20	
N/A	GND	AL19	
N/A	GND	AF19	
N/A	GND	AE19	