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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	8272
Number of Logic Elements/Cells	74448
Total RAM Bits	6045696
Number of I/O	964
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp70-7ff1517c



Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview

DS083 (v5.0) June 21, 2011

Product Specification

Summary of Virtex-II Pro™ / Virtex-II Pro X Features

- High-Performance Platform FPGA Solution, Including
 - Up to twenty RocketIO™ or RocketIO X embedded Multi-Gigabit Transceivers (MGTS)
 - Up to two IBM PowerPC™ RISC processor blocks
 - Based on Virtex-II™ Platform FPGA Technology
 - Flexible logic resources
 - SRAM-based in-system configuration
 - Active Interconnect technology
 - SelectRAM™+ memory hierarchy
 - Dedicated 18-bit x 18-bit multiplier blocks
 - High-performance clock management circuitry
 - SelectIO™-Ultra technology
 - XCITE Digitally Controlled Impedance (DCI) I/O
- Virtex-II Pro / Virtex-II Pro X family members and resources are shown in [Table 1](#).

Table 1: Virtex-II Pro / Virtex-II Pro X FPGA Family Members

Device ⁽¹⁾	RocketIO Transceiver Blocks	PowerPC Processor Blocks	Logic Cells ⁽²⁾	CLB (1 = 4 slices = max 128 bits)		18 X 18 Bit Multiplier Blocks	Block SelectRAM+		DCMs	Maximum User I/O Pads
				Slices	Max Distr RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)		
XC2VP2	4	0	3,168	1,408	44	12	12	216	4	204
XC2VP4	4	1	6,768	3,008	94	28	28	504	4	348
XC2VP7	8	1	11,088	4,928	154	44	44	792	4	396
XC2VP20	8	2	20,880	9,280	290	88	88	1,584	8	564
XC2VPX20	8 ⁽⁴⁾	1	22,032	9,792	306	88	88	1,584	8	552
XC2VP30	8	2	30,816	13,696	428	136	136	2,448	8	644
XC2VP40	0 ⁽³⁾ , 8, or 12	2	43,632	19,392	606	192	192	3,456	8	804
XC2VP50	0 ⁽³⁾ or 16	2	53,136	23,616	738	232	232	4,176	8	852
XC2VP70	16 or 20	2	74,448	33,088	1,034	328	328	5,904	8	996
XC2VPX70	20 ⁽⁴⁾	2	74,448	33,088	1,034	308	308	5,544	8	992
XC2VP100	0 ⁽³⁾ or 20	2	99,216	44,096	1,378	444	444	7,992	12	1,164

Notes:

- 7 speed grade devices are not available in Industrial grade.
- Logic Cell $\approx$ (1) 4-input LUT + (1)FF + Carry Logic
- These devices can be ordered in a configuration without RocketIO transceivers. See [Table 3](#) for package configurations.
- Virtex-II Pro X devices equipped with RocketIO X transceiver cores.

RocketIO X Transceiver Features (XC2VPX20 and XC2VPX70 Only)

- Variable-Speed Full-Duplex Transceiver (XC2VPX20) Allowing 2.488 Gb/s to 6.25 Gb/s Baud Transfer Rates.
 - Includes specific baud rates used by various standards, as listed in [Table 4, Module 2](#).
- Fixed-Speed Full-Duplex Transceiver (XC2VPX70) Operating at 4.25 Gb/s Baud Transfer Rate.
- Eight or Twenty Transceiver Modules on an FPGA, Depending upon Device
- Monolithic Clock Synthesis and Clock Recovery
 - Eliminates the need for external components
- Automatic Lock-to-Reference Function
- Programmable Serial Output Differential Swing
 - 200 mV to 1600 mV, peak-peak
 - Allows compatibility with other serial system voltage levels
- Programmable Pre-emphasis Levels 0 to 500%
- Telecom/Datacom Support Modes
 - "x8" and "x10" clocking/data paths
 - 64B/66B clocking support

Each RocketIO or RocketIO X core implements the following technology:

- Serializer and deserializer (SERDES)
- Monolithic clock synthesis and clock recovery (CDR)
- 10 Gigabit Attachment Unit Interface (XAUI) Fibre Channel (3.1875 Gb/s XAUI), Infiniband, PCI Express, Aurora, SXI-5 (SFI-5,/SPI-5), and OC-48 compatibility⁽¹⁾
- 8/16/32-bit (RocketIO) or 8/16/32/64-bit (RocketIO X) selectable FPGA interface
- 8B/10B (RocketIO) or 8B/10B and 64B/66B (RocketIO X) encoder and decoder with bypassing option on each channel
- Channel bonding support (two to twenty channels)
 - Elastic buffers for inter-chip deskewing and channel-to-channel alignment
- Receiver clock recovery tolerance of up to 75 non-transitioning bits
- 50Ω (RocketIO X) or 50Ω / 75Ω selectable (RocketIO) on-chip transmit and receive terminations
- Programmable comma detection and word alignment
- Rate matching via insertion/deletion characters
- Automatic lock-to-reference function
- Programmable pre-emphasis support
- Per-channel serial and parallel transmitter-to-receiver internal loopback modes
- Optional transmit and receive data inversion
- Cyclic Redundancy Check support (RocketIO only)

PowerPC 405 Processor Block

The PPC405 RISC CPU can execute instructions at a sustained rate of one instruction per cycle. On-chip instruction and data cache reduce design complexity and improve system throughput.

The PPC405 features include:

- PowerPC RISC CPU
 - Implements the PowerPC User Instruction Set Architecture (UISA) and extensions for embedded applications
 - Thirty-two 32-bit general purpose registers (GPRs)
 - Static branch prediction
 - Five-stage pipeline with single-cycle execution of most instructions, including loads/stores
 - Unaligned and aligned load/store support to cache, main memory, and on-chip memory
 - Hardware multiply/divide for faster integer arithmetic (4-cycle multiply, 35-cycle divide)
 - Enhanced string and multiple-word handling
 - Big/little endian operation support
- Storage Control

- Separate instruction and data cache units, both two-way set-associative and non-blocking
- Eight words (32 bytes) per cache line
- 16 KB array Instruction Cache Unit (ICU), 16 KB array Data Cache Unit (DCU)
- Operand forwarding during instruction cache line fill
- Copy-back or write-through DCU strategy
- Doubleword instruction fetch from cache improves branch latency
- Virtual mode memory management unit (MMU)
 - Translation of the 4 GB logical address space into physical addresses
 - Software control of page replacement strategy
 - Supports multiple simultaneous page sizes ranging from 1 KB to 16 MB
- OCM controllers provide dedicated interfaces between Block SelectRAM+ memory and processor block instruction and data paths for high-speed access
- PowerPC timer facilities
 - 64-bit time base
 - Programmable interval timer (PIT)
 - Fixed interval timer (FIT)
 - Watchdog timer (WDT)
- Debug Support
 - Internal debug mode
 - External debug mode
 - Debug Wait mode
 - Real Time Trace debug mode
 - Enhanced debug support with logical operators
 - Instruction trace and trace-back support
 - Forward or backward trace
- Two hardware interrupt levels support
- Advanced power management support

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single data rate (SDR) or double data rate (DDR) register
- Output block with an optional SDR or DDR register and an optional 3-state buffer to be driven directly or through an SDR or DDR register
- Bidirectional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTTL, LVCMOS (3.3V,⁽²⁾ 2.5V, 1.8V, and 1.5V)
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V⁽³⁾
- PCI compliant (66 MHz and 33 MHz) at 3.3V⁽³⁾
- GTL and GTLP

1. Refer to [Table 4, Module 2](#) for detailed information about RocketIO and RocketIO X transceiver compatible protocols.

2. Refer to [XAPP659](#) for more information.

3. Refer to [XAPP653](#) for more information.

Table 5: Clock Ratios for Various Data Widths

Fabric Data Width	Frequency Ratio of USRCLK:USRCLK2
1-byte	1:2 ⁽¹⁾
2-byte	1:1
4-byte	2:1 ⁽¹⁾

Notes:

- Each edge of slower clock must align with falling edge of faster clock.

FPGA Transmit Interface

The FPGA can send either one, two, or four characters of data to the transmitter. Each character can be either 8 bits or 10 bits wide. If 8-bit data is applied, the additional inputs become control signals for the 8B/10B encoder. When the 8B/10B encoder is bypassed, the 10-bit character order is generated as follows:

TXCHARDISPMODE[0] (first bit transmitted)
TXCHARDISPVAL[0]
TXDATA[7:0] (last bit transmitted is TXDATA[0])

Disparity Control

The 8B/10B encoder is initialized with a negative running disparity. Unique control allows forcing the current running disparity state.

TXRUNDISP signals its current running disparity. This may be useful in those cases where there is a need to manipulate the initial running disparity value.

Bits TXCHARDISPMODE and TXCHARDISPVAL control the generation of running disparity before each byte.

For example, the transceiver can generate the sequence

K28.5+ K28.5+ K28.5- K28.5-
or

K28.5- K28.5- K28.5+ K28.5+

by specifying inverted running disparity for the second and fourth bytes.

Transmit FIFO

Proper operation of the circuit is only possible if the FPGA clock (TXUSRCLK) is frequency-locked to the reference clock (REFCLK). Phase variations up to one clock cycle are allowable. The FIFO has a depth of four. Overflow or underflow conditions are detected and signaled at the interface. Bypassing of this FIFO is programmable.

8B/10B Encoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

A bypassable 8B/10B encoder is included. The encoder uses the same 256 data characters and 12 control characters used by Gigabit Ethernet, Fibre Channel, and InfiniBand.

The encoder accepts 8 bits of data along with a K-character signal for a total of 9 bits per character applied, and generates a 10 bit character for transmission. If the K-character signal is High, the data is encoded into one of the twelve possible K-characters available in the 8B/10B code. If the K-character input is Low, the 8 bits are encoded as standard data. If the K-character input is High, and a user applies other than one of the twelve possible combinations, TXKERR indicates the error.

8B/10B Decoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

An optional 8B/10B decoder is included. A programmable option allows the decoder to be bypassed. When the 8B/10B decoder is bypassed, the 10-bit character order is, for example,

RXCHARISK[0] (first bit received)
RXRUNDISP[0]
RXDATA[7:0] (last bit received is RXDATA[0])

The decoder uses the same table that is used for Gigabit Ethernet, Fibre Channel, and InfiniBand. In addition to decoding all data and K-characters, the decoder has several extra features. The decoder separately detects both "disparity errors" and "out-of-band" errors. A disparity error is the reception of 10-bit character that exists within the 8B/10B table but has an incorrect disparity. An out-of-band error is the reception of a 10-bit character that does not exist within the 8B/10B table. It is possible to obtain an out-of-band error without having a disparity error. The proper disparity is always computed for both legal and illegal characters. The current running disparity is available at the RXRUNDISP signal.

The 8B/10B decoder performs a unique operation if out-of-band data is detected. If out-of-band data is detected, the decoder signals the error and passes the illegal 10-bits through and places them on the outputs. This can be used for debugging purposes if desired.

The decoder also signals the reception of one of the 12 valid K-characters. In addition, a programmable comma detect is included. The comma detect signal registers a comma on the receipt of any comma+, comma-, or both. Since the comma is defined as a 7-bit character, this includes several out-of-band characters. Another option allows the decoder to detect only the three defined commas (K28.1, K28.5, and K28.7) as comma+, comma-, or both. In total, there are six possible options, three for valid commas and three for "any comma."

Note that all bytes (1, 2, or 4) at the RX FPGA interface each have their own individual 8B/10B indicators (K-character, disparity error, out-of-band error, current running disparity, and comma detect).

Date	Version	Revision
03/24/03	2.5.1	Table 10: Corrected I/O standard names SSTL18_I and SSTL18_II to SSTL18_I_DCI and SSTL18_II_DCI respectively. Figure 61, text below: Corrected wording of criteria for clock switching.
05/27/03	2.6	- Removed Compatible Output Standards and Compatible Input Standards tables. - Added new Table 12, Summary of Voltage Supply Requirements for All Input and Output Standards. This table replaces deleted I/O standards tables. - Corrected sentence in section Input/Output Individual Options, page 27, to read "The optional weak-keeper circuit is connected to each <i>user I/O pad</i>." - Added section Rules for Combining I/O Standards in the Same Bank, page 29.
06/02/03	2.7	- Added four Differential Termination I/O standards to Table 9 and Table 12. - Added section On-Chip Differential Termination and Figure 31, page 34.
08/25/03	2.7.1	Added footnote referring to XAPP659 to 3.3V I/O callouts in Table 8 and Table 12.
09/10/03	2.8	Section Configuration, page 56: Added text indicating that the mode pins M0-M2 must be held to a constant DC level during and after configuration.
10/14/03	2.9	- Deleted section Functional Description: RocketIO Multi-Gigabit Transceiver (MGT), page 10. Added section Local Clocking, page 51. - Sections Slave-Serial Mode and Master-Serial Mode, page 56: Changed "rising" to "falling" edge with respect to DOUT. Table 8, page 24 and Table 10, page 25: Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V.
12/10/03	3.0	XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to Production status.
02/19/04	3.1	Section BUFGMUX, page 50: Corrected the definition of the "presently selected clock" to be I0 or I1. Corrected signal names in Figure 61 and associated text from CLK0 and CLK1 to I0 and I1.
03/09/04	3.1.1	Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
04/22/04	3.2	Section Clock De-skew, page 52: Removed reference to CLK2X as an option for DCM clock feedback.
06/30/04	4.0	Merged in DS110-2 (Module 2 of Virtex-II Pro X data sheet). Separate RocketIO and RocketIO X sections created.
11/17/04	4.1	Figure 11, page 12: Corrected figure by removing coupling capacitors from input. - Section Rules for Combining I/O Standards in the Same Bank, page 29: Corrected I/O standard in the first example from LVDS_25_DCI to LVDS_25.
03/01/05	4.2	- Reassigned heading hierarchies for better agreement with content. Table 7: Corrected VCCAUTX and VCCAUXRX to AVCCAUTX and AVCCAUXRX respectively. Table 9: Corrected V_{OD} (output voltage) range for LVDSEXT_25. Table 25: Corrected SelectRAM+ memory available for XC2VPX70 device. Table 33: Updated configuration default bitstream lengths.
06/20/05	4.3	<i>No changes in Module 2 for this revision.</i>
09/15/05	4.4	Table 1: Deleted SONET OC-192 protocol. Table 3: Deleted RocketIO X primitives for SONET OC-192, 10 Gbit Ethernet, and Xilinx 10G (Aurora) protocols. - Changed all instances of 10.3125 Gb/s to 6.25 Gb/s. Table 7: Changed RocketIO X VCCAUXRX from 1.5V globally to 1.5V for 8B/10B encoding, 1.8V for all other encoding protocols.

LVDS DC Specifications (LVDS_25)

Table 8: LVDS DC Specifications

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Output High Voltage for Q and $\bar{Q}$	V_{OH}	$R_T = 100\ \Omega$ across Q and $\bar{Q}$ signals			1.602	V
Output Low Voltage for Q and $\bar{Q}$	V_{OL}	$R_T = 100\ \Omega$ across Q and $\bar{Q}$ signals	0.898			V
Differential Output Voltage (Q – $\bar{Q}$), Q = High ($\bar{Q}$ – Q), $\bar{Q}$ = High	V_{ODIFF}	$R_T = 100\ \Omega$ across Q and $\bar{Q}$ signals	247	350	454	mV
Output Common-Mode Voltage	V_{OCM}	$R_T = 100\ \Omega$ across Q and $\bar{Q}$ signals	1.125	1.250	1.375	V
Differential Input Voltage (Q – $\bar{Q}$), Q = High ($\bar{Q}$ – Q), $\bar{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25V	100	350	600	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ± 350 mV	0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDS_EXT_25)

Table 9: Extended LVDS DC Specifications

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Output High Voltage for Q and $\bar{Q}$	V_{OH}	$R_T = 100\ \Omega$ across Q and $\bar{Q}$ signals			1.785	V
Output Low Voltage for Q and $\bar{Q}$	V_{OL}	$R_T = 100\ \Omega$ across Q and $\bar{Q}$ signals	0.715			V
Differential Output Voltage (Q – $\bar{Q}$), Q = High ($\bar{Q}$ – Q), $\bar{Q}$ = High	V_{ODIFF}	$R_T = 100\ \Omega$ across Q and $\bar{Q}$ signals	440		820	mV
Output Common-Mode Voltage	V_{OCM}	$R_T = 100\ \Omega$ across Q and $\bar{Q}$ signals	1.125	1.250	1.375	V
Differential Input Voltage (Q – $\bar{Q}$), Q = High ($\bar{Q}$ – Q), $\bar{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25V	100		1000	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ± 350 mV	0.3	1.2	2.2	V

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower

common-mode ranges. Table 10 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-II Pro Platform FPGA User Guide*.

Table 10: LVPECL DC Specifications

DC Parameter	$V_{CCO} = 2.375V$		$V_{CCO} = 2.5V$		$V_{CCO} = 2.625V$		Units
	Min	Max	Min	Max	Min	Max	
V_{OH}	1.35	1.495	1.475	1.62	1.6	1.745	V
V_{OL}	0.565	0.755	0.69	0.88	0.815	1.005	V
V_{IH}	0.8	2.0	0.8	2.0	0.8	2.0	V
V_{IL}	0.5	1.7	0.5	1.7	0.5	1.7	V
Differential Input Voltage	0.100	1.5	0.100	1.5	0.100	1.5	V

Table 24: RocketIO X Receiver Switching Characteristics⁽¹⁾

Description	Symbol	Conditions	Min	Typ	Max	Units
Receive total jitter tolerance using default equalization and PRBS-15 pattern	T_{JTOL}	2.488 Gb/s		0.80	0.65	UI ⁽²⁾
		3.125 Gb/s		0.80	0.65	UI
		4.25 Gb/s		0.80	0.65	UI
		6.25 Gb/s		0.80	0.65	UI
Receive random jitter tolerance	T_{RJTO}	2.488 Gb/s		0.30		UI
		3.125 Gb/s		0.30		UI
		4.25 Gb/s		0.30		UI
		6.25 Gb/s		0.30		UI
Receive sinusoidal jitter tolerance measured at 70 MHz	T_{SJTO}	2.488 Gb/s		0.30	0.15	UI
		3.125 Gb/s		0.30	0.15	UI
		4.25 Gb/s		0.30	0.15	UI
		6.25 Gb/s		0.30	0.15	UI
Receive deterministic jitter tolerance	T_{DJTO}	2.488 Gb/s		0.55	0.45	UI
		3.125 Gb/s		0.55	0.45	UI
		4.25 Gb/s		0.55	0.45	UI
		6.25 Gb/s		0.50	0.45	UI
Receive latency ⁽³⁾	T_{RXLAT}			25	34 ⁽⁴⁾	RXUSRCLK cycles
RXUSRCLK duty cycle	T_{RXDC}		45	50	55	%
RXUSRCLK2 duty cycle	T_{RX2DC}		45	50	55	%
Differential receive input sensitivity	V_{EYE}			120	250	mV

Notes:

1. The XC2VPX70 operates at a fixed 4.25 Gb/s baud rate.
2. UI = Unit Interval
3. Receive latency delay RXP/RXN to RXDATA. Refer to [RocketIO X Transceiver User Guide](#) for more information on calculating latency.
4. This maximum may occur when certain conditions are present and clock correction and channel bonding are enabled. If these functions are both disabled, the maximum will be near the typical values.

Table 25: RocketIO Receiver Switching Characteristics

Description	Symbol	Conditions	Min	Typ	Max	Units
Receive total jitter tolerance	T_{JTOL}	2.126 Gb/s – 3.125 Gb/s			0.65	UI ⁽¹⁾
		1.0626 Gb/s – 2.125 Gb/s			0.65	UI
		1.0 Gb/s – 1.0625 Gb/s			0.68	UI
		600 Mb/s – 999 Mb/s			0.68 ⁽²⁾	UI
Receive deterministic jitter tolerance	T_{DJTOL}	2.126 Gb/s – 3.125 Gb/s			0.41	UI
		1.0626 Gb/s – 2.125 Gb/s			0.43	UI
		1.0 Gb/s – 1.0625 Gb/s			0.47	UI
		600 Mb/s – 999 Mb/s			0.47 ⁽²⁾	
Receive latency ⁽³⁾	T_{RXLAT}			25	42 ⁽⁴⁾	RXUSRCLK cycles
RXUSRCLK duty cycle	T_{RXDC}		45	50	55	%
RXUSRCLK2 duty cycle	T_{RX2DC}		45	50	55	%

Notes:

1. UI = Unit Interval
2. The oversampling techniques described in [XAPP572](#) are required to meet these specifications for serial rates less than 1 Gb/s.
3. Receive latency delay RXP/RXN to RXDATA. Refer to [RocketIO Transceiver User Guide](#) for more information on calculating latency.
4. This maximum may occur when certain conditions are present and clock correction and channel bonding are enabled. If these functions are both disabled, the maximum will be near the typical values.

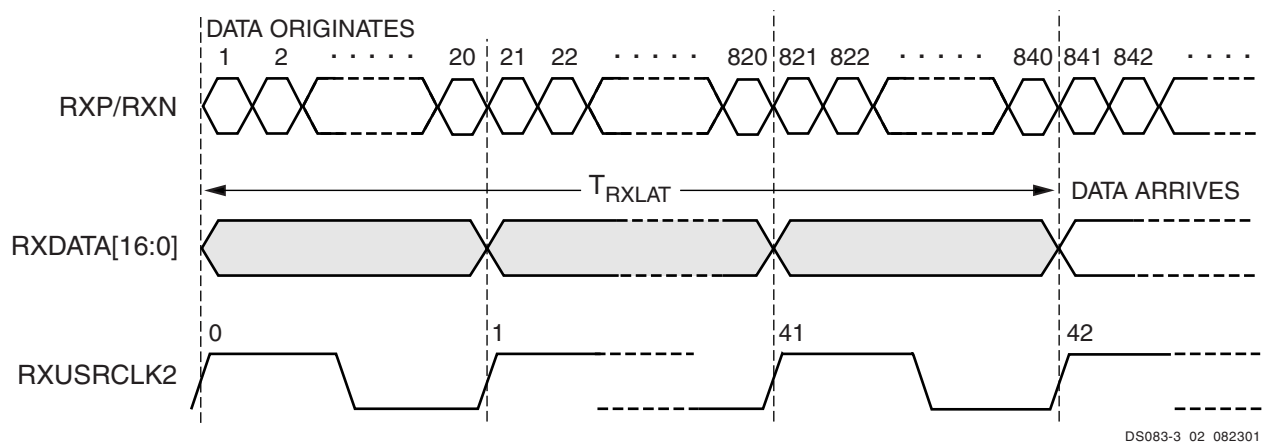


Table 3: Virtex-II Pro Available I/Os and RocketIO MGT Pins per Device/Package Combination

Virtex-II Pro Device	User I/Os & RocketIO MGT Pins	Virtex-II Pro Package ⁽¹⁾									
		FG256/ FGG256	FG456/ FGG456	FG676/ FGG456	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
XC2VP2	Available User I/Os	140	156	-	204	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	76	-	100	-	-	-	-	-	-
XC2VP4	Available User I/Os	140	248	-	348	-	-	-	-	-	-
	RocketIO MGT Pins	36	36	-	36	-	-	-	-	-	-
	Differential I/O Pairs	68	122	-	172	-	-	-	-	-	-
XC2VP7	Available User I/Os	-	248	-	396	396	-	-	-	-	-
	RocketIO MGT Pins	-	72	-	72	72	-	-	-	-	-
	Differential I/O Pairs	-	122	-	196	196	-	-	-	-	-
XC2VP20	Available User I/Os	-	-	404	-	556	564	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	196	-	272	276	-	-	-	-
XC2VPX20	Available User I/Os	-	-	-	-	552	-	-	-	-	-
	RocketIO X MGT Pins	-	-	-	-	72	-	-	-	-	-
	Differential I/O Pairs	-	-	-	-	270	-	-	-	-	-
XC2VP30	Available User I/Os	-	-	416	-	556	644	-	-	-	-
	RocketIO MGT Pins	-	-	72	-	72	72	-	-	-	-
	Differential I/O Pairs	-	-	202	-	272	316	-	-	-	-
XC2VP40	Available User I/Os	-	-	416	-	-	692	804	-	-	-
	RocketIO MGT Pins	-	-	72	-	-	108	0	-	-	-
	Differential I/O Pairs	-	-	202	-	-	340	396	-	-	-
XC2VP50	Available User I/Os	-	-	-	-	-	692	812	852	-	-
	RocketIO MGT Pins	-	-	-	-	-	144	0	144	-	-
	Differential I/O Pairs	-	-	-	-	-	340	400	420	-	-

Table 6: FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
4	IO_L69P_4/VREF_4	AA12			
4	IO_L74N_4/GCLK3S	U12			
4	IO_L74P_4/GCLK2P	V12			
4	IO_L75N_4/GCLK1S	W12			
4	IO_L75P_4/GCLK0P	Y12			
5	IO_L75N_5/GCLK7S	Y11			
5	IO_L75P_5/GCLK6P	W11			
5	IO_L74N_5/GCLK5S	V11			
5	IO_L74P_5/GCLK4P	U11			
5	IO_L69N_5/VREF_5	AA11			
5	IO_L69P_5	Y10			
5	IO_L67N_5	V10			
5	IO_L67P_5	U10			
5	IO_L09N_5/VREF_5	W10			
5	IO_L09P_5	W9			
5	IO_L07N_5/VREF_5	V9			
5	IO_L07P_5	U9			
5	IO_L06N_5/VRP_5	Y8			
5	IO_L06P_5/VRN_5	W8			
5	IO_L05_5/No_Pair	V8			
5	IO_L03N_5/D4	Y7			
5	IO_L03P_5/D5	W7			
5	IO_L02N_5/D6	V7			
5	IO_L02P_5/D7	V6			
5	IO_L01N_5/RDWR_B	W6			
5	IO_L01P_5/CS_B	W5			
6	IO_L01P_6/VRN_6	AB2			
6	IO_L01N_6/VRP_6	AA1			
6	IO_L02P_6	Y2			
6	IO_L02N_6	Y1			
6	IO_L03P_6	W2			
6	IO_L03N_6/VREF_6	W1			
6	IO_L05P_6	V4			
6	IO_L05N_6	V3			
6	IO_L06P_6	V2			

Table 7: FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
4	IO_L54N_4	V15			
4	IO_L54P_4	W15			
4	IO_L55N_4	Y15			
4	IO_L55P_4	AA15			
4	IO_L57N_4	AB15			
4	IO_L57P_4/VREF_4	AA14			
4	IO_L67N_4	AC15			
4	IO_L67P_4	AD15			
4	IO_L69N_4	V14			
4	IO_L69P_4/VREF_4	W14			
4	IO_L74N_4/GCLK3S	AB14			
4	IO_L74P_4/GCLK2P	AC14			
4	IO_L75N_4/GCLK1S	AD14			
4	IO_L75P_4/GCLK0P	AE14			
5	IO_L75N_5/GCLK7S	AE13			
5	IO_L75P_5/GCLK6P	AD13			
5	IO_L74N_5/GCLK5S	AC13			
5	IO_L74P_5/GCLK4P	AB13			
5	IO_L69N_5/VREF_5	W13			
5	IO_L69P_5	V13			
5	IO_L67N_5	AD12			
5	IO_L67P_5	AC12			
5	IO_L57N_5/VREF_5	AA13			
5	IO_L57P_5	AB12			
5	IO_L55N_5	AA12			
5	IO_L55P_5	Y12			
5	IO_L54N_5	W12			
5	IO_L54P_5	V12			
5	IO_L53_5/No_Pair	AA11			
5	IO_L50_5/No_Pair	Y11			
5	IO_L49N_5	AD10			
5	IO_L49P_5	AC10			
5	IO_L48N_5	AB11			
5	IO_L48P_5	AB10			

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
4	IO_L05_4/No_Pair		AD8			
4	IO_L06N_4/VRP_4		AG8			
4	IO_L06P_4/VRN_4		AH8			
4	IO_L07N_4		AC10			
4	IO_L07P_4/VREF_4		AD10			
4	IO_L08N_4		AE7			
4	IO_L08P_4		AE8			
4	IO_L09N_4		AJ8			
4	IO_L09P_4/VREF_4		AK8			
4	IO_L37N_4		AC11			
4	IO_L37P_4		AD11			
4	IO_L38N_4		AF8			
4	IO_L38P_4		AF9			
4	IO_L39N_4		AF10			
4	IO_L39P_4		AG10			
4	IO_L43N_4		AC12			
4	IO_L43P_4		AD12			
4	IO_L44N_4		AE9			
4	IO_L44P_4		AE10			
4	IO_L45N_4		AH9			
4	IO_L45P_4/VREF_4		AJ9			
4	IO_L46N_4		AC13	NC		
4	IO_L46P_4		AD13	NC		
4	IO_L47N_4		AE11	NC		
4	IO_L47P_4		AE12	NC		
4	IO_L48N_4		AH10	NC		
4	IO_L48P_4		AH11	NC		
4	IO_L49N_4		AB14	NC		
4	IO_L49P_4		AC14	NC		
4	IO_L50_4/No_Pair		AF11	NC		
4	IO_L53_4/No_Pair		AG11	NC		
4	IO_L54N_4		AJ10	NC		
4	IO_L54P_4		AK10	NC		
4	IO_L56N_4		AF12	NC		
4	IO_L56P_4		AF13	NC		
4	IO_L57N_4		AG13	NC		

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	GND		U18			
N/A	GND		U17			
N/A	GND		U16			
N/A	GND		U15			
N/A	GND		U14			
N/A	GND		U13			
N/A	GND		U12			
N/A	GND		U6			
N/A	GND		T19			
N/A	GND		T18			
N/A	GND		T17			
N/A	GND		T16			
N/A	GND		T15			
N/A	GND		T14			
N/A	GND		T13			
N/A	GND		T12			
N/A	GND		R19			
N/A	GND		R18			
N/A	GND		R17			
N/A	GND		R16			
N/A	GND		R15			
N/A	GND		R14			
N/A	GND		R13			
N/A	GND		R12			
N/A	GND		P25			
N/A	GND		P19			
N/A	GND		P18			
N/A	GND		P17			
N/A	GND		P16			
N/A	GND		P15			
N/A	GND		P14			
N/A	GND		P13			
N/A	GND		P12			
N/A	GND		P6			
N/A	GND		N19			
N/A	GND		N18			

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
1	IO_L37N_1	G13				
1	IO_L37P_1	H13				
1	IO_L27N_1/VREF_1	J13	NC	NC		
1	IO_L27P_1	K13	NC	NC		
1	IO_L26N_1	D8	NC	NC		
1	IO_L26P_1	E8	NC	NC		
1	IO_L25N_1	F12	NC	NC		
1	IO_L25P_1	G12	NC	NC		
1	IO_L21N_1	G11	NC	NC		
1	IO_L21P_1	H11	NC	NC		
1	IO_L20N_1	C7	NC	NC		
1	IO_L20P_1	D7	NC	NC		
1	IO_L19N_1	E11	NC	NC		
1	IO_L19P_1	F11	NC	NC		
1	IO_L09N_1/VREF_1	J12				
1	IO_L09P_1	K12				
1	IO_L08N_1	D6				
1	IO_L08P_1	D5				
1	IO_L07N_1	E9				
1	IO_L07P_1	F9				
1	IO_L06N_1	J11				
1	IO_L06P_1	K11				
1	IO_L05_1/No_Pair	J10				
1	IO_L03N_1/VREF_1	G10				
1	IO_L03P_1	H10				
1	IO_L02N_1	G9				
1	IO_L02P_1	H9				
1	IO_L01N_1/VRP_1	E7				
1	IO_L01P_1/VRN_1	E6				
2	IO_L01N_2/VRP_2	D2				
2	IO_L01P_2/VRN_2	D1				
2	IO_L02N_2	F8				
2	IO_L02P_2	F7				
2	IO_L03N_2	E4				
2	IO_L03P_2	E3				
2	IO_L04N_2/VREF_2	E2				
2	IO_L04P_2	E1				

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
2	IO_L05N_2	J8				
2	IO_L05P_2	J7				
2	IO_L06N_2	F5				
2	IO_L06P_2	F4				
2	IO_L15N_2	G4	NC			
2	IO_L15P_2	G3	NC			
2	IO_L16N_2/VREF_2	G6	NC			
2	IO_L16P_2	G5	NC			
2	IO_L17N_2	F2	NC			
2	IO_L17P_2	F1	NC			
2	IO_L18N_2	L10	NC			
2	IO_L18P_2	L9	NC			
2	IO_L19N_2	H6	NC			
2	IO_L19P_2	H5	NC			
2	IO_L20N_2	G2	NC			
2	IO_L20P_2	G1	NC			
2	IO_L21N_2	J6	NC			
2	IO_L21P_2	J5	NC			
2	IO_L22N_2/VREF_2	J4	NC			
2	IO_L22P_2	J3	NC			
2	IO_L23N_2	K8	NC			
2	IO_L23P_2	K7	NC			
2	IO_L24N_2	H4	NC			
2	IO_L24P_2	H3	NC			
2	IO_L31N_2	H2				
2	IO_L31P_2	H1				
2	IO_L32N_2	M10				
2	IO_L32P_2	M9				
2	IO_L33N_2	K5				
2	IO_L33P_2	K4				
2	IO_L34N_2/VREF_2	J2				
2	IO_L34P_2	K2				
2	IO_L35N_2	L8				
2	IO_L35P_2	L7				
2	IO_L36N_2	L6				
2	IO_L36P_2	L5				
2	IO_L37N_2	K1				
2	IO_L37P_2	L1				

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
5	IO_L69P_5	AJ18		
5	IO_L68N_5	AF18		
5	IO_L68P_5	AG18		
5	IO_L67N_5	AM19		
5	IO_L67P_5	AN19		
5	IO_L66N_5/VREF_5	AH19	NC	
5	IO_L66P_5	AJ19	NC	
5	IO_L57N_5/VREF_5	AN20		
5	IO_L57P_5	AP20		
5	IO_L56N_5	AD19		
5	IO_L56P_5	AE19		
5	IO_L55N_5	AL19		
5	IO_L55P_5	AM20		
5	IO_L54N_5	AJ20		
5	IO_L54P_5	AK20		
5	IO_L53_5/No_Pair	AG19		
5	IO_L50_5/No_Pair	AH20		
5	IO_L49N_5	AN21		
5	IO_L49P_5	AP21		
5	IO_L48N_5	AL21		
5	IO_L48P_5	AM21		
5	IO_L47N_5	AD20		
5	IO_L47P_5	AE20		
5	IO_L46N_5	AJ21		
5	IO_L46P_5	AK21		
5	IO_L45N_5/VREF_5	AG21		
5	IO_L45P_5	AH21		
5	IO_L44N_5	AD21		
5	IO_L44P_5	AE21		
5	IO_L43N_5	AM22		
5	IO_L43P_5	AN22		
5	IO_L39N_5	AH22		
5	IO_L39P_5	AJ22		
5	IO_L38N_5	AF20		
5	IO_L38P_5	AF21		
5	IO_L37N_5	AN23		
5	IO_L37P_5	AP23		
5	IO_L27N_5/VREF_5	AL22		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L82N_7/VREF_7	G37	NC	
7	IO_L81P_7	G33	NC	
7	IO_L81N_7	G34	NC	
7	IO_L79P_7	F38	NC	
7	IO_L79N_7	F39	NC	
7	IO_L78P_7	F36	NC	
7	IO_L78N_7	F37	NC	
7	IO_L76P_7	G35	NC	
7	IO_L76N_7/VREF_7	F35	NC	
7	IO_L75P_7	E37	NC	
7	IO_L75N_7	E38	NC	
7	IO_L73P_7	D38	NC	
7	IO_L73N_7	D39	NC	
7	IO_L06P_7	F33		
7	IO_L06N_7	E33		
7	IO_L05P_7	J31		
7	IO_L05N_7	H32		
7	IO_L04P_7	E34		
7	IO_L04N_7/VREF_7	D34		
7	IO_L03P_7	D35		
7	IO_L03N_7	C35		
7	IO_L02P_7	H31		
7	IO_L02N_7	G31		
7	IO_L01P_7/VRN_7	D33		
7	IO_L01N_7/VRP_7	C33		
7	VCCO_7	E39		
7	VCCO_7	U37		
7	VCCO_7	N36		
7	VCCO_7	J36		
7	VCCO_7	E36		
7	VCCO_7	Y35		
7	VCCO_7	U33		
7	VCCO_7	N32		
7	VCCO_7	J32		
7	VCCO_7	F32		
7	VCCO_7	U29		
7	VCCO_7	N28		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L34N_6		AH38		
6	IO_L35P_6		AH31		
6	IO_L35N_6		AH32		
6	IO_L36P_6		AJ40		
6	IO_L36N_6		AH40		
6	IO_L37P_6		AH41		
6	IO_L37N_6		AH42		
6	IO_L38P_6		AH35		
6	IO_L38N_6		AG35		
6	IO_L39P_6		AG36		
6	IO_L39N_6/VREF_6		AG37		
6	IO_L40P_6		AG38		
6	IO_L40N_6		AG39		
6	IO_L41P_6		AG32		
6	IO_L41N_6		AG33		
6	IO_L42P_6		AG40		
6	IO_L42N_6		AG41		
6	IO_L43P_6		AF33		
6	IO_L43N_6		AF34		
6	IO_L44P_6		AF35		
6	IO_L44N_6		AF36		
6	IO_L45P_6		AF37		
6	IO_L45N_6/VREF_6		AF38		
6	IO_L46P_6		AF39		
6	IO_L46N_6		AF40		
6	IO_L47P_6		AF31		
6	IO_L47N_6		AG31		
6	IO_L48P_6		AF41		
6	IO_L48N_6		AF42		
6	IO_L49P_6		AE35		
6	IO_L49N_6		AE36		
6	IO_L50P_6		AE31		
6	IO_L50N_6		AF32		
6	IO_L51P_6		AE38		
6	IO_L51N_6/VREF_6		AE39		
6	IO_L52P_6		AE41		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L09P_7		K36		
7	IO_L09N_7		K35		
7	IO_L08P_7		K38		
7	IO_L08N_7		K37		
7	IO_L07P_7		L33		
7	IO_L07N_7		K34		
7	IO_L84P_7		J41		
7	IO_L84N_7		J42		
7	IO_L83P_7		J39		
7	IO_L83N_7		J38		
7	IO_L82P_7		J36		
7	IO_L82N_7/VREF_7		J37		
7	IO_L81P_7		J35		
7	IO_L81N_7		H36		
7	IO_L80P_7		H41		
7	IO_L80N_7		H40		
7	IO_L79P_7		H38		
7	IO_L79N_7		H39		
7	IO_L78P_7		H37		
7	IO_L78N_7		G38		
7	IO_L77P_7		G42		
7	IO_L77N_7		G41		
7	IO_L76P_7		G39		
7	IO_L76N_7/VREF_7		G40		
7	IO_L75P_7		F41		
7	IO_L75N_7		F42		
7	IO_L74P_7		F40		
7	IO_L74N_7		F39		
7	IO_L73P_7		E41		
7	IO_L73N_7		E42		
7	IO_L06P_7		D41		
7	IO_L06N_7		D42		
7	IO_L05P_7		E40		
7	IO_L05N_7		D40		
7	IO_L04P_7		F36		
7	IO_L04N_7/VREF_7		G37		

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L26P_7	V31	
7	IO_L26N_7	U31	
7	IO_L25P_7	L41	
7	IO_L25N_7	L42	
7	IO_L24P_7	K40	
7	IO_L24N_7	L40	
7	IO_L23P_7	T34	
7	IO_L23N_7	T35	
7	IO_L22P_7	L38	
7	IO_L22N_7/VREF_7	L39	
7	IO_L21P_7	K36	
7	IO_L21N_7	L36	
7	IO_L20P_7	T32	
7	IO_L20N_7	T33	
7	IO_L19P_7	K41	
7	IO_L19N_7	K42	
7	IO_L18P_7	K37	
7	IO_L18N_7	K38	
7	IO_L17P_7	R34	
7	IO_L17N_7	R35	
7	IO_L16P_7	H42	
7	IO_L16N_7/VREF_7	J41	
7	IO_L15P_7	J39	
7	IO_L15N_7	J40	
7	IO_L14P_7	R32	
7	IO_L14N_7	R33	
7	IO_L13P_7	J36	
7	IO_L13N_7	J37	
7	IO_L12P_7	H40	
7	IO_L12N_7	H41	
7	IO_L11P_7	T31	
7	IO_L11N_7	R31	
7	IO_L10P_7	H38	
7	IO_L10N_7/VREF_7	H39	
7	IO_L09P_7	H36	
7	IO_L09N_7	H37	
7	IO_L08P_7	P34	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	BB34	
N/A	GND	AV34	
N/A	GND	AP34	
N/A	GND	AK34	
N/A	GND	AF34	
N/A	GND	AC34	
N/A	GND	Y34	
N/A	GND	U34	
N/A	GND	N34	
N/A	GND	J34	
N/A	GND	E34	
N/A	GND	A34	
N/A	GND	AD31	
N/A	GND	W31	
N/A	GND	BB30	
N/A	GND	AV30	
N/A	GND	AP30	
N/A	GND	J30	
N/A	GND	E30	
N/A	GND	A30	
N/A	GND	BB26	
N/A	GND	AV26	
N/A	GND	AP26	
N/A	GND	AE26	
N/A	GND	AD26	
N/A	GND	AC26	
N/A	GND	AB26	
N/A	GND	AA26	
N/A	GND	Y26	
N/A	GND	W26	
N/A	GND	V26	
N/A	GND	J26	
N/A	GND	E26	
N/A	GND	A26	
N/A	GND	AF25	
N/A	GND	AE25	
N/A	GND	AD25	