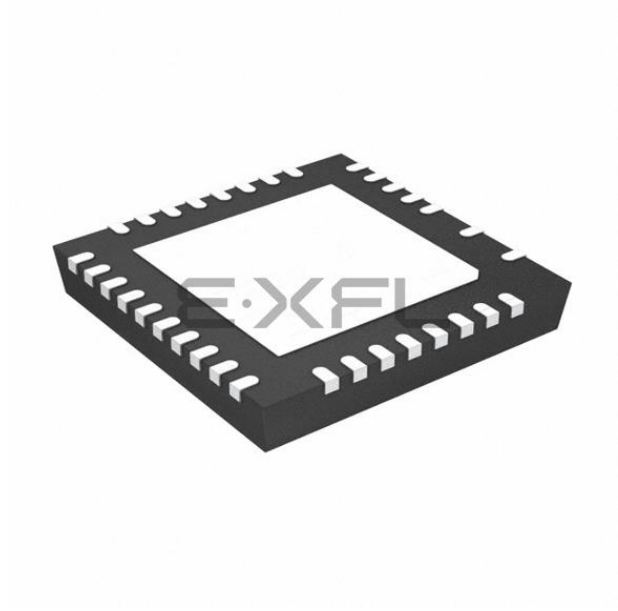

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	29
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	33-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini51tan

CONTENTS

List of Figures

3.2 PIN CONFIGURATION

3.2.1 LQFP 48-pin

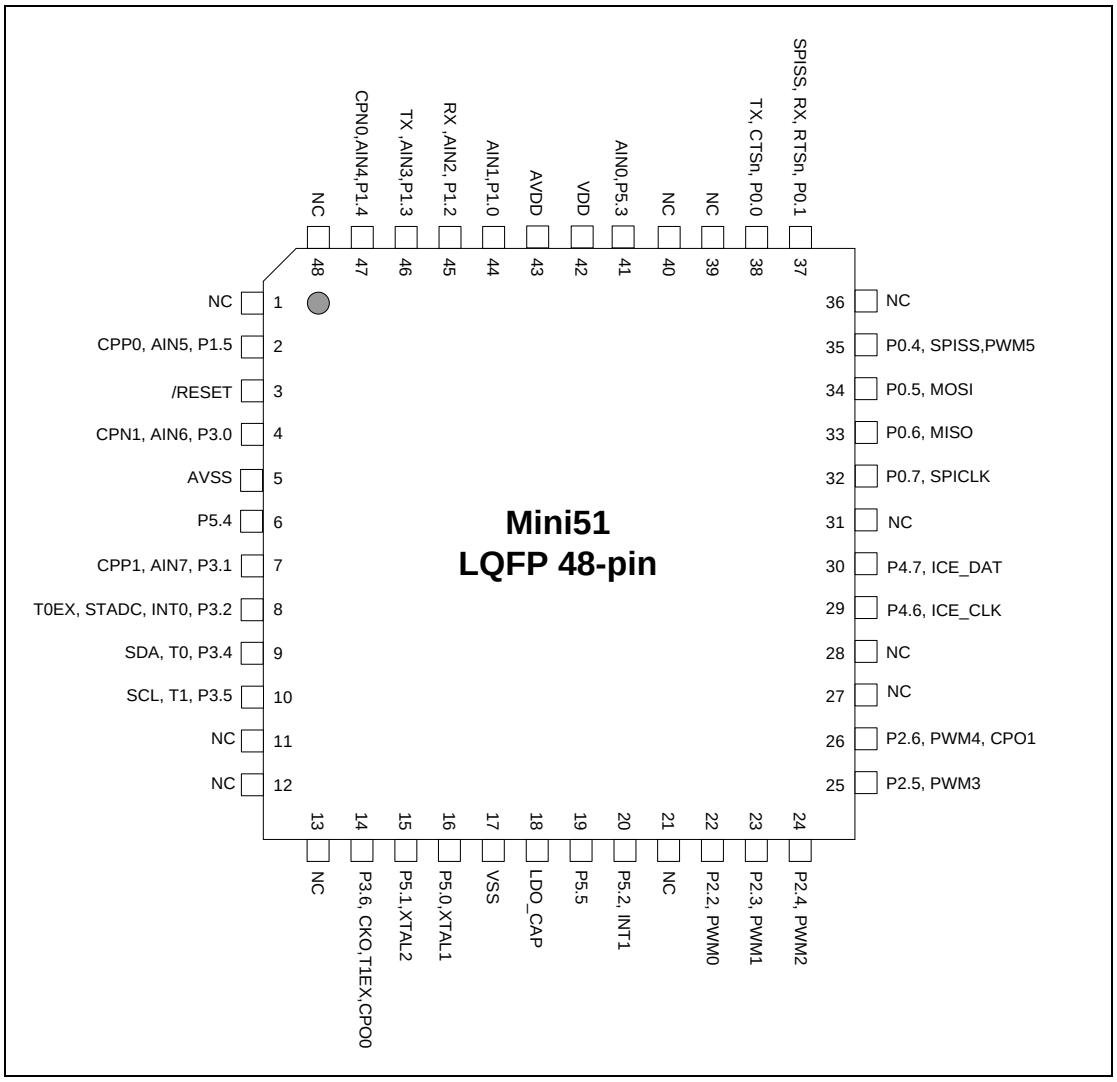

Figure 3.2-1 NuMicro Mini51™ Series LQFP 48-pin Assignment

Pin Number		Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin			
		AIN1	**AI**	ADC analog input pin
45	30	P1.2	**I/O**	Digital GPIO pin
		AIN2	**AI**	ADC analog input pin
		RX	**I**	UART data receiver input pin
46	31	P1.3	**I/O**	Digital GPIO pin
		AIN3	**AI**	ADC analog input pin
		TX	**O**	UART transmitter output pin
47	32	P1.4	**I/O**	Digital GPIO pin
		AIN4	**I/O**	PWM5: PWM output/Capture input
		CPN0	**AI**	Analog comparator negative input pin
48		NC		Not connected

Table 3.3-1 NuMicro Mini51™ Series Pin Description

[1] I/O type description: I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

5 FUNCTIONAL DESCRIPTION

5.1 Memory Organization

5.1.1 Overview

The NuMicro Mini51™ series provides a 4G-byte address space for programmers. The memory locations assigned to each on-chip modules are shown in **錯誤! 找不到參照來源。**. The detailed register and memory addressing and programming will be described in the following sections for individual on-chip modules. The NuMicro Mini51™ series only supports little-endian data format.

5.1.2 System Memory Map

The memory locations assigned to each on-chip controllers are shown in the following table.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_3FFF	FLASH_BA	Flash Memory Space (16 KB)
0x2000_0000 – 0x2000_07FF	SRAM_BA	SRAM Memory Space (2 KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GP_BA	GPIO Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB1 Controllers Space (0x4000_0000 – 0x401F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C_BA	I^2C Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI_BA	SPI Control Registers
0x4004_0000 – 0x4004_3FFF	PWM_BA	PWM Control Registers
0x4005_0000 – 0x4005_3FFF	UART_BA	UART Control Registers
0x400D_0000 – 0x400D_3FFF	CMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
System Controllers Space (0xE000_E000 – 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	Nested Vectored Interrupt Control Registers
0xE000_ED00 – 0xE000_ED8F	SCB_BA	System Control Block Registers

Table 5.1-1 Address Space Assignments for On-Chip Modules

Fault".

Exception Name	Exception Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 5.2-1 Exception Model

Exception Number	IRQ Number (Bit in Interrupt Registers)	Exception Name	Source IP	Exception Description	Power-down Wake-up
1 ~ 15	-	**-**	-	System exceptions	-
16	0	**BOD_OUT**	Brown-out	Brown-out low voltage detected interrupt	Yes
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt	Yes
18	2	**EINT0**	GPIO	External signal interrupt from P3.2 pin	Yes
19	3	**EINT1**	GPIO	External signal interrupt from P5.2 pin	Yes
20	4	**GP0/1_INT**	GPIO	External signal interrupt from GPIO group P0~P1	Yes
21	5	**GP2/3/4_INT**	GPIO	External signal interrupt from GPIO group P2~P4 except P3.2	Yes
22	6	**PWM_INT**	PWM	PWM interrupt	No
23	7	**BRAKE_INT**	PWM	PWM interrupt	No
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt	Yes
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt	Yes
26 ~ 27	10 ~ 11	**-**	-	-	
28	12	**UART_INT**	UART	UART interrupt	Yes
29	13	**-**	-	-	

5.3 System Manager

5.3.1 Overview

The following functions are included in the system manager section:

- System Memory Map
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System management registers for product ID
- System management registers for chip and module functional reset and multi-function pin control
- Brown-out and chip miscellaneous Control Register
- Combined peripheral interrupt source identify

5.3.2 System Reset

The system reset includes one of the following as the event occurs. For these reset events flags can be read by RSTSRC register.

- Power-On Reset (POR)
- Low level on the /RESET pin
- Watchdog Time-out Reset (WDT)
- Brown-out Detected Reset (BOD)
- Cortex™-M0 CPU Reset
- Software one shot Reset

5.3.3 System Power Distribution

In this device, the power distribution is divided into three segments.

- Analog power from AVDD and AVSS supplies power for analog module operation
- Digital power from VDD and VSS supplies power to the internal regulator which provides a fixed 1.8V power for digital operation and I/O pins
- Built-in capacitor for internal voltage regulator

The output of internal voltage regulator, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. **錯誤! 找不到參照來源。** shows the power architecture of this device.

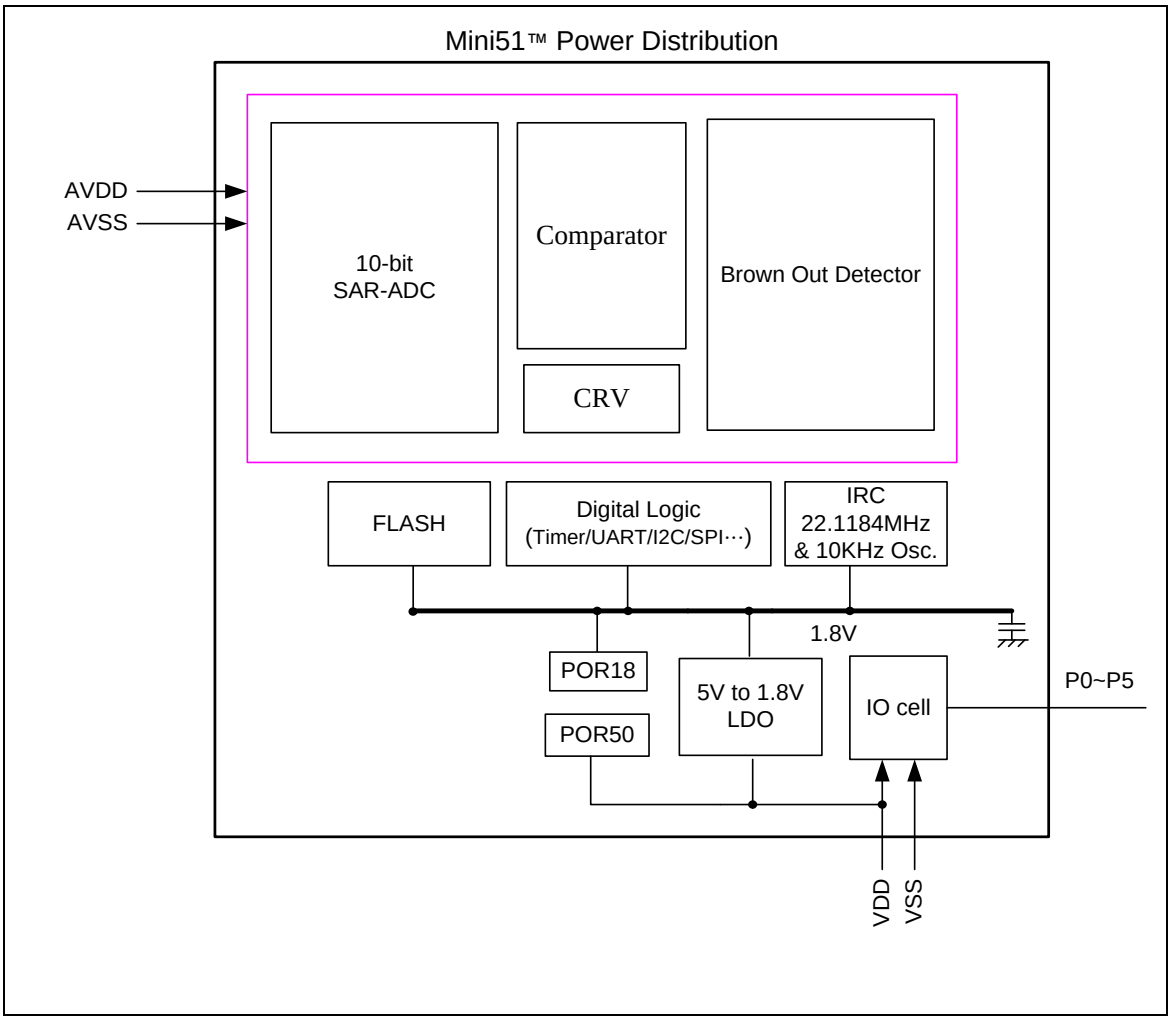

Figure 5.3-1 NuMicro Mini51™ Series Power Distribution Diagram

5.4 Clock Controller

5.4.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a 4-bit clock divider. The chip will not enter Power-down mode until CPU sets the power-down enable bit (PWR_DOWN_EN) and Cortex-M0 core executes the WFI instruction. After that, the chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the external crystal and internal 22.1184 MHz oscillator to reduce the overall system power consumption.

5.4.2 Clock Generator

The clock generator consists of 3 sources which are listed below:

- One external 12 MHz (HXT) or 32 KHz (LXT) crystal
- One internal 22.1184 MHz RC oscillator (HIRC)
- One internal 10 KHz oscillator (LIRC)

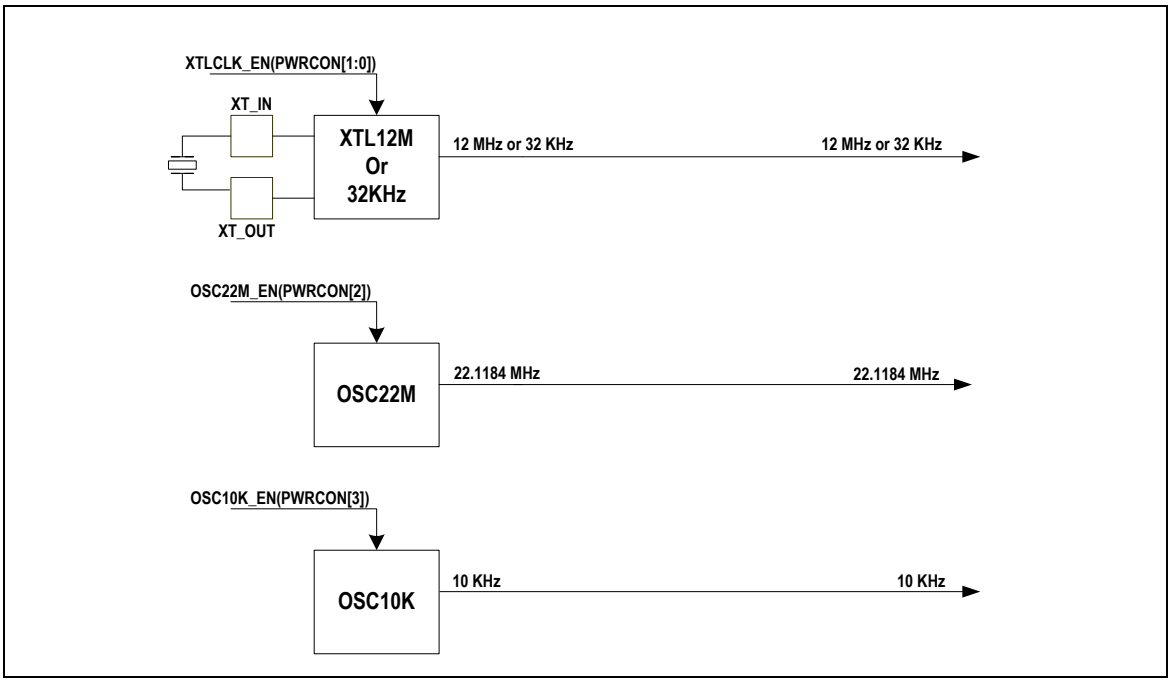

Figure 5.4-1 Clock Generator Block Diagram

5.4.3 System Clock and SysTick Clock

The system clock has 3 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown below.

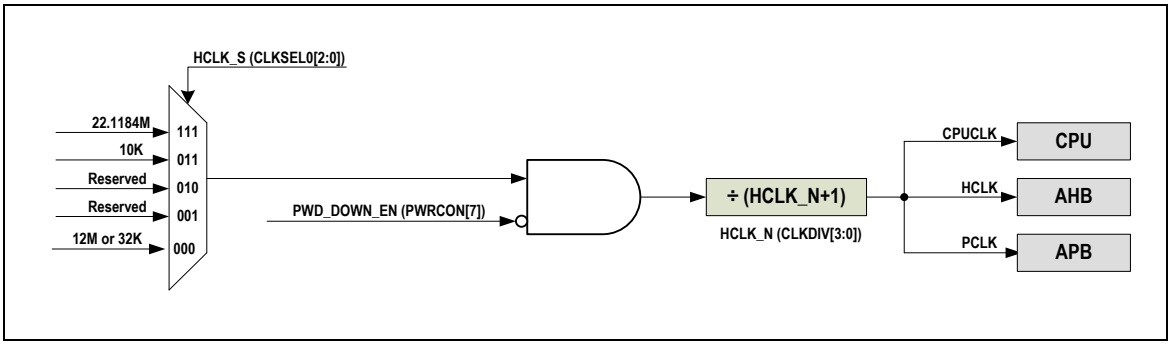

Figure 5.4-2 System Clock Block Diagram

The clock source of SysTick in Cortex-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in **錯誤! 找不到參照來源。**.

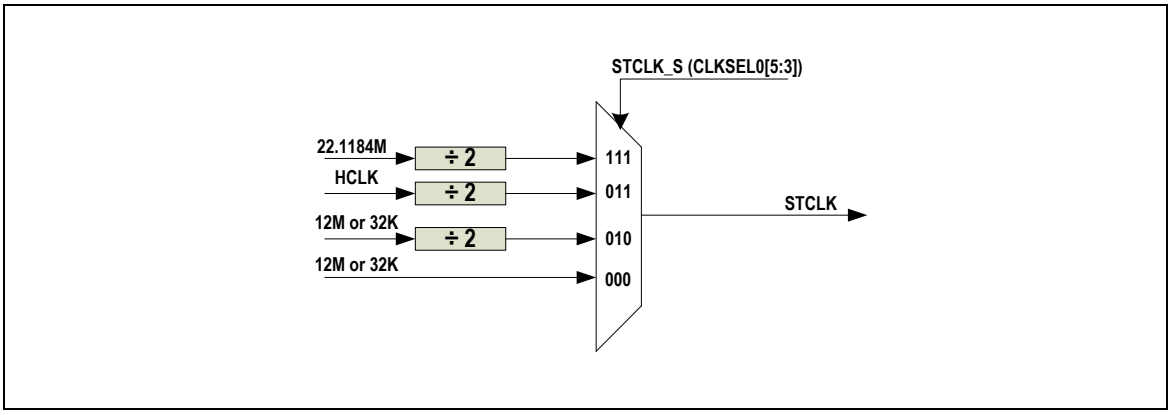

Figure 5.4-3 SysTick Clock Control Block Diagram

	Ext. CLK (12M or 32K)	IRC22.1184M	IRC10K	PCLK
WDT	Yes	No	Yes	Yes
Timer0	Yes	Yes	Yes	Yes
Timer1	Yes	Yes	Yes	Yes
I^2C	No	No	No	Yes
SPI	No	No	No	Yes
UART	Yes	Yes	No	No
PWM	No	No	No	Yes
ADC	Yes	Yes	No	Yes
ACMP	No	No	No	Yes

Table 5.4-1 Peripherals Engine Clock Source Selection Table

5.4.6 Power-down Mode Clock

When entering Power-down mode, some clock sources and peripheral clocks and system clocks will be disabled. Some clock sources and peripheral clocks are still active in Power-down mode.

Clocks that still be kept active are listed below.

- Clock Generator
  - Internal 10 KHz RC oscillator (LIRC) clock
  - External 32.768 KHz crystal oscillator (LXT) clock (If PD_32K = “1” and XTLCLK_EN[1:0] = “10”)
- Peripherals Clock (When these IP adopt 10 KHz as clock source)
  - Watchdog Clock
  - Timer 0/1 Clock

5.5 Comparator Controller (CMPC)

5.5.1 Overview

The NuMicro Mini51™ Series contains two comparators which can be used in a number of different configurations. The comparator output is a logical one when positive input is greater than negative input; otherwise, the output is zero. Each comparator can be configured to cause an interrupt when the comparator output value changes. The block diagram is shown in **錯誤! 找不到參照來源。**.

Note that the analog input port pins must be configured as the input type before Analog Comparator function is enabled.

5.5.2 Features

- Analog input voltage range: 0 ~ 5.0V
- Hysteresis function support
- Two analog comparators with optional internal reference voltage input at negative end
- One comparator interrupt requested by one of the comparators

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	Min	MAX	UNIT
DC power supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input voltage	VIN	V_{SS}-0.3	V_{DD}+0.3	V
Oscillator frequency	$1/t_{CLCL}$	4	24	MHz
Operating temperature	TA	-40	+85	°C
Storage temperature	TST	-55	+150	°C
Maximum current into VDD		-	120	mA
Maximum current out of VSS			120	mA
Maximum current sunk by a I/O pin			35	mA
Maximum current sourced by a I/O pin			35	mA
Maximum current sunk by total I/O pins			100	mA
Maximum current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

8.2 DC Electrical Characteristics

(VDD-VSS = 5.0 V, TA = 25°C, FOSC = 24 MHz unless otherwise specified.)

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} = 2.5 V ~ 5.5 V up to 24 MHz
V_{DD} rise rate to ensure internal operation correctly	V_{RISE}	0.05			V/mS	
Power ground	V_{SS} AV_{SS}	-0.3			V	
LDO output voltage	V_{LDO}	-10%	1.8	+10%	V	V_{DD} = 2.5V ~ 5.5V
Analog operating voltage	AV_{DD}	0		V_{DD}	V	
Operating current Normal run mode at 24 MHz	I_{DD1}		9.5		mA	V_{DD} = 5.5V at 24 MHz, all IP Enabled
	I_{DD2}		7.5		mA	V_{DD} = 5.5V at 24 MHz, all IP Disabled
	I_{DD3}		7.5		mA	V_{DD} = 3.3V at 24 MHz, all IP Enabled
	I_{DD4}		6		mA	V_{DD} = 3.3V at 24 MHz, all IP Disabled
Operating current Normal run mode at 12 MHz	I_{DD5}		5.5		mA	V_{DD} = 5.5V at 12 MHz, all IP Enabled
	I_{DD6}		4.5		mA	V_{DD} = 5.5V at 12 MHz, all IP Disabled
	I_{DD7}		4		mA	V_{DD} = 3.3V at 12 MHz, all IP Enabled
	I_{DD8}		3		mA	V_{DD} = 3.3V at 12 MHz, all IP Disabled
Operating current Normal run mode at 4 MHz	I_{DD9}		3.6		mA	V_{DD} = 5.5V at 4 MHz, all IP Enabled
	I_{DD10}		3.3		mA	V_{DD} = 5.5V at 4 MHz, all IP Disabled
	I_{DD11}		1.7		mA	V_{DD} = 3.3V at 4 MHz, all IP Enabled
	I_{DD12}		1.4		mA	V_{DD} = 3.3V at 4 MHz, all IP Disabled
Operating current Normal run mode at 22.1184 MHz IRC	I_{DD13}		6.6		mA	V_{DD} = 5.5V at 22.1184 MHz, all IP Enabled
	I_{DD14}		5		mA	V_{DD} = 5.5V at 22.1184 MHz, all IP Disabled
	I_{DD15}		6.6		mA	V_{DD} = 3.3V at 22.1184 MHz, all IP Enabled
	I_{DD16}		5		mA	V_{DD} = 3.3V at 22.1184 MHz, all IP Disabled

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
	I_{IDLE16}		1.2		mA	V_{DD} = 3.3V at 22.1184 MHz, all IP Disabled
Operating current Idle mode at 32.768 KHz crystal oscillator	I_{IDLE17}		110		µA	V_{DD} = 5.5V at 32.768 KHz, all IP Enabled
	I_{IDLE18}		107		µA	V_{DD} = 5.5V at 32.768 KHz, all IP Disabled
	I_{IDLE19}		105		µA	V_{DD} = 3.3V at 32.768 KHz, all IP Enabled
	I_{IDLE20}		102		µA	V_{DD} = 3.3V at 32.768 KHz, all IP Disabled
Operating current Idle mode at 10 KHz IRC	I_{IDLE21}		103		µA	V_{DD} = 5.5V at 10 KHz, all IP Enabled
	I_{IDLE22}		102		µA	V_{DD} = 5.5V at 10 KHz, all IP Disabled
	I_{IDLE23}		96		µA	V_{DD} = 3.3V at 10 KHz, all IP Enabled
	I_{IDLE24}		95		µA	V_{DD} = 3.3V at 10 KHz, all IP Disabled
Standby current Power-down mode	I_{PWD1}		10		µA	V_{DD} = 5.0V, CPU STOP All IP and Clock OFF
	I_{PWD2}		5		µA	V_{DD} = 3.3V, CPU STOP All IP and Clock OFF
Standby current Power-down mode with 32.768 KHz crystal enabled	I_{PWD3}		12		µA	V_{DD} = 5.0V, CPU STOP All IP and Clock OFF except 32.768KHz crystal oscillator
	I_{PWD4}		7		µA	V_{DD} = 3.3V, CPU STOP All IP and Clock OFF except 32.768KHz crystal oscillator
Input current P0~P5 (Quasi-bidirectional mode)	I_{IN1}		-50	-60	µA	V_{DD} = 5.5 V, V_{IN} = 0 V or V_{IN} = V_{DD}
Input current at /RESET[1]	I_{IN2}	-55	-45	-30	µA	V_{DD} = 3.3 V, V_{IN} = 0.45 V
Input leakage current PA, PB, PC, PD, PE	I_{LK}	-0.1	-	+0.1	µA	V_{DD} = 5.5 V, 0<V_{IN}<V_{DD}
Logic 1 to 0 transition current PA~PE (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	µA	V_{DD} = 5.5 V, V_{IN}<2.0 V
Input low voltage	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5 V

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
P0~P5 (TTL input)		-0.3	-	0.6		V_{DD} = 2.5 V
Input high voltage P0~P5 (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} = 3.0V
Input low voltage P0~P5, (Schmitt input)	V_{IL2}		0.4 V_{DD}		V	
Input high voltage P0~P5, (Schmitt input)	V_{IH2}		0.6 V_{DD}		V	
Hysteresis voltage of P0~P5 (Schmitt input)	V_{HY}		0.2 V_{DD}		V	
Input low voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input high voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Internal /RESET pin pull-up resistor	R_{RST}	40	-	100	KΩ	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	0.3 V_{DD}	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	0.6 V_{DD}	-	V_{DD}+0.5	V	
Source current P0~P5. (Quasi-bidirectional mode)	I_{SR11}	-300	-370	-450	µA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	µA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	µA	V_{DD} = 2.5V, V_S = 2.0V
Source current P0~P5, (Push-pull mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink current P0~P5, (Quasi-bidirectional and Push-pull mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V

Notes:

1. /RESET pin is a Schmitt trigger input.

Figure 8.3-1 Typical Crystal Application Circuit

8.3.4 External 32.768 KHz XTAL Oscillator

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Oscillator frequency	fL_{XTAL}		32.768		KHz	V_{DD} = 2.5V ~ 5.5V
Temperature	TL_{XTAL}	-40		+85	°C	
Operating current	I_{HXTAL}		TBD		μA	V_{DD} = 5.0V

8.3.5 Internal 22.1184 MHz RC Oscillator

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Supply voltage[1]	V_{HRC}		1.8		V	
Center frequency	F_{HRC}	21.89	22.1184	22.34	MHz	25°C, V_{DD} = 5V
		20.57	22.1184	23.23	MHz	-40°C~+85 °C, V_{DD} = 2.5V~5.5V
		21.78	22.0	22.22	MHz	-40°C~+85 °C, V_{DD} = 2.5V~5.5V 32.768K crystal oscillator Enabled and TRIM_SEL = 1
Operating current	I_{HRC}		TBD		mA	

Note: Internal operation voltage comes from LDO.

8.3.6 Internal 10 KHz RC Oscillator

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Supply voltage[1]	V_{LRC}		1.8		V	
Center frequency	F_{LRC}	7	10	13	KHz	25°C, V_{DD} = 5V
		5	10	15	KHz	-40°C = ~+85 °C, V_{DD} = 2.5V~5.5V
Operating current	I_{LRC}		TBD		μA	V_{DD} = 5V

Note: Internal operation voltage comes from LDO.