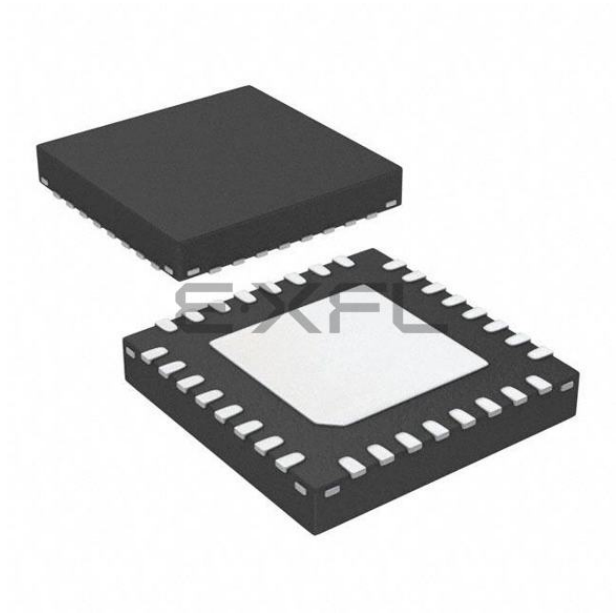

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	29
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini51zan

1 GENERAL DESCRIPTION

The NuMicro Mini51™ series 32-bit microcontroller is embedded with an ARM® Cortex™-M0 core for industrial controls and applications which require high performance, high integration, and low cost. The Cortex™-M0 is the newest ARM embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The NuMicro Mini51™ series can run up to 24 MHz, and thus can afford to support a variety of industrial controls and applications requiring high CPU performance. The NuMicro Mini51™ series provides 4K/8K/16K-byte embedded program flash, size configurable data flash (shared with program flash), 2K-byte flash for the ISP, and 2K-byte embedded SRAM.

A number of system-level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, and low voltage detector, have been incorporated in the NuMicro Mini51™ series to reduce component count, board space, and system cost. These useful functions make the NuMicro Mini51™ series powerful for a wide range of applications.

Additionally, the NuMicro Mini51™ series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, allowing user to update program memory without removing a chip from an actual end product.

2 FEATURES

- Core
  - ARM® Cortex™-M0 core running up to 24 MHz
  - One 24-bit system timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for 32 interrupt inputs, each with 4-level priority
  - Supports Serial Wire Debug (SWD) with 2 watchpoints/4 breakpoints
- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- Memory
  - 4KB/8KB/16KB flash memory for program memory (APROM)
  - Configurable flash memory for data memory (Data Flash)
  - 2KB flash memory for loader (LDROM)
  - 2KB SRAM for internal scratch-pad RAM (SRAM)
- In-System Programming (ISP) and In-Circuit Programming (ICP)
- Clock Control
  - Programmable system clock source
    - Switch clock sources on-the-fly
  - 4 ~ 24 MHz crystal oscillator (HXT)
  - 32.768K crystal oscillator (LXT) for idle wake-up and system operation clock
  - 22.1184 MHz internal oscillator (HIRC) (1% accuracy at 25^0C, 5V)
    - Dynamically calibrating the HIRC OSC to 22.0 MHz ±1% from -40^0C to 85^0C by external 32.768K crystal oscillator (LXT)
  - 10 KHz internal low-power oscillator (LIRC) for watchdog and idle wake-up
- I/O Port
  - Up to 30 GPIO (General Purpose I/O) pins for LQFP-48 package
  - Software-configured I/O type
    - Quasi-bidirectional input/output
    - Push-pull output
    - Open-drain output
    - Input-only (high impendence)
  - Optional Schmitt trigger input
- Timer
  - Two 24-bit Timers with 8-bit prescaler
    - Supports Event Counter mode
    - Supports Toggle Output mode

3.2 PIN CONFIGURATION

3.2.1 LQFP 48-pin

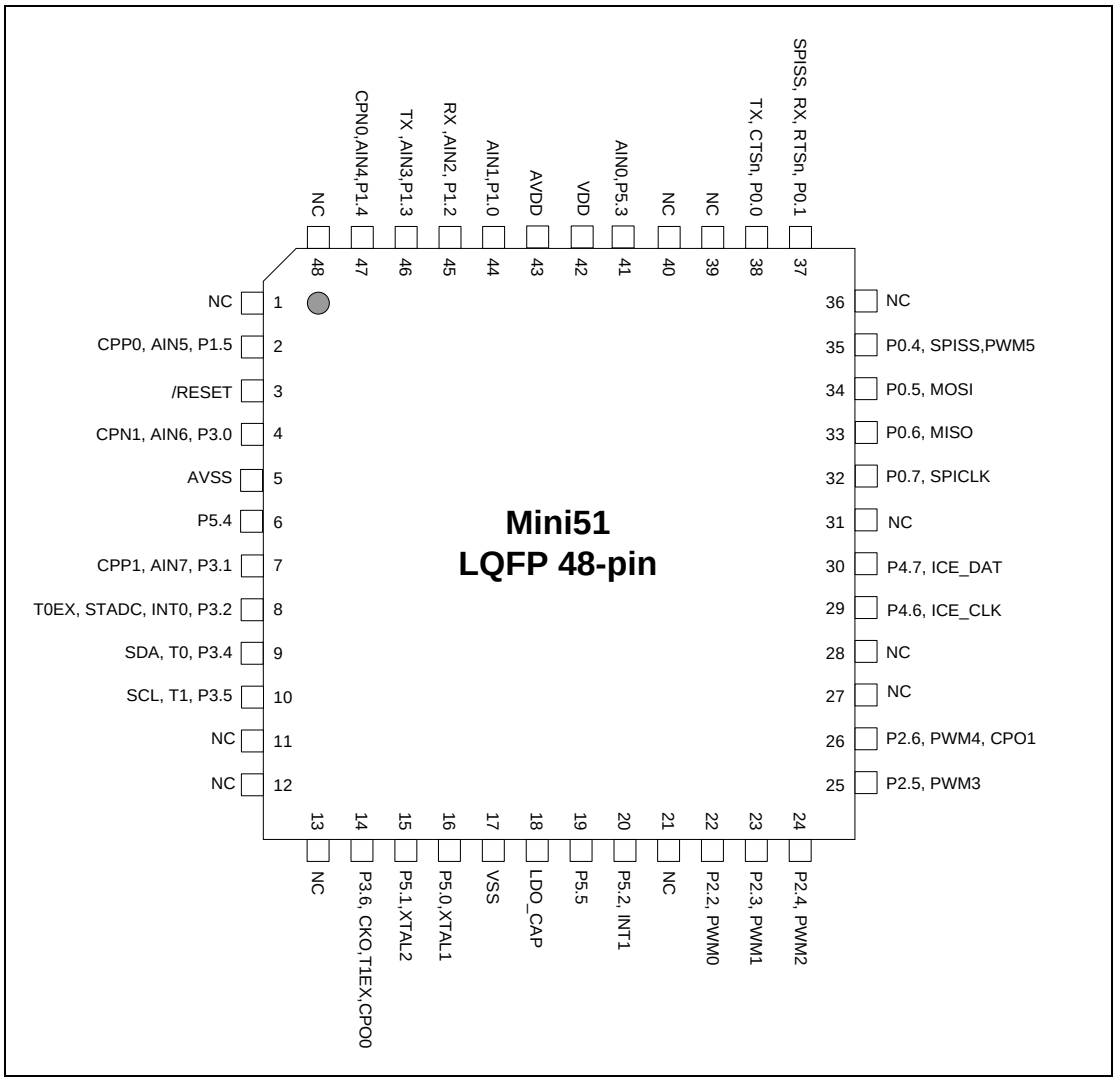

Figure 3.2-1 NuMicro Mini51™ Series LQFP 48-pin Assignment

Pin Number		Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin			
		AIN1	**AI**	ADC analog input pin
45	30	P1.2	**I/O**	Digital GPIO pin
		AIN2	**AI**	ADC analog input pin
		RX	**I**	UART data receiver input pin
46	31	P1.3	**I/O**	Digital GPIO pin
		AIN3	**AI**	ADC analog input pin
		TX	**O**	UART transmitter output pin
47	32	P1.4	**I/O**	Digital GPIO pin
		AIN4	**I/O**	PWM5: PWM output/Capture input
		CPN0	**AI**	Analog comparator negative input pin
48		NC		Not connected

Table 3.3-1 NuMicro Mini51™ Series Pin Description

[1] I/O type description: I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

5 FUNCTIONAL DESCRIPTION

5.1 Memory Organization

5.1.1 Overview

The NuMicro Mini51™ series provides a 4G-byte address space for programmers. The memory locations assigned to each on-chip modules are shown in **錯誤! 找不到參照來源。**. The detailed register and memory addressing and programming will be described in the following sections for individual on-chip modules. The NuMicro Mini51™ series only supports little-endian data format.

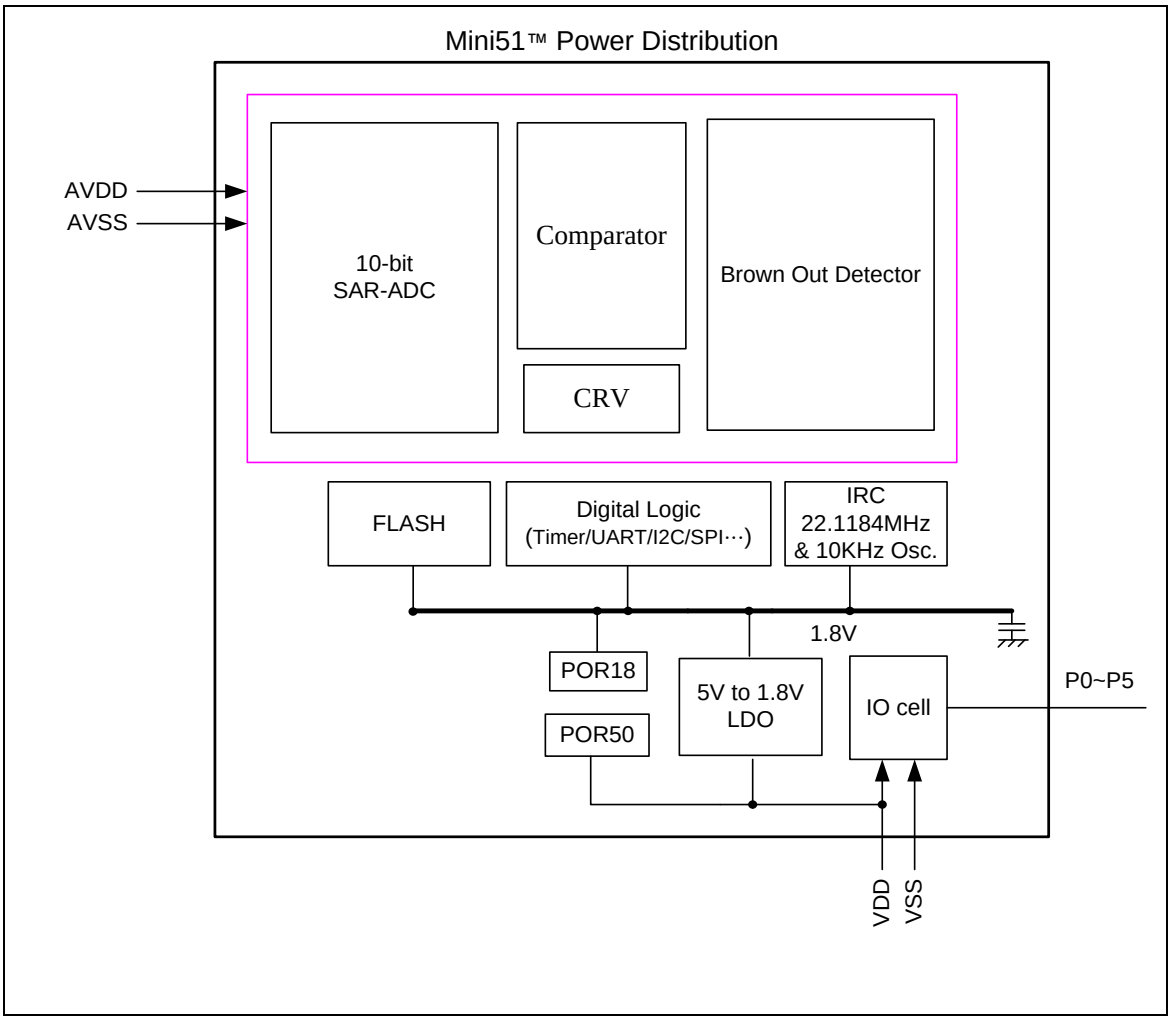

Figure 5.3-1 NuMicro Mini51™ Series Power Distribution Diagram

5.4.4 AHB Clock Source Selection

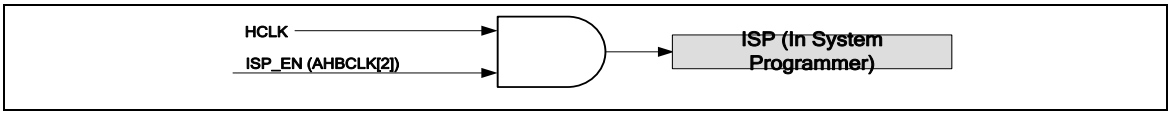

Figure 5.4-4 AHB Clock Source for HCLK

5.4.5 Peripheral Clock Source Selection

The peripheral clock has different clock source switch settings depending on different peripherals. Please refer to the CLKSEL1 and APBCLK register description in section 錯誤! 找不到參照來源。.

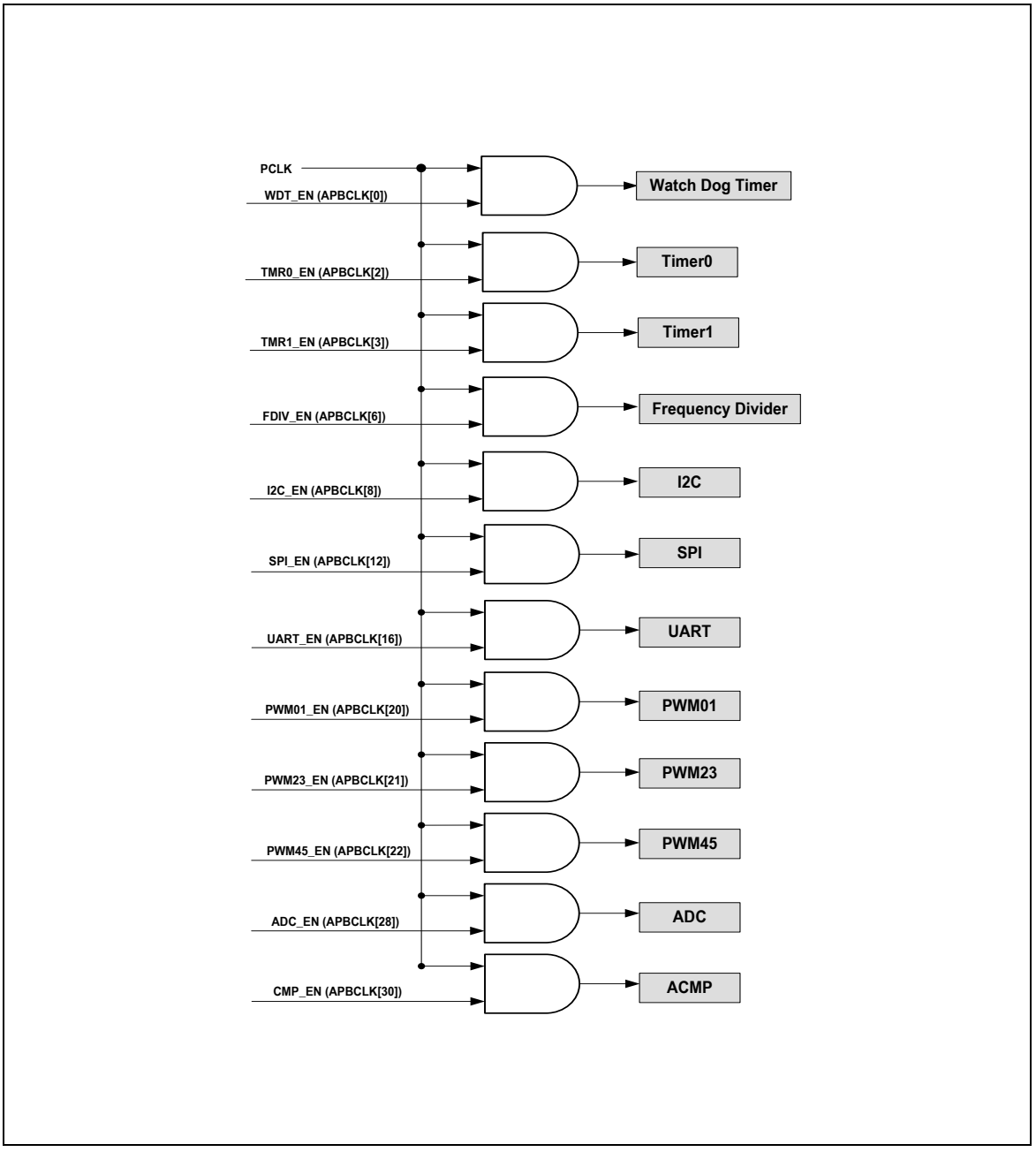

Figure 5.4-5 Peripherals Clock Source Selection for PCLK

5.4.7 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to P3.6. Therefore, there are 16 options of power-of-2 divided clocks with the frequency from Fin/21 to Fin/217 where Fin is input clock frequency to the clock divider.

The output formula is Fout = Fin/2(N+1), where Fin is the input clock frequency, Fout is the clock divider output frequency and N is the 4-bit value in FREQDIV.FSEL[3:0].

When FREQDIV.FDIV_EN[4] is set to high, the rising transition will reset the chained counter and starts counting. When FREQDIV.FDIV_EN[4] is written with zero, the chained counter continuously runs until the divided clock reaches low state and stays in low state.

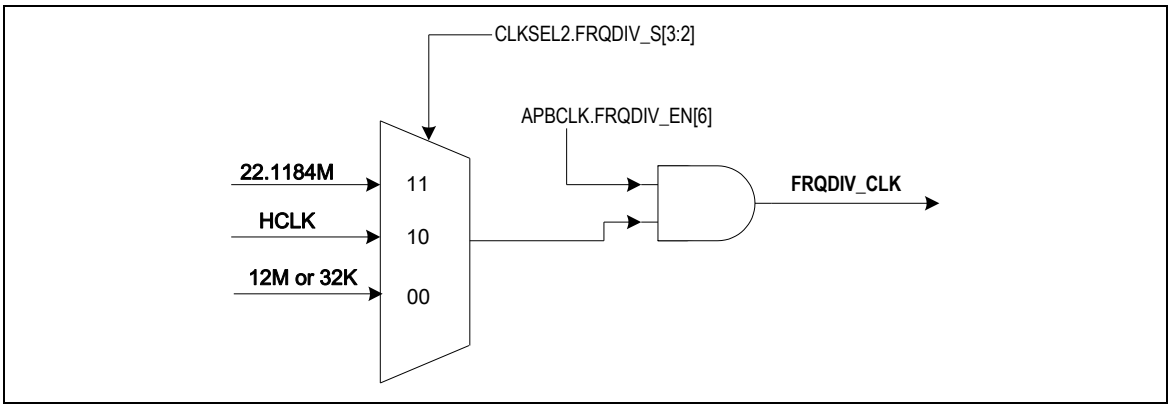

Figure 5.4-6 Clock Source of Frequency Divider

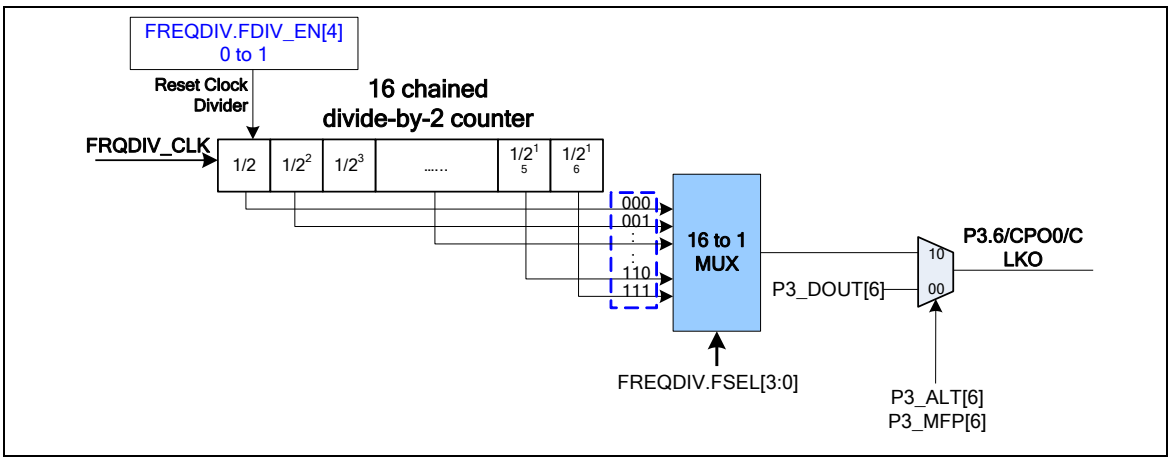

Figure 5.4-7 Block Diagram of Frequency Divider

5.9 I²C Serial Interface Controller (Master/Slave)

5.9.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. Serial 8-bit oriented bi-directional data transfers can be made up 1.0 Mbps.

Data is transferred between a master and a slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more detailed I²C BUS Timing.

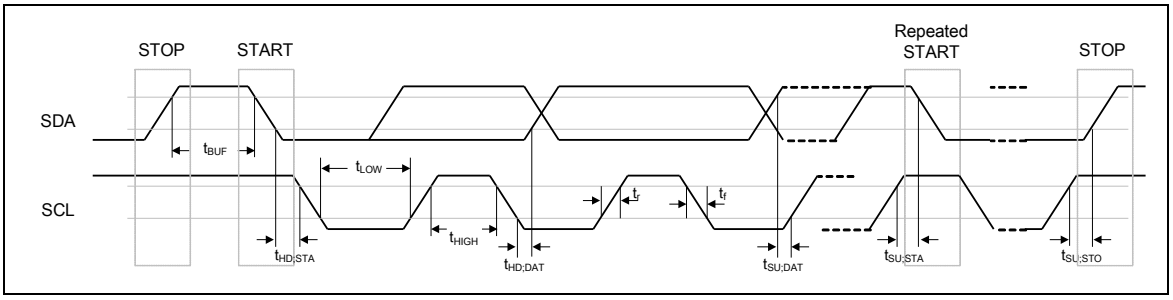

Figure 5.9-1 Bus Timing

The device's on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit ENSI in I2CON should be set to "1". The I²C hardware interfaces to the I²C bus via two pins: SDA (P3.4, serial data line) and SCL (P3.5, serial clock line). Since the pull-up resistor is needed for Pin P3.4 and P3.5 for I²C operation as these are open-drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

5.9.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Supports Master/Slave mode
- Bi-directional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer

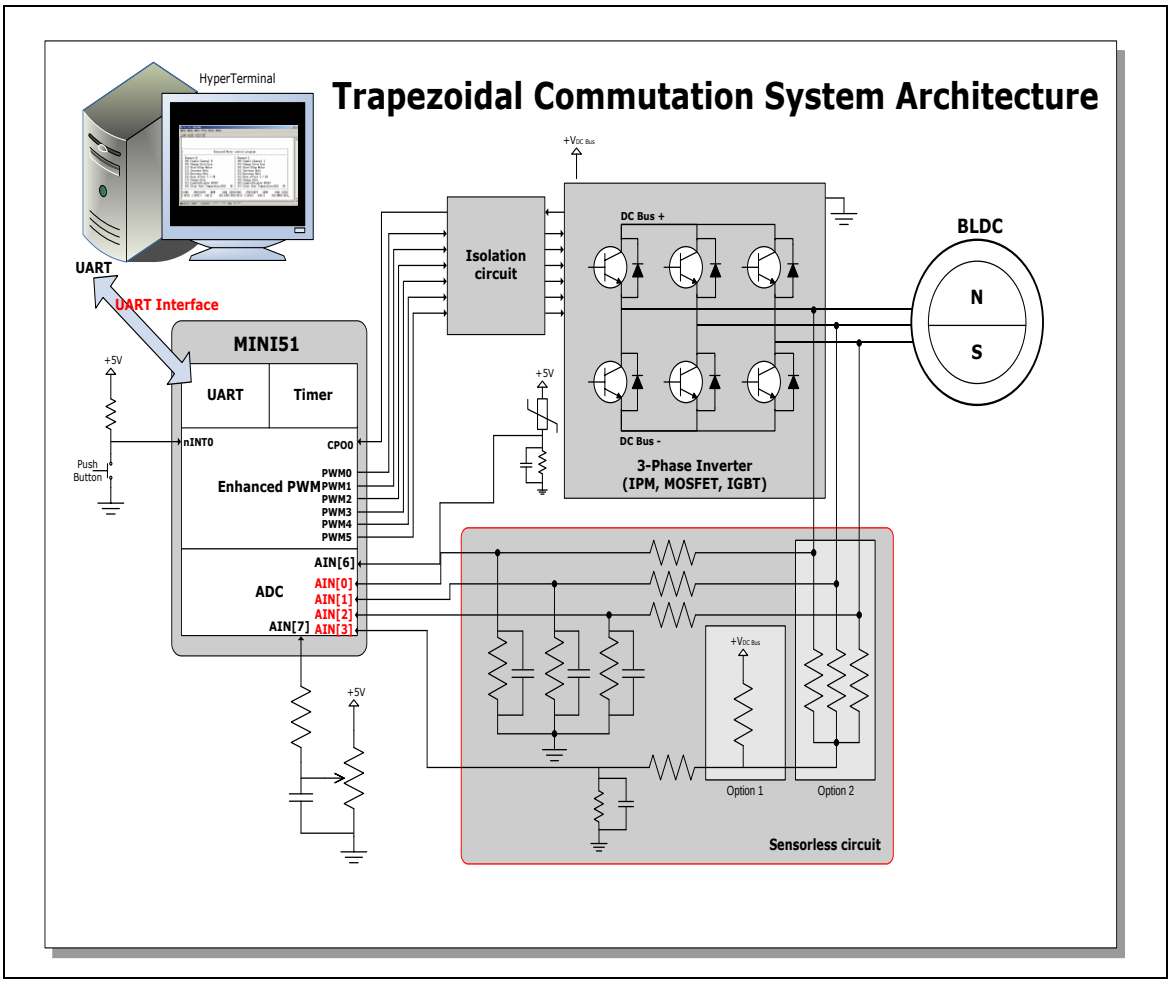

Figure 5.10-1 Application Circuit Diagram

5.13 UART Interface Controller

The NuMicro Mini51™ series provides one channel of Universal Asynchronous Receiver/Transmitters (UART). UART performs Normal Speed UART, and support flow control function.

5.13.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR function, and RS-485 mode functions. Each UART channel supports six types of interrupts, including transmitter FIFO empty interrupt (INT_THRE), receiver threshold level reaching interrupt (INT_RDA), line status interrupt (parity error or framing error or break interrupt) (INT_RLS), receiver buffer time-out interrupt (INT_TOUT), MODEM/Wake-up status interrupt (INT_MODEM), and Buffer error interrupt (INT_BUF_ERR). Interrupt number 12 (vector number is 28) supports UART interrupt. Refer to Nested Vectored Interrupt Controller chapter for System Interrupt Map.

The UART is built-in with a 16-byte transmitter FIFO (TX_FIFO) and a 16-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU and the CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, framing error, break interrupt and buffer error) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing crystal clock input by divisors to produce the clock that transmitter and receiver need. The baud rate equation is Baud Rate = UART_CLK / M * [BRD + 2], where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). The following table lists the equations in the various conditions and the UART baud rate setting table.

Table 5.13-1 UART Baud Rate Setting Table

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	Baud Rate Equation
0	0	0	B	A	UART_CLK / [16 * (A+2)]
1	1	0	B	A	UART_CLK / [(B+1) * (A+2)] , B must >= 8
2	1	1	Don't care	A	UART_CLK / (A+2), A must >=3

Table 5.13-2 UART Baud Rate Setting Table

System clock = 22.1184 MHz			
Baud rate	**Mode0**	**Mode1**	**Mode2**
921600	Not Support	A=0, B=11	A=22
460800	A=1	A=1, B=15 A=2, B=11	A=46
230400	A=4	A=4, B=15 A=6, B=11	A=94
115200	A=10	A=10, B=15	A=190

5.13.2 Features

- Full duplex, asynchronous communications
- Separates receive/transmit 16 bytes entry FIFO for data payloads
- Supports hardware auto flow control/flow control function (CTSn, RTSn) and programmable RTSn flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTSn wake-up function
- Supports 7-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR[DLY] register
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5, 6, 7, 8 character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports 3/16-bit duration for normal mode
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software RTSn control or software GPIO control to control transfer direction

6.2 Features

- A low gate count processor
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - Supports little-endian data accesses
  - Deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model:

    ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low power Idle mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-Maskable Interrupt (NMI) input
  - Supports both level-sensitive and pulse-sensitive interrupt lines
  - Wake-up Interrupt Controller (WIC) with ultra-low power Idle mode support
- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the Debug Access Port DAP (DAP)

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	Min	MAX	UNIT
DC power supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input voltage	VIN	V_{SS}-0.3	V_{DD}+0.3	V
Oscillator frequency	$1/t_{CLCL}$	4	24	MHz
Operating temperature	TA	-40	+85	°C
Storage temperature	TST	-55	+150	°C
Maximum current into VDD		-	120	mA
Maximum current out of VSS			120	mA
Maximum current sunk by a I/O pin			35	mA
Maximum current sourced by a I/O pin			35	mA
Maximum current sunk by total I/O pins			100	mA
Maximum current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
	I_{IDLE16}		1.2		mA	V_{DD} = 3.3V at 22.1184 MHz, all IP Disabled
Operating current Idle mode at 32.768 KHz crystal oscillator	I_{IDLE17}		110		µA	V_{DD} = 5.5V at 32.768 KHz, all IP Enabled
	I_{IDLE18}		107		µA	V_{DD} = 5.5V at 32.768 KHz, all IP Disabled
	I_{IDLE19}		105		µA	V_{DD} = 3.3V at 32.768 KHz, all IP Enabled
	I_{IDLE20}		102		µA	V_{DD} = 3.3V at 32.768 KHz, all IP Disabled
Operating current Idle mode at 10 KHz IRC	I_{IDLE21}		103		µA	V_{DD} = 5.5V at 10 KHz, all IP Enabled
	I_{IDLE22}		102		µA	V_{DD} = 5.5V at 10 KHz, all IP Disabled
	I_{IDLE23}		96		µA	V_{DD} = 3.3V at 10 KHz, all IP Enabled
	I_{IDLE24}		95		µA	V_{DD} = 3.3V at 10 KHz, all IP Disabled
Standby current Power-down mode	I_{PWD1}		10		µA	V_{DD} = 5.0V, CPU STOP All IP and Clock OFF
	I_{PWD2}		5		µA	V_{DD} = 3.3V, CPU STOP All IP and Clock OFF
Standby current Power-down mode with 32.768 KHz crystal enabled	I_{PWD3}		12		µA	V_{DD} = 5.0V, CPU STOP All IP and Clock OFF except 32.768KHz crystal oscillator
	I_{PWD4}		7		µA	V_{DD} = 3.3V, CPU STOP All IP and Clock OFF except 32.768KHz crystal oscillator
Input current P0~P5 (Quasi-bidirectional mode)	I_{IN1}		-50	-60	µA	V_{DD} = 5.5 V, V_{IN} = 0 V or V_{IN} = V_{DD}
Input current at /RESET[1]	I_{IN2}	-55	-45	-30	µA	V_{DD} = 3.3 V, V_{IN} = 0.45 V
Input leakage current PA, PB, PC, PD, PE	I_{LK}	-0.1	-	+0.1	µA	V_{DD} = 5.5 V, 0<V_{IN}<V_{DD}
Logic 1 to 0 transition current PA~PE (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	µA	V_{DD} = 5.5 V, V_{IN}<2.0 V
Input low voltage	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5 V

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Stable time	T_{STBL}			2	μS	CPPx = 1.3V and CPNX = 1.2V

8.4.4 Analog Comparator Reference Voltage (CRV)

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operating voltage	V_{BOD}	2.5		5.5	V	
CRV step size	V_{STEP}		V_{DD}/24		V	VDD = 5V, BOD27 and BOD38 Enabled
CRV output voltage absolute accuracy	A_{CRV}	-5		+5	%	
Unit resistor value	R_{CRV}		2K		ohm	

8.4.5 10-bit ADC

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operating voltage	AV_{DD}	2.7		5.5	V	$AV_{DD} = V_{DD}$
Operating current	I_{ADC}			1	mA	$AV_{DD} = V_{DD} = 5V$, F_{SPS} = 150K
Resolution	R_{ADC}			10	bit	
Reference voltage	V_{REF}		A_{VDD}		V	V_{REF} connected to A_{VDD} in chip
ADC input voltage	V_{IN}	0		V_{REF}	V	
Conversion time	T_{CONV}	6.7			μS	
Sampling rate	F_{SPS}	150K			Hz	V_{DD} = 5V, ADC clock = 6MHz Free running conversion
Integral non-linearity error (INL)	INL			±1	LSB	
Differential non-linearity (DNL)	DNL			±1	LSB	
Gain error	E_G			±2	LSB	
Offset error	E_{OFFSET}			3	LSB	
Absolute error	E_{ABS}			4	LSB	
ADC clock frequency	F_{ADC}	5K		6M	Hz	V_{DD} = 5V
Clock cycle	AD_{CYC}	38			Cycle	
Bang-gap voltage	V_{BG}	1.27	1.35	1.44	V	-40°C ~ +85°C

8.4.6 Flash Memory Characteristics

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Cycling (erase/write) Program memory	N_{CYC}	100			K cycle	
Data retention	T_{RET}	10			years	T_A = +85°C
Erase time of ISP mode	T_{ERASE}	2.3	2.5	2.7	mS	Erase time for one page
Program time of ISP mode	T_{PROG}	57	62	67	μS	Programming time for one word
Program current	I_{PROG}		3.3		mA	V_{DD} = 5.5V

10 REVISION HISTORY

Date	Revision	Changes
Sep 6, 2011	1.00	Initial release
Oct 20, 2011	1.01	1. Change electrical characteristics of comparator, 22MHZ RC oscillator, ADC and band-gap. 2. Add electrical characteristics of Flash memory 3. Change maximum SPI frequency as 12MHz 4. Fix some typos.
Dec 1, 2011	1.02	1. Fix electrical characteristics of 22MHZ RC oscillator 2. Modify all “1XX” description in registers and related figures. 3. Modify 33-pin QFN 5mmx5mm package outline specification. 4. Fix some typos.
Feb 9, 2012	1.03	1. Added the VDD rise rate specification. 2. Revised the minimum ADC clock frequency specification. 3. Revised the minimum and maximum specification of band-gap voltage.