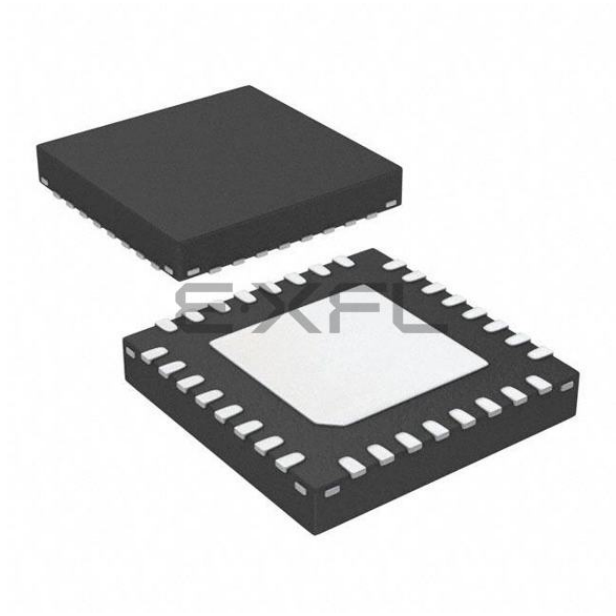

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	29
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini52zan

List of Figures

- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Programmable clocks allowing for versatile rate control
- Supports multiple address recognition (4 slave addresses with mask option)

- ADC (Analog-to-Digital Converter)
  - 10-bit SAR ADC with 150K SPS
  - Up to 8-ch single-end input and one internal input from band-gap
  - Conversion started by software or external pin
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Built-in CRV (comparator reference voltage)
- BOD (Brown-Out Detection) Reset
  - Three programmable threshold levels: 3.8V/2.7V/2.0V (default as 2.0V)
  - Optional BOD interrupt or reset
- 96-bit unique ID
- Operating Temperature: -40℃~85℃
- Packages:
  - Green package (RoHS)
  - LQFP 48-pin (7x7), QFN 33-pin (5x5), QFN 33-pin (4x4)

3.2.2 QFN 33-pin

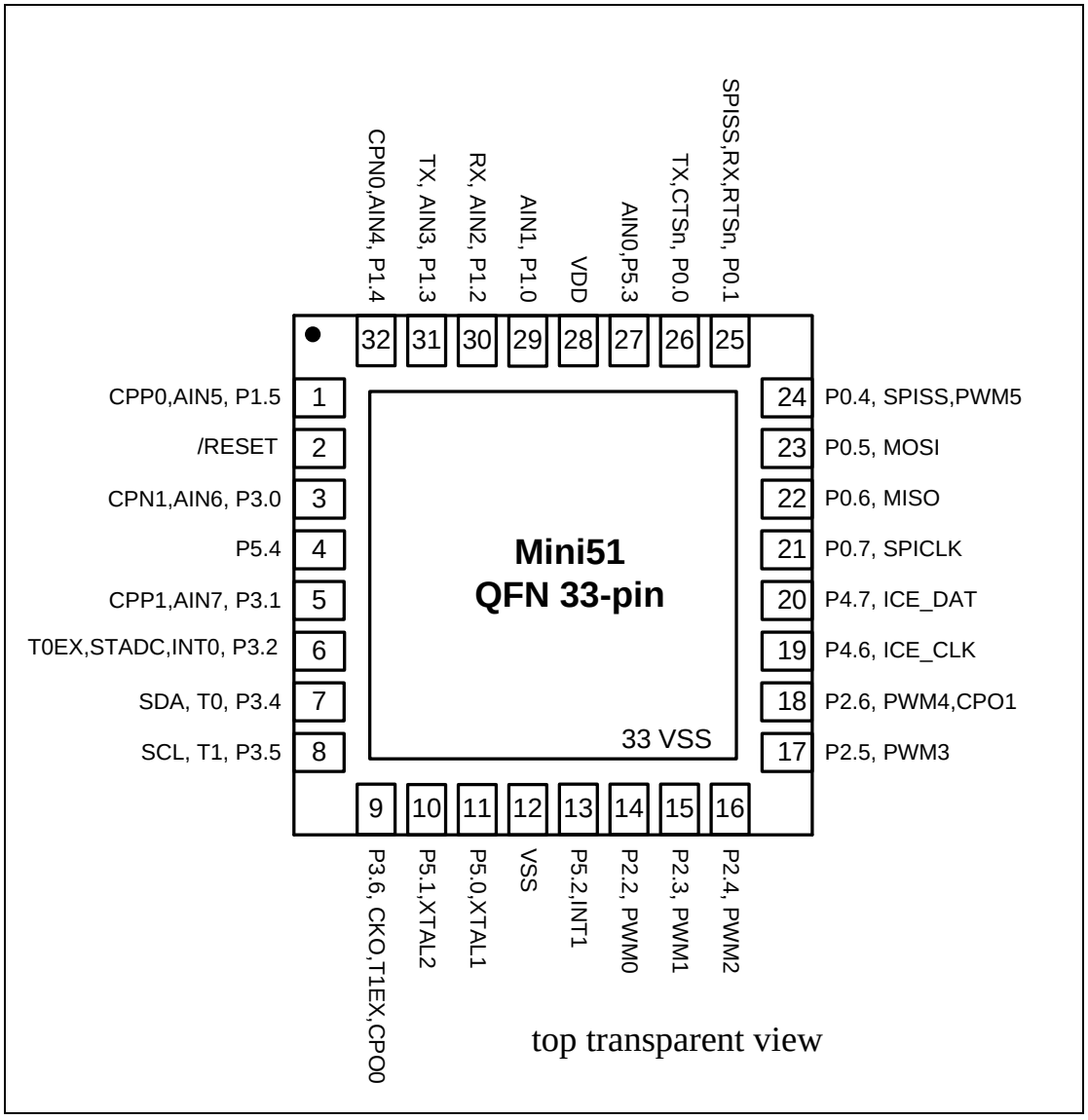


Figure 3.2-2 NuMicro Mini51™ Series QFN 33-pin Assignment

Pin Number		Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin			
14	9	P3.6	**I/O**	Digital GPIO pin
		CPO0	**O**	Analog comparator output pin
		CKO	**O**	Frequency divider output pin
		T1EX	**I**	Timer 1 external capture/reset trigger input pin
15	10	P5.1	**I/O**	Digital GPIO pin
		XTAL2	**O**	The output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.
16	11	P5.0	**I/O**	Digital GPIO pin
		XTAL1	**I**	The input pin to the internal inverting amplifier. The system clock could be from external crystal or resonator.
17	12	VSS	**P**	Ground pin for digital circuit
	33			
18		LDO_CAP	**P**	LDO output pin
19		P5.5	**I/O**	Digital GPIO pin User program must enable pull-up resistor in the QFN-33 package.
20	13	P5.2	**I/O**	Digital GPIO pin
		INT1	**I**	External interrupt 1 input pin
21		NC		Not connected
22	14	P2.2	**I/O**	Digital GPIO pin
		PWM0	**O**	PWM0 output of PWM unit
23	15	P2.3	**I/O**	Digital GPIO pin
		PWM1	**O**	PWM1 output of PWM unit
24	16	P2.4	**I/O**	Digital GPIO pin
		PWM2	**O**	PWM2 output of PWM unit
25	17	P2.5	**I/O**	Digital GPIO pin
		PWM3	**O**	PWM3 output of PWM unit
26	18	P2.6	**I/O**	Digital GPIO pin
		PWM4	**O**	PWM4 output of PWM unit
		CPO1	**O**	Analog comparator output pin
27		NC		Not connected

Pin Number		Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin			
28		NC		Not connected
29	19	P4.6	**I/O**	Digital GPIO pin
		ICE_CLK	**I**	Serial wired debugger clock pin
30	20	P4.7	**I/O**	Digital GPIO pin
		ICE_DAT	**I/O**	Serial wired debugger data pin
31		NC		Not connected
32	21	P0.7	**I/O**	Digital GPIO pin
		SPICLK	**I/O**	SPI serial clock pin
33	22	P0.6	**I/O**	Digital GPIO pin
		MISO	**I/O**	SPI MISO (master in/slave out) pin
34	23	P0.5	**I/O**	Digital GPIO pin
		MOSI	**O**	SPI MOSI (master out/slave in) pin
35	24	P0.4	**I/O**	Digital GPIO pin
		SPISS	**I/O**	SPI slave select pin
		PWM5	**O**	PWM5 output of PWM unit
36		NC		Not connected
37	25	P0.1	**I/O**	Digital GPIO pin
		RTSn	**O**	UART RTS pin
		RX	**I**	UART data receiver input pin
		SPISS	**I/O**	SPI slave select pin
38	26	P0.0	**I/O**	Digital GPIO pin
		CTSn	**I**	UART CTS pin
		TX	**O**	UART transmitter output pin
39		NC		Not connected
40		NC		Not connected
41	27	P5.3	**I/O**	Digital GPIO pin
		AIN0	**AI**	ADC analog input pin
42	28	VDD	**P**	Power supply for digital circuit
43		AVDD	**P**	Power supply for analog circuit
44	29	P1.0	**I/O**	Digital GPIO pin

5.3 System Manager

5.3.1 Overview

The following functions are included in the system manager section:

- System Memory Map
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System management registers for product ID
- System management registers for chip and module functional reset and multi-function pin control
- Brown-out and chip miscellaneous Control Register
- Combined peripheral interrupt source identify

5.3.2 System Reset

The system reset includes one of the following as the event occurs. For these reset events flags can be read by RSTSRC register.

- Power-On Reset (POR)
- Low level on the /RESET pin
- Watchdog Time-out Reset (WDT)
- Brown-out Detected Reset (BOD)
- Cortex™-M0 CPU Reset
- Software one shot Reset

5.3.3 System Power Distribution

In this device, the power distribution is divided into three segments.

- Analog power from AVDD and AVSS supplies power for analog module operation
- Digital power from VDD and VSS supplies power to the internal regulator which provides a fixed 1.8V power for digital operation and I/O pins
- Built-in capacitor for internal voltage regulator

The output of internal voltage regulator, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. **錯誤! 找不到參照來源。** shows the power architecture of this device.

5.4.3 System Clock and SysTick Clock

The system clock has 3 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown below.

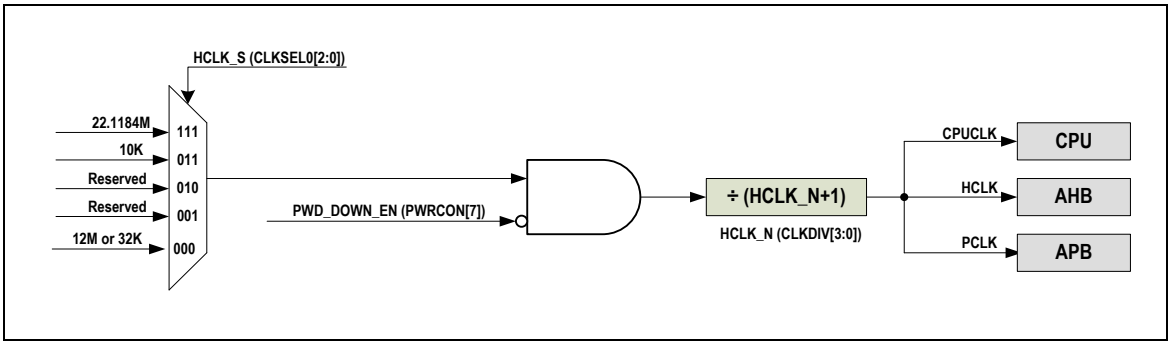


Figure 5.4-2 System Clock Block Diagram

The clock source of SysTick in Cortex-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in **錯誤! 找不到參照來源。**.

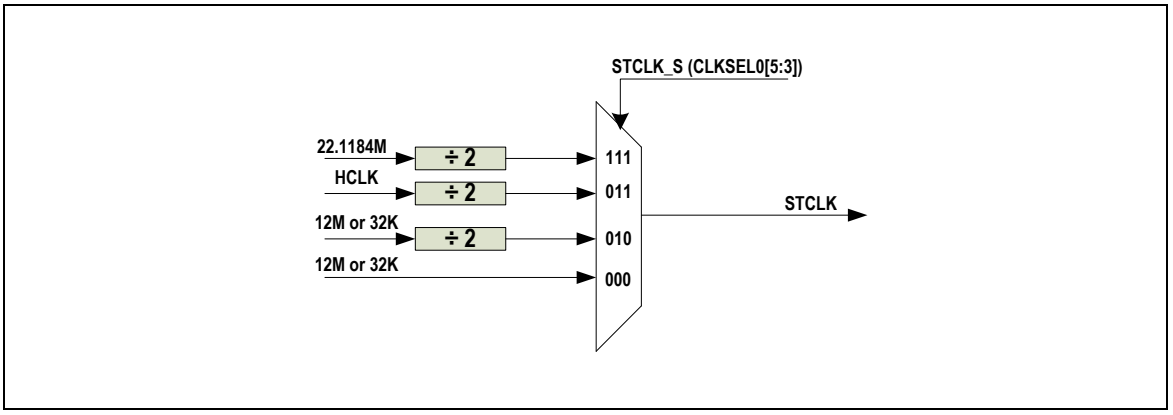


Figure 5.4-3 SysTick Clock Control Block Diagram

5.4.7 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to P3.6. Therefore, there are 16 options of power-of-2 divided clocks with the frequency from Fin/21 to Fin/217 where Fin is input clock frequency to the clock divider.

The output formula is Fout = Fin/2(N+1), where Fin is the input clock frequency, Fout is the clock divider output frequency and N is the 4-bit value in FREQDIV.FSEL[3:0].

When FREQDIV.FDIV_EN[4] is set to high, the rising transition will reset the chained counter and starts counting. When FREQDIV.FDIV_EN[4] is written with zero, the chained counter continuously runs until the divided clock reaches low state and stays in low state.

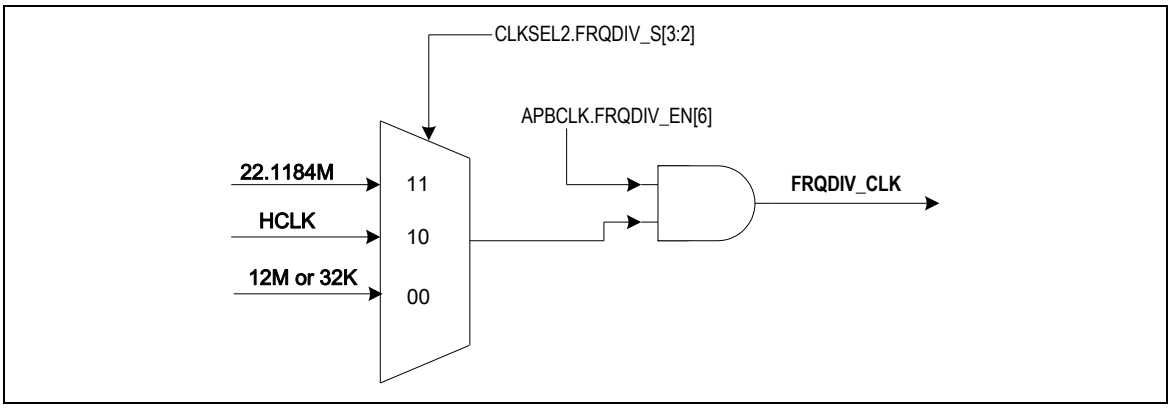


Figure 5.4-6 Clock Source of Frequency Divider

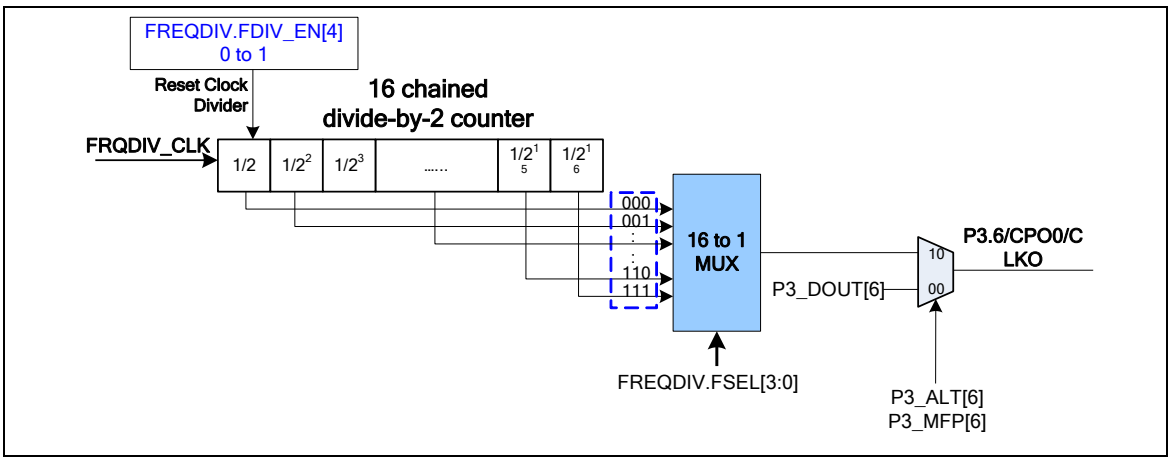


Figure 5.4-7 Block Diagram of Frequency Divider

5.7 Flash Memory Controller (FMC)

5.7.1 Overview

The NuMicro Mini51™ series is equipped with 4K/8K/16K bytes on chip embedded Flash EPROM for application program memory (APROM) that can be updated through ISP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip powered on Cortex-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, the NuMicro Mini51™ series also provides DATA Flash Region, where the data flash is shared with original program memory and its start address is configurable and defined by user in Config1. The data flash size is defined by user depending on the application request.

5.7.2 Features

- Compatible with AHB interface
- Running up to 24 MHz with zero wait state for discontinuous address read access
- 4K/8K/16KB application program memory (APROM)
- 2KB in system programming (ISP) loader program memory (LDROM)
- Programmable data flash start address and memory size with 512 bytes page erase unit
- In System Program (ISP) to update on chip Flash EPROM

5.10 Enhanced PWM Generator

5.10.1 Overview

The NuMicro Mini51™ series has built one PWM unit which is specially designed for motor driving control applications. The PWM unit supports 6 PWM generators which can be configured as 6 independent PWM outputs, PWM0~PWM5, or as 3 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5) with 3 programmable dead-zone generators.

Each PWM generator shares the 8-bit prescaler, clock divider providing 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16). Each PWM output has independent 16-bit counter for PWM period control, and 16-bit comparators for PWM duty control. The 6 PWM generators provide six independent PWM interrupt flags which are set by hardware when the corresponding PWM period counter comparison matched. Each PWM interrupt source with its corresponding enable bit can request PWM interrupt. The PWM generators can be configured as One-shot mode to produce only one PWM cycle signal or Auto-reload mode to output PWM waveform continuously.

5.10.2 Features

The PWM unit supports the following features:

- Six independent 16-bit PWM duty control units with maximum 6 port pins:
  - 6 independent PWM outputs – PWM0, PWM1, PWM2, PWM3, PWM4, and PWM5
  - 3 complementary PWM pairs, with each pin in a pair mutually complement to each other and capable of programmable dead-zone insertion – (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5)
  - 3 synchronous PWM pairs, with each pin in a pair in-phase – (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5)
- Group control bit – PWM2 and PWM4 are synchronized with PWM0
- One-shot (only support edge alignment mode) or Auto-reload mode PWM
- Up to 16-bit resolution
- Supports Edge-aligned and Center-aligned mode
- Programmable dead-zone insertion between complementary paired PWMs
- Each pin of PWM0 to PWM5 has independent polarity setting control
- Hardware fault brake protections
  - Two Interrupt source types:
    - Synchronously requested at PWM frequency when down counter comparison matched (edge- and center-aligned mode) or underflow (edge-aligned mode)
    - Requested when external fault brake asserted
      - BKP0: EINT0
      - BKP1: EINT1 or CPO0
- The PWM signals before polarity control stage are defined in view of positive logic. Whether the PWM ports are active high or active low is controlled by the polarity control register.

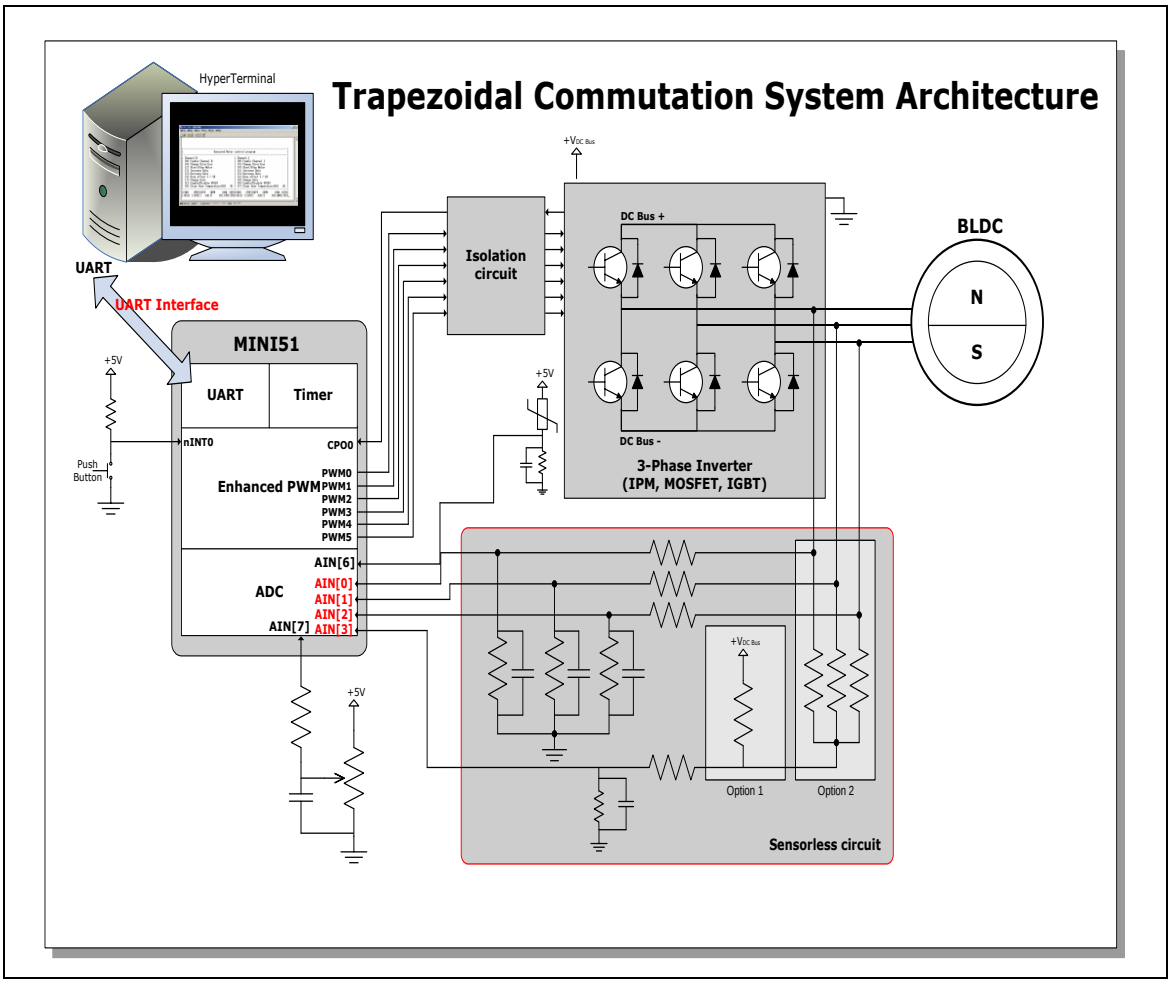


Figure 5.10-1 Application Circuit Diagram

5.11 Serial Peripheral Interface (SPI) Controller

5.11.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol which operates in full duplex mode. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. NuMicro Mini51™ series contain one set of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. SPI controller can be set as a master; it also can be set as a slave controlled by an off-chip master device.

5.11.2 Features

- Supports Master or Slave mode operation
- MSB or LSB first transfer
- Byte or word Suspend mode
- Variable output serial clock frequency in Master mode
- Supports two programmable serial clock frequencies in Master mode

5.13.2 Features

- Full duplex, asynchronous communications
- Separates receive/transmit 16 bytes entry FIFO for data payloads
- Supports hardware auto flow control/flow control function (CTSn, RTSn) and programmable RTSn flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTSn wake-up function
- Supports 7-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR[DLY] register
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5, 6, 7, 8 character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports 3/16-bit duration for normal mode
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software RTSn control or software GPIO control to control transfer direction

6 ARM® CORTEX™-M0 CORE

6.1 Overview

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processors. The profile supports two modes - Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset and can be entered as a result of an exception return. 錯誤! 找不到參照來源。 shows the functional controller of the processor.

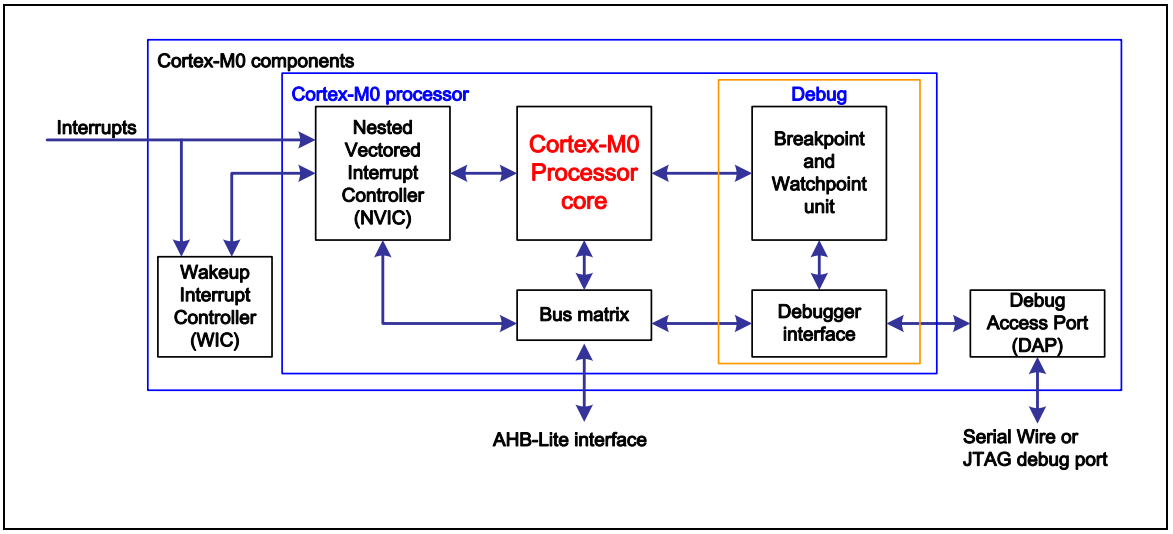
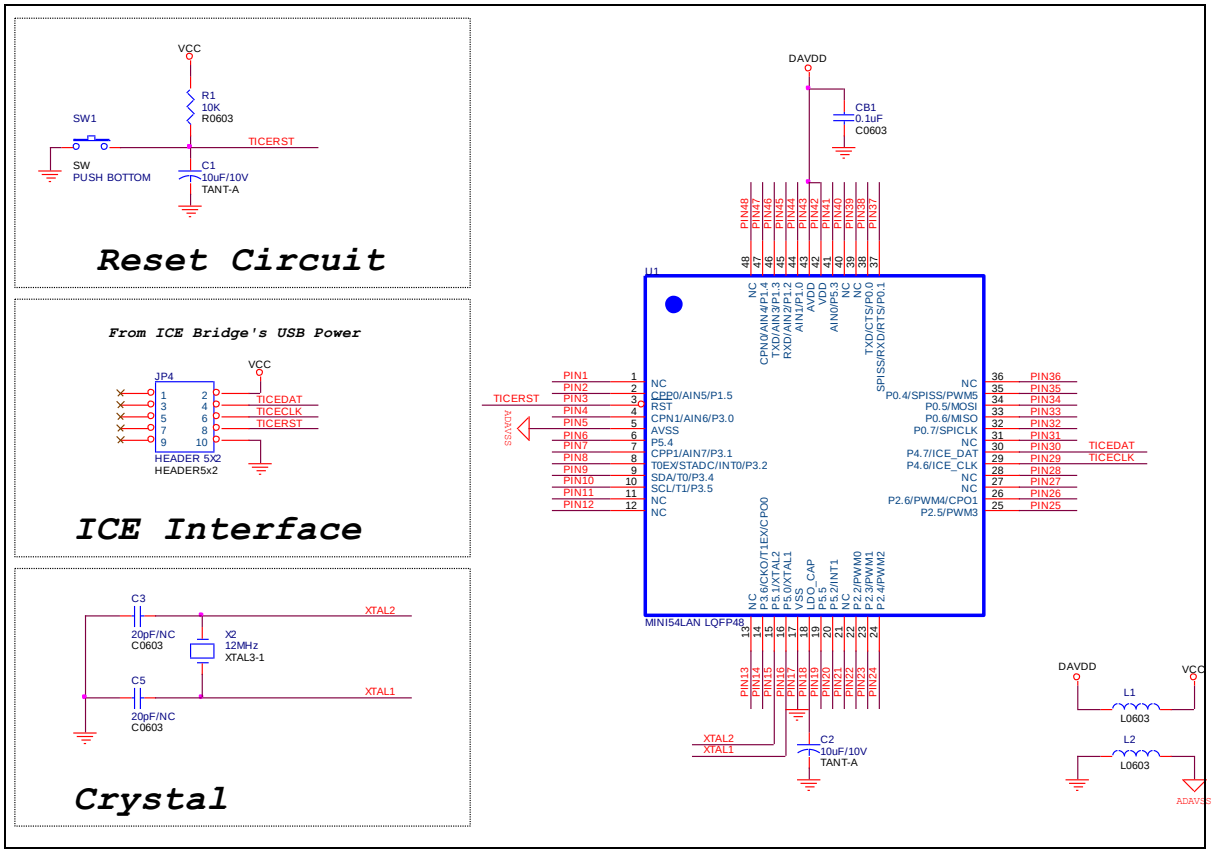


Figure 6.1-1 Functional Block Diagram

7 APPLICATION CIRCUIT



8.4 Analog Characteristics

(V_{DD}-V_{SS} = 5.0V, TA = 25°C, FOSC = 24 MHz unless otherwise specified.)

8.4.1 Brown-Out Reset (BOD)

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operating voltage	V_{BOD}	2.0		5.5	V	
Operating current	I_{BOD}		5	15	μA	V_{DD} = 5V BOD27 and BOD38 Enabled
BOD38 detection level	V_{B38dt}	3.6	3.8	4.0	V	25°C
BOD27 detection level	V_{B27dt}	2.6	2.7	2.8	V	25°C

8.4.2 Low Voltage Reset (LVR)

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operating voltage	V_{BOD}	2.0		5.5	V	
Operating current	I_{BOD}		1	2	μA	
Detection level	V_{LVR}		2.0		V	25°C
LVR always enabled		1.6	2.0	2.4	V	-40°C ~ +85°C

8.4.3 Analog Comparator

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operating voltage	V_{BOD}	2.5	3.3	5.5	V	
Operating current	I_{CMP}		40	80	μA	
Input offset voltage	V_{OFFSET}		10	20	mV	
Output swing voltage	V_{swin}	0.2		V_{DD}-0.2	V	
Input common mode range (V_{CM})	V_{CM}	0.1		V_{DD}-0.1	V	
DC gain	G_{DC}		70		dB	
Propagation delay	T_{PDLY}		200		ns	V_{CM} = 1.2V The difference voltage in CPPx and CPNx is 0.1V
Hysteresis	V_{HYS}		±10		mV	One bit control W/O and W. hysteresis @V_{CM} = 0.2V ~ VDD-0.2V

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Stable time	T_{STBL}			2	μS	CPPx = 1.3V and CPNX = 1.2V

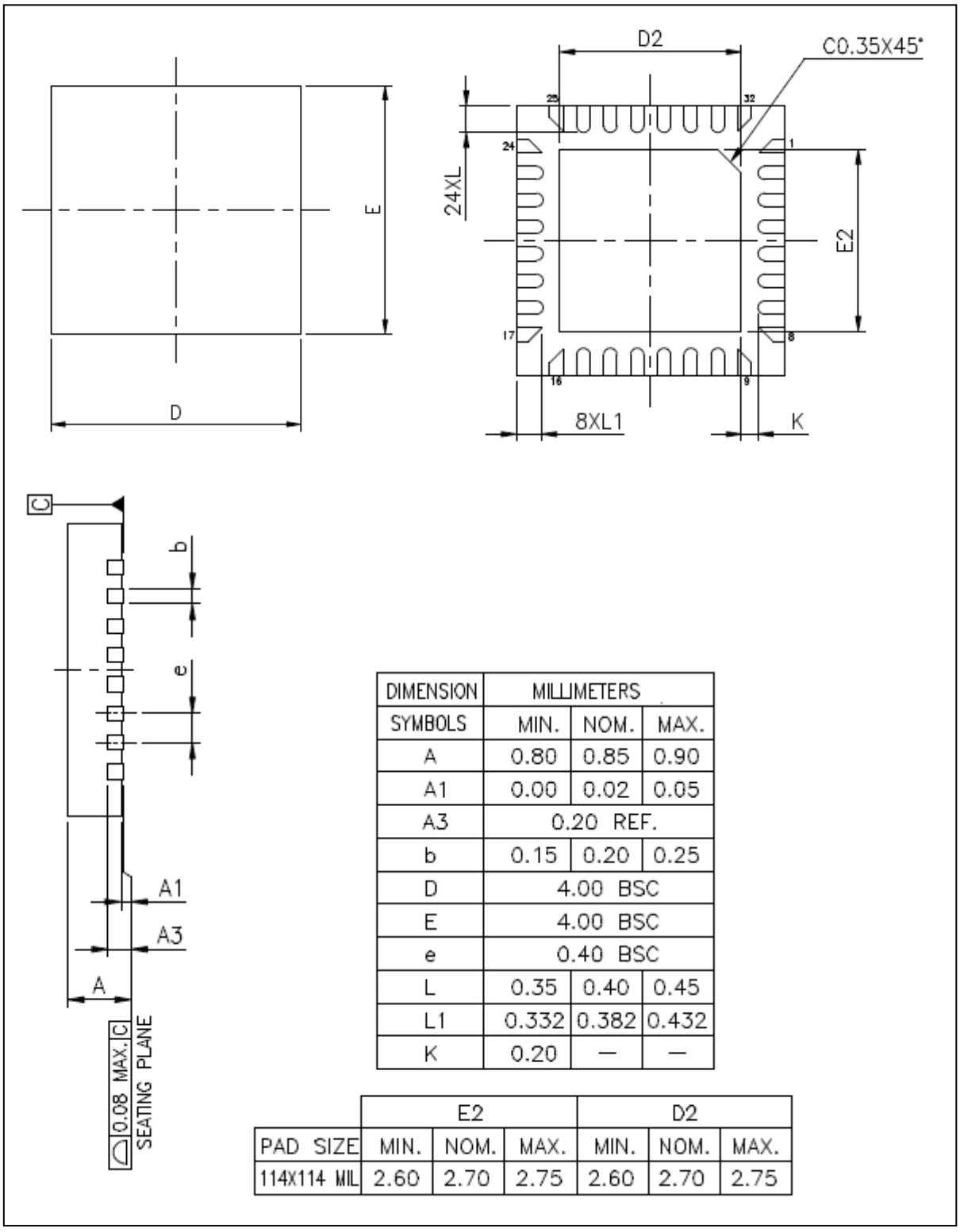
8.4.4 Analog Comparator Reference Voltage (CRV)

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operating voltage	V_{BOD}	2.5		5.5	V	
CRV step size	V_{STEP}		V_{DD}/24		V	VDD = 5V, BOD27 and BOD38 Enabled
CRV output voltage absolute accuracy	A_{CRV}	-5		+5	%	
Unit resistor value	R_{CRV}		2K		ohm	

8.4.5 10-bit ADC

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operating voltage	AV_{DD}	2.7		5.5	V	$AV_{DD} = V_{DD}$
Operating current	I_{ADC}			1	mA	$AV_{DD} = V_{DD} = 5V$, F_{SPS} = 150K
Resolution	R_{ADC}			10	bit	
Reference voltage	V_{REF}		A_{VDD}		V	V_{REF} connected to A_{VDD} in chip
ADC input voltage	V_{IN}	0		V_{REF}	V	
Conversion time	T_{CONV}	6.7			μS	
Sampling rate	F_{SPS}	150K			Hz	V_{DD} = 5V, ADC clock = 6MHz Free running conversion
Integral non-linearity error (INL)	INL			±1	LSB	
Differential non-linearity (DNL)	DNL			±1	LSB	
Gain error	E_G			±2	LSB	
Offset error	E_{OFFSET}			3	LSB	
Absolute error	E_{ABS}			4	LSB	
ADC clock frequency	F_{ADC}	5K		6M	Hz	V_{DD} = 5V
Clock cycle	AD_{CYC}	38			Cycle	
Bang-gap voltage	V_{BG}	1.27	1.35	1.44	V	-40°C ~ +85°C

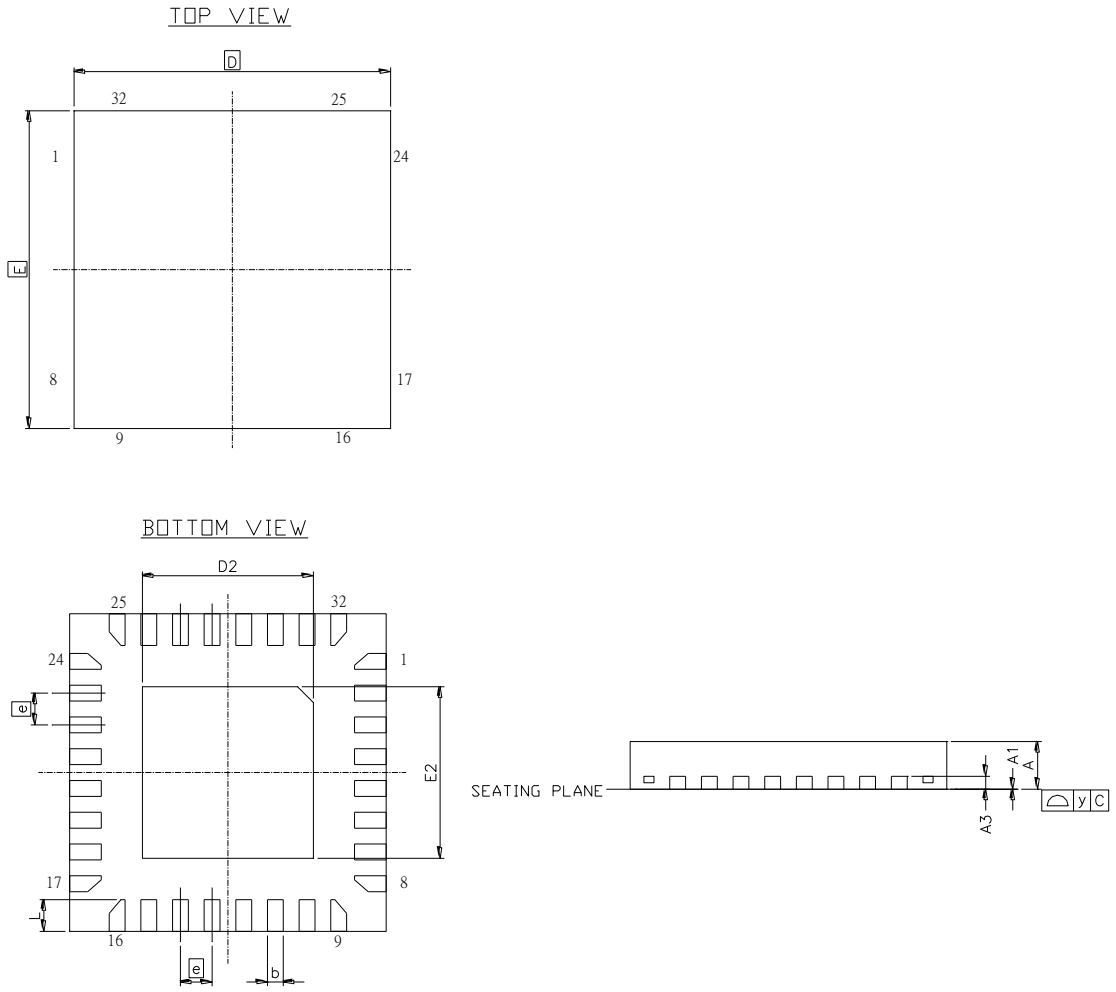
9.2 33-pin QFN (4mm x 4mm)



DIMENSION	MILLIMETERS		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
L	0.35	0.40	0.45
L1	0.332	0.382	0.432
K	0.20	—	—

	E2			D2		
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
114X114 MIL	2.60	2.70	2.75	2.60	2.70	2.75

9.3 33-pin QFN (5mm x 5mm)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
E	5.00 BSC			0.197 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		

SYMBOL	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
DIMENSION (MM)	3.4	3.5	3.6	3.4	3.5	3.6

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