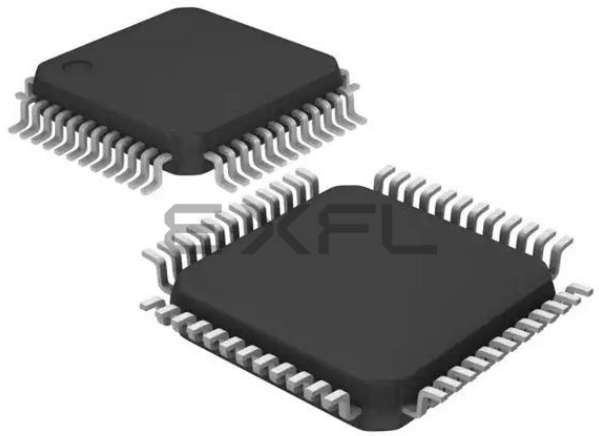

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	30
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini54lan

3.2.2 QFN 33-pin

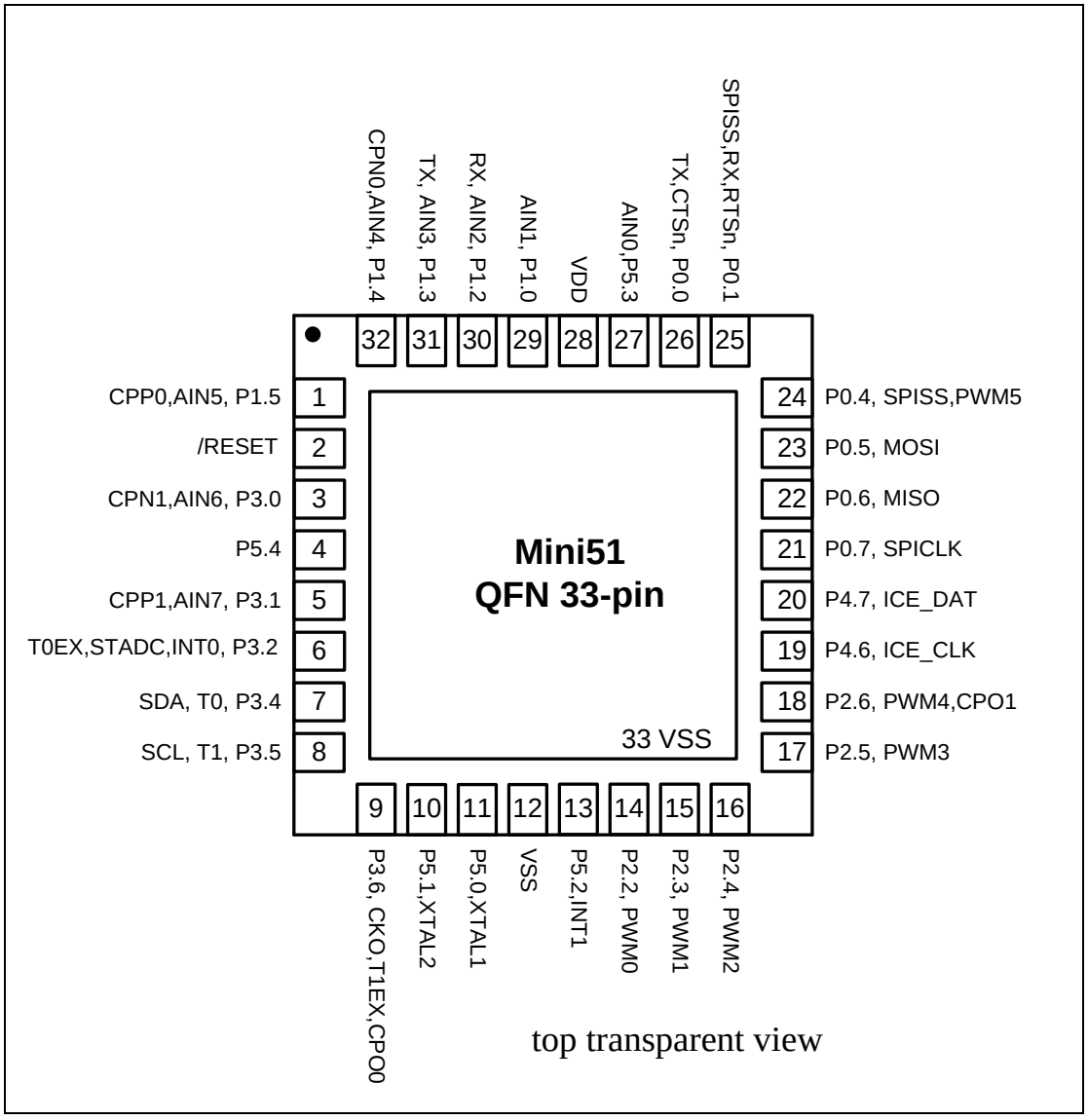


Figure 3.2-2 NuMicro Mini51™ Series QFN 33-pin Assignment

Pin Number		Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin			
14	9	P3.6	**I/O**	Digital GPIO pin
		CPO0	**O**	Analog comparator output pin
		CKO	**O**	Frequency divider output pin
		T1EX	**I**	Timer 1 external capture/reset trigger input pin
15	10	P5.1	**I/O**	Digital GPIO pin
		XTAL2	**O**	The output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.
16	11	P5.0	**I/O**	Digital GPIO pin
		XTAL1	**I**	The input pin to the internal inverting amplifier. The system clock could be from external crystal or resonator.
17	12	VSS	**P**	Ground pin for digital circuit
	33			
18		LDO_CAP	**P**	LDO output pin
19		P5.5	**I/O**	Digital GPIO pin User program must enable pull-up resistor in the QFN-33 package.
20	13	P5.2	**I/O**	Digital GPIO pin
		INT1	**I**	External interrupt 1 input pin
21		NC		Not connected
22	14	P2.2	**I/O**	Digital GPIO pin
		PWM0	**O**	PWM0 output of PWM unit
23	15	P2.3	**I/O**	Digital GPIO pin
		PWM1	**O**	PWM1 output of PWM unit
24	16	P2.4	**I/O**	Digital GPIO pin
		PWM2	**O**	PWM2 output of PWM unit
25	17	P2.5	**I/O**	Digital GPIO pin
		PWM3	**O**	PWM3 output of PWM unit
26	18	P2.6	**I/O**	Digital GPIO pin
		PWM4	**O**	PWM4 output of PWM unit
		CPO1	**O**	Analog comparator output pin
27		NC		Not connected

Pin Number		Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin			
28		NC		Not connected
29	19	P4.6	**I/O**	Digital GPIO pin
		ICE_CLK	**I**	Serial wired debugger clock pin
30	20	P4.7	**I/O**	Digital GPIO pin
		ICE_DAT	**I/O**	Serial wired debugger data pin
31		NC		Not connected
32	21	P0.7	**I/O**	Digital GPIO pin
		SPICLK	**I/O**	SPI serial clock pin
33	22	P0.6	**I/O**	Digital GPIO pin
		MISO	**I/O**	SPI MISO (master in/slave out) pin
34	23	P0.5	**I/O**	Digital GPIO pin
		MOSI	**O**	SPI MOSI (master out/slave in) pin
35	24	P0.4	**I/O**	Digital GPIO pin
		SPISS	**I/O**	SPI slave select pin
		PWM5	**O**	PWM5 output of PWM unit
36		NC		Not connected
37	25	P0.1	**I/O**	Digital GPIO pin
		RTSn	**O**	UART RTS pin
		RX	**I**	UART data receiver input pin
		SPISS	**I/O**	SPI slave select pin
38	26	P0.0	**I/O**	Digital GPIO pin
		CTSn	**I**	UART CTS pin
		TX	**O**	UART transmitter output pin
39		NC		Not connected
40		NC		Not connected
41	27	P5.3	**I/O**	Digital GPIO pin
		AIN0	**AI**	ADC analog input pin
42	28	VDD	**P**	Power supply for digital circuit
43		AVDD	**P**	Power supply for analog circuit
44	29	P1.0	**I/O**	Digital GPIO pin

5.1.2 System Memory Map

The memory locations assigned to each on-chip controllers are shown in the following table.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_3FFF	FLASH_BA	Flash Memory Space (16 KB)
0x2000_0000 – 0x2000_07FF	SRAM_BA	SRAM Memory Space (2 KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GP_BA	GPIO Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB1 Controllers Space (0x4000_0000 – 0x401F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C_BA	I^2C Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI_BA	SPI Control Registers
0x4004_0000 – 0x4004_3FFF	PWM_BA	PWM Control Registers
0x4005_0000 – 0x4005_3FFF	UART_BA	UART Control Registers
0x400D_0000 – 0x400D_3FFF	CMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
System Controllers Space (0xE000_E000 – 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	Nested Vectored Interrupt Control Registers
0xE000_ED00 – 0xE000_ED8F	SCB_BA	System Control Block Registers

Table 5.1-1 Address Space Assignments for On-Chip Modules

Exception Number	IRQ Number (Bit in Interrupt Registers)	Exception Name	Source IP	Exception Description	Power-down Wake-up
30	14	**SPI_INT**	SPI	SPI interrupt	No
31	15	**-**	-	-	
32	16	**GP5_INT**	GPIO	External signal interrupt from GPIO group P5 except P5.2	Yes
33	17	**HFIRC_TRIM_INT**	HFIRC	HFIRC trim interrupt	No
34	18	**I2C_INT**	I^2C	I^2C interrupt	No
35 ~ 40	19 ~ 24	**-**	-	-	
41	25	**ACMP_INT**	ACMP	Analog Comparator 0 or 1 interrupt	Yes
42 ~ 43	26 ~ 27	**-**	-	-	
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state	Yes
45	29	**ADC_INT**	ADC	ADC interrupt	No
46 ~ 47	30 ~ 31	**-**	-	-	

Table 5.2-2 System Interrupt Map

5.2.4 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table based address is fixed at 0x0000_0000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with the exception handler entry as illustrated in the previous section.

Vector Table Word Offset (Bytes)	Description
0x00	Initial Stack Pointer Value
Exception Number × 0x04	Exception Entry Pointer using that Exception Number

Table 5.2-3 Vector Table Format

5.3.4 Memory Mapping Table

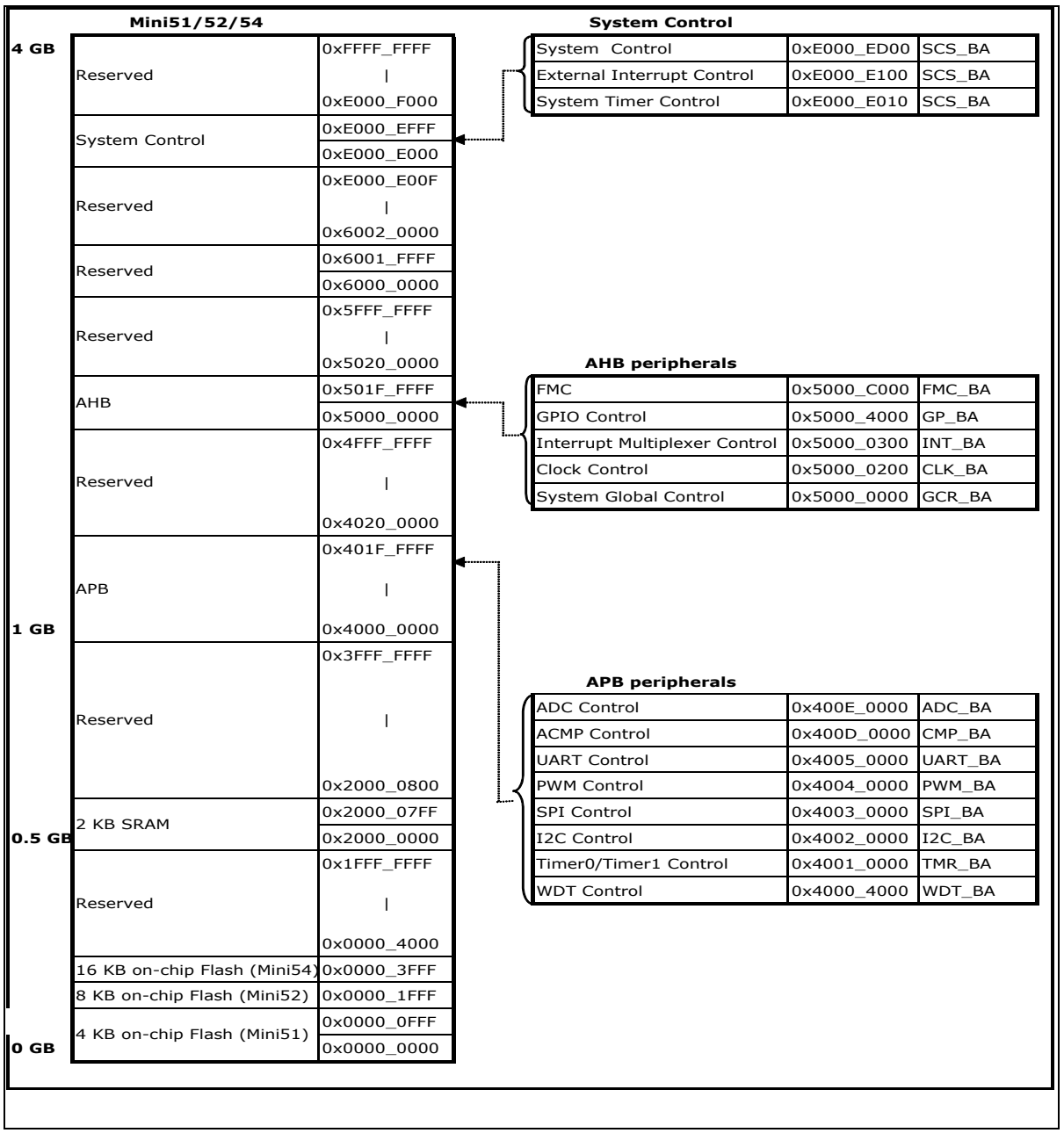


Table 5.3-1 Memory Mapping Table

5.4 Clock Controller

5.4.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a 4-bit clock divider. The chip will not enter Power-down mode until CPU sets the power-down enable bit (PWR_DOWN_EN) and Cortex-M0 core executes the WFI instruction. After that, the chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the external crystal and internal 22.1184 MHz oscillator to reduce the overall system power consumption.

5.4.2 Clock Generator

The clock generator consists of 3 sources which are listed below:

- One external 12 MHz (HXT) or 32 KHz (LXT) crystal
- One internal 22.1184 MHz RC oscillator (HIRC)
- One internal 10 KHz oscillator (LIRC)

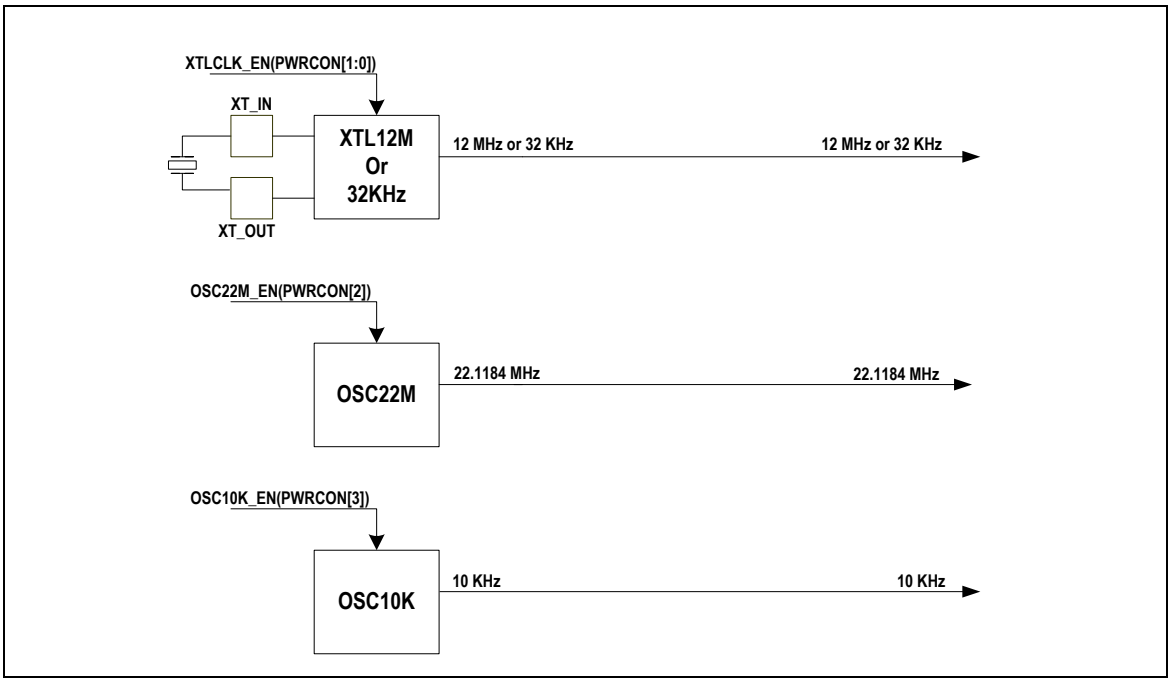


Figure 5.4-1 Clock Generator Block Diagram

5.4.5 Peripheral Clock Source Selection

The peripheral clock has different clock source switch settings depending on different peripherals. Please refer to the CLKSEL1 and APBCLK register description in section 錯誤! 找不到參照來源。.

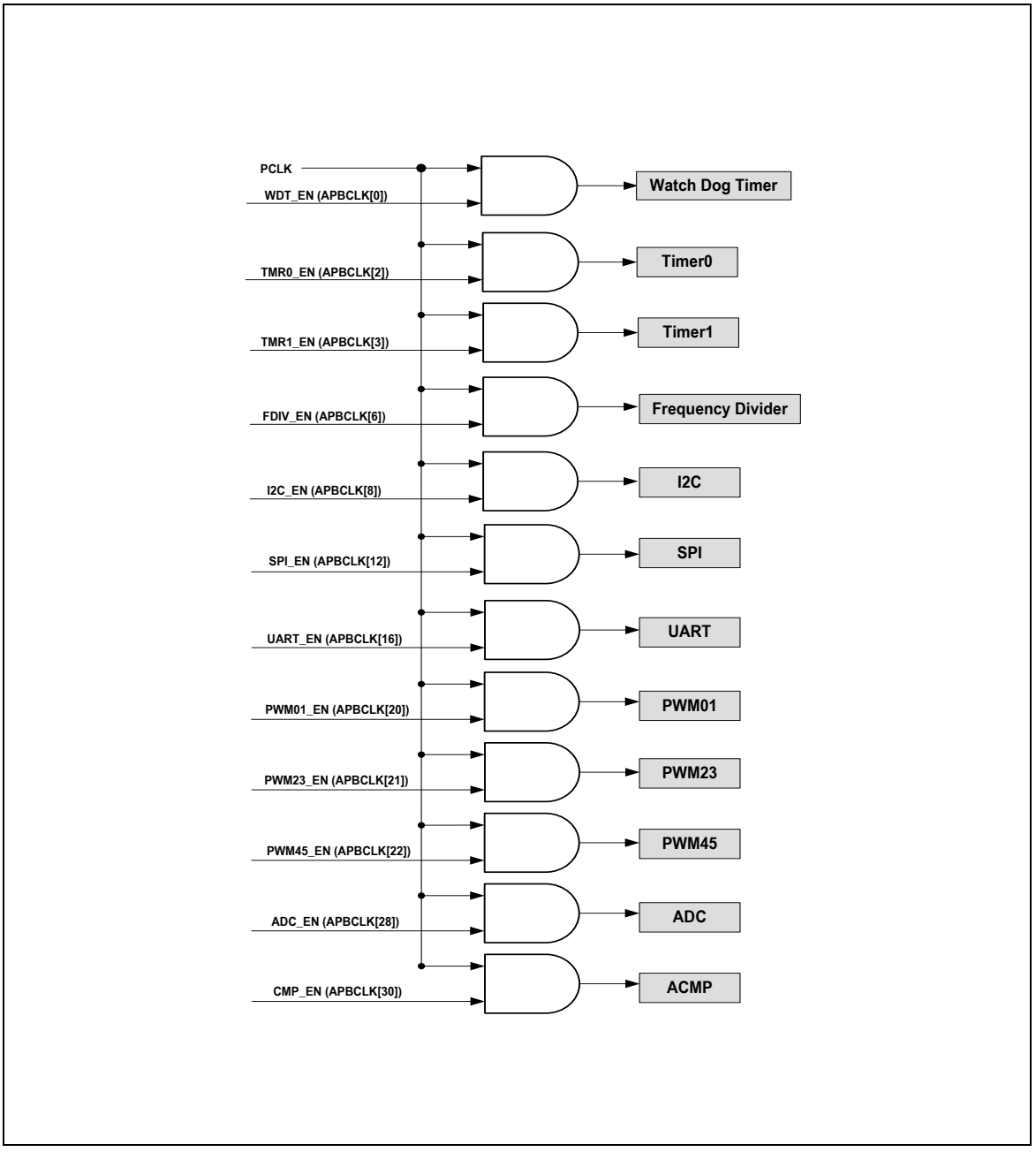


Figure 5.4-5 Peripherals Clock Source Selection for PCLK

5.4.6 Power-down Mode Clock

When entering Power-down mode, some clock sources and peripheral clocks and system clocks will be disabled. Some clock sources and peripheral clocks are still active in Power-down mode.

Clocks that still be kept active are listed below.

- Clock Generator
  - Internal 10 KHz RC oscillator (LIRC) clock
  - External 32.768 KHz crystal oscillator (LXT) clock (If PD_32K = “1” and XTLCLK_EN[1:0] = “10”)
- Peripherals Clock (When these IP adopt 10 KHz as clock source)
  - Watchdog Clock
  - Timer 0/1 Clock

5.4.7 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to P3.6. Therefore, there are 16 options of power-of-2 divided clocks with the frequency from Fin/21 to Fin/217 where Fin is input clock frequency to the clock divider.

The output formula is Fout = Fin/2(N+1), where Fin is the input clock frequency, Fout is the clock divider output frequency and N is the 4-bit value in FREQDIV.FSEL[3:0].

When FREQDIV.FDIV_EN[4] is set to high, the rising transition will reset the chained counter and starts counting. When FREQDIV.FDIV_EN[4] is written with zero, the chained counter continuously runs until the divided clock reaches low state and stays in low state.

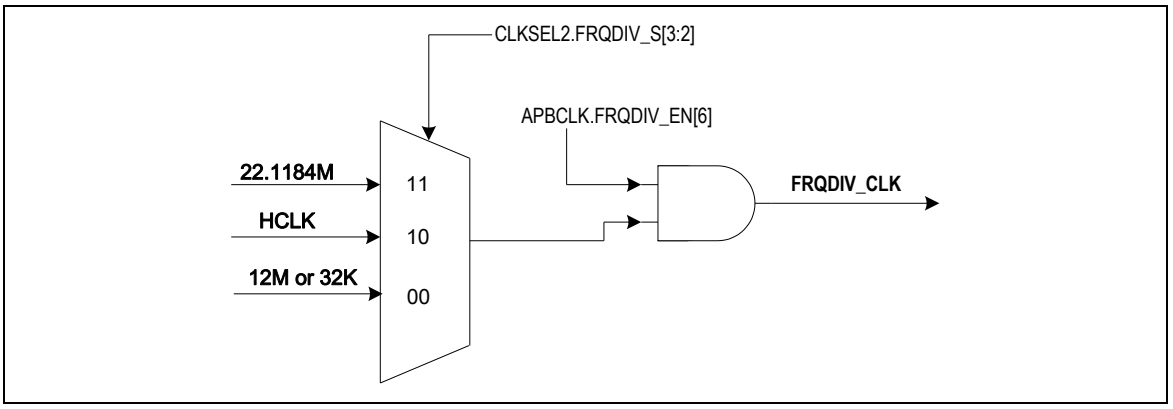


Figure 5.4-6 Clock Source of Frequency Divider

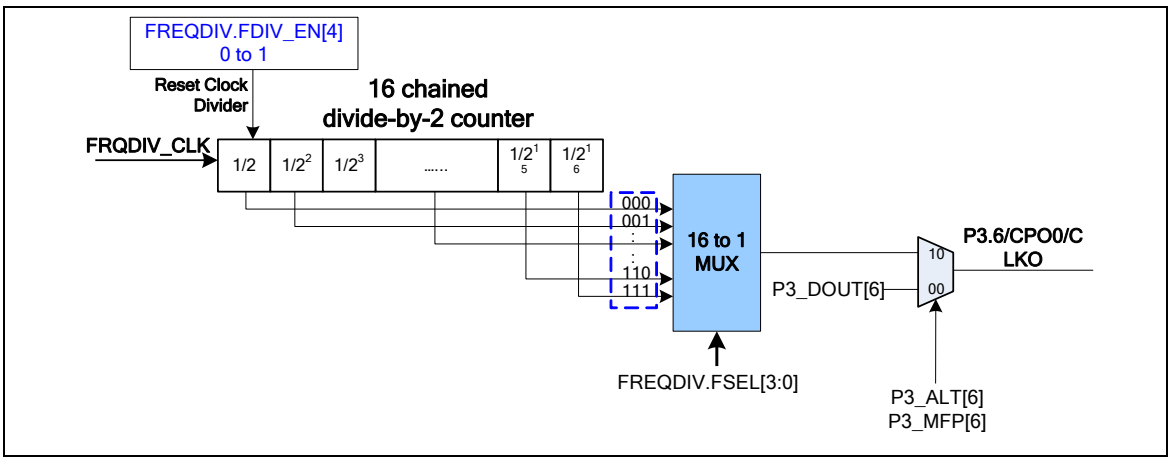


Figure 5.4-7 Block Diagram of Frequency Divider

5.8 General Purpose I/O

5.8.1 Overview

There are 30 General Purpose I/O pins shared with special feature functions in this MCU. The 30 pins are arranged in 6 ports named P0, P1, P2, P3, P4 and P5. Each of the 30 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each I/O pin can be independently software configured as input, output, open-drain, or Quasi-bidirectional mode. After reset, the I/O type of all pins stay in input mode and port data register Px_DOUT[n] resets to “1”. For Quasi-bidirectional mode, each I/O pin is equipped with a very weak individual pull-up resistor about 110KΩ ~ 300KΩ for VDD from 5.0V to 2.5V.

5.8.2 Features

- Four I/O modes:
  - Quasi bi-direction
  - Push-Pull output
  - Open-Drain output
  - Input-only with high impendence
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- High driver and high sink IO mode support

5.9 I²C Serial Interface Controller (Master/Slave)

5.9.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. Serial 8-bit oriented bi-directional data transfers can be made up 1.0 Mbps.

Data is transferred between a master and a slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more detailed I²C BUS Timing.

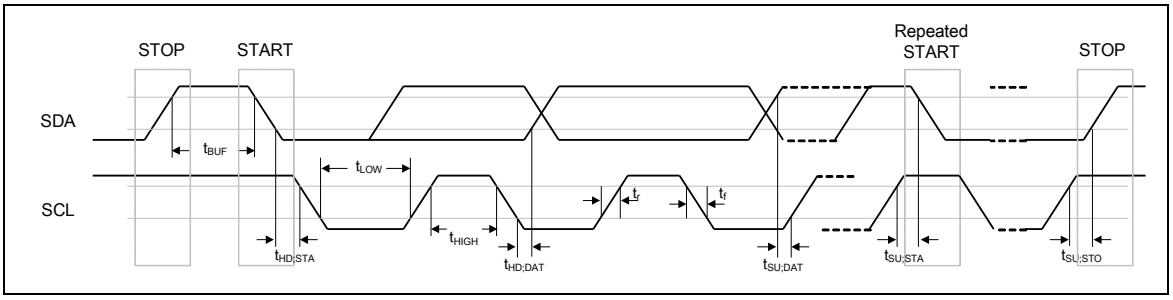


Figure 5.9-1 Bus Timing

The device's on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit ENSI in I2CON should be set to "1". The I²C hardware interfaces to the I²C bus via two pins: SDA (P3.4, serial data line) and SCL (P3.5, serial clock line). Since the pull-up resistor is needed for Pin P3.4 and P3.5 for I²C operation as these are open-drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

5.9.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Supports Master/Slave mode
- Bi-directional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer

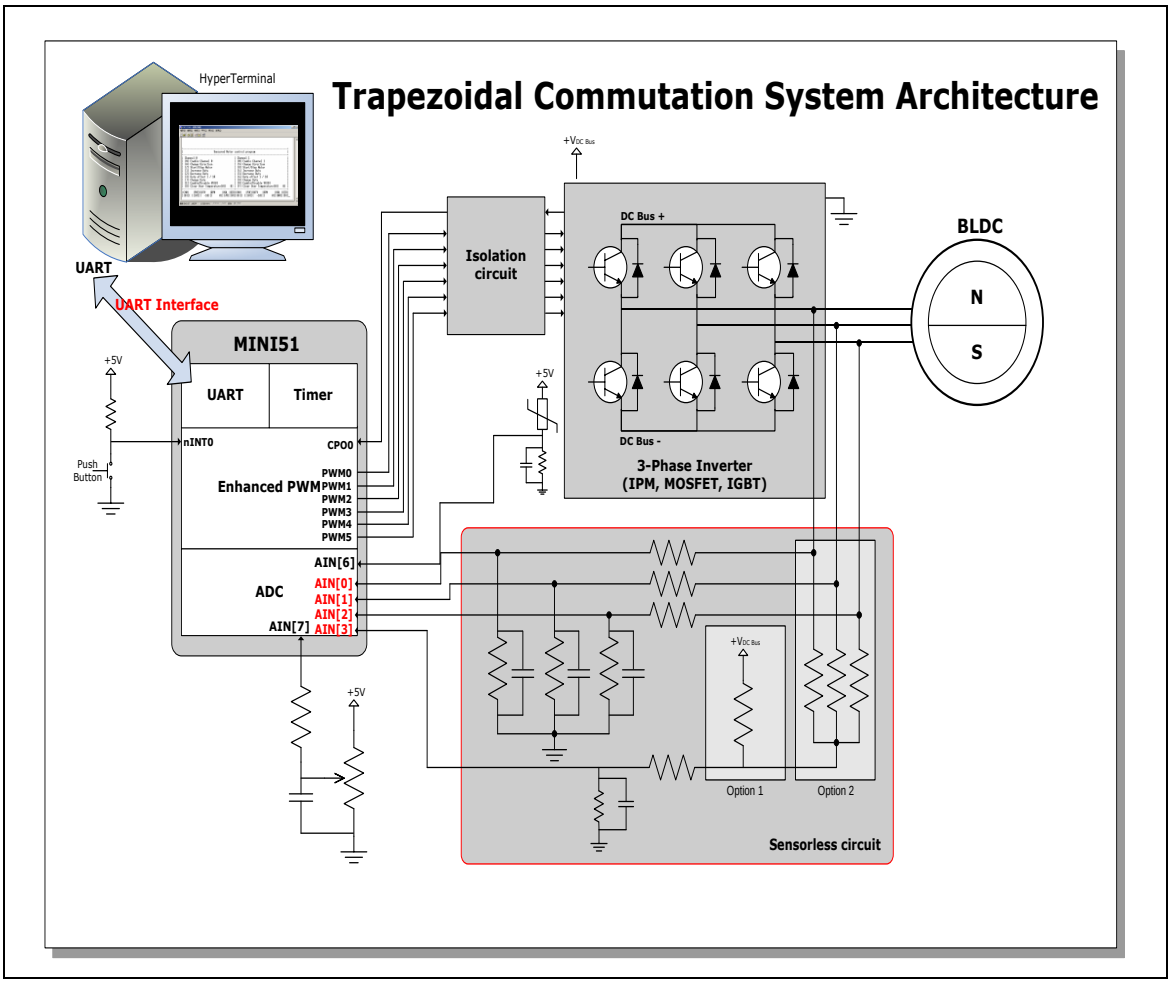


Figure 5.10-1 Application Circuit Diagram

5.12 Timer Controller

5.12.1 Overview

The timer module includes two channels, TIMER0~TIMER1, which allow user to easily implement a timer control for applications. The timer can perform functions like frequency measurement, interval measurement, clock generation, delay timing, and so on. The timer can generate an interrupt signal upon time-out, or provide the current value of count during operation.

5.12.2 Features

- Two sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each channel (TMR0_CLK, TMR1_CLK)
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Time-out period = (period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}); T is the period of timer clock
- Internal 24-bit up timer is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external pin
- Supports input capture function to capture or reset counter value

		A=14, B=11	
57600	A=22	A=22, B=15 A=30, B=11	A=382
38400	A=34	A=62, B=8 A=46, B=11 A=34, B=15	A=574
19200	A=70	A=126, B=8 A=94, B=11 A=70, B=15	A=1150
9600	A=142	A=254, B=8 A=190, B=11 A=142, B=15	A=2302
4800	A=286	A=510, B=8 A=382, B=11 A=286, B=15	A=4606

5.13.1.1 Auto-Flow Control

The UART controller supports auto-flow control function that uses two low-level signals, CTSn (clear-to-send) and RTSn (request-to-send), to control the flow of data transfer between the UART and external devices (ex: Modem). When auto-flow is enabled, the UART is not allowed to receive data until the UART asserts RTSn to external device. When the number of bytes in the RX FIFO equals the value of RTS_TRI_LEV (UA_FCR[19:16]), the RTSn is de-asserted. The UART sends data out when UART controller detects CTSn is asserted from external device. If a validly asserted CTSn is not detected the UART controller will not send data out.

5.13.1.2 IrDA Function Mode

The UART controllers also provides Serial IrDA (SIR, Serial Infrared) function (user must set IrDA_EN (UA_FUN_SEL[1:0]) to enable IrDA function). The SIR specification defines a short-range infrared asynchronous serial transmission mode with one start bit, 8 data bits, and 1 stop bit. The maximum data rate is 115.2 Kbps (half duplex). The IrDA SIR block contains an IrDA SIR Protocol encoder/decoder. The IrDA SIR protocol is half-duplex only. Thus it cannot transmit and receive data at the same time. The IrDA SIR physical layer specifies a minimum 10ms transfer delay between transmission and reception. This delay feature must be implemented by software.

5.13.1.3 RS-485 Function Mode

Alternate function of UART controllers is RS-485 9 bit mode function, direction control provided by RTSn pin or can program GPIO (P0.1 for RTSn) to implement the function by software. The RS-485 mode is selected by setting the UA_FUN_SEL register to select RS-485 function. The RS-485 driver control is implemented using the RTSn control signal from an asynchronous serial port to enable the RS-485 driver. In RS-485 mode, many characteristics of the RX and TX are the same as UART.

5.13.2 Features

- Full duplex, asynchronous communications
- Separates receive/transmit 16 bytes entry FIFO for data payloads
- Supports hardware auto flow control/flow control function (CTSn, RTSn) and programmable RTSn flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTSn wake-up function
- Supports 7-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR[DLY] register
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5, 6, 7, 8 character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports 3/16-bit duration for normal mode
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software RTSn control or software GPIO control to control transfer direction

5.14 Watchdog Timer

5.14.1 Overview

The purpose of Watchdog Timer (WDT) is to perform a system reset after software runs into a problem. This prevents system from hanging for an infinite period of time. Besides, the Watchdog Timer supports another function to wake up CPU from Power-down mode. The Watchdog timer includes an 18-bit free running counter with programmable time-out intervals. The following table shows the Watchdog time-out interval selection and the following figure shows the timing of Watchdog interrupt signal and reset signal.

Setting WTE (WTCR[7]) will enable the watchdog timer and the WDT counter starts counting up. When the counter reaches the selected time-out interval, the Watchdog timer interrupt flag WTIF will be set immediately to request a WDT interrupt if the Watchdog timer interrupt enable bit WTIE is set; in the meanwhile, a specified delay time (1024 * TWDT) follows the time-out event. User must set WTR (WTCR[0]) (Watchdog Timer Reset) high to reset the 18-bit WDT counter to avoid CPU from Watchdog Timer Reset before the delay time expires. The WTR bit is cleared automatically by hardware after the WDT counter is reset. There are eight time-out intervals with specific delay time which are selected by Watchdog timer interval select bits WTIS (WTCR[10:8]). If the WDT counter has not been cleared after the specific delay time expires, the Watchdog timer will set Watchdog Timer Reset Flag (WTRF) high and reset CPU. This reset will last 63 WDT clocks (TRST) and then CPU restarts executing program from reset vector (0x0000_0000). WTRF will not be cleared by Watchdog reset. User may poll WTRF through software to recognize the reset source. WDT also provides the wake-up function. When chip is powered down and the Watchdog Timer Wake-up Function Enable bit (WTCR[4]) is set, if the WDT counter has not been cleared after the specific delay time expires, the chip will be waked up from Power-down state.

WTIS	WTR Timeout Interval T_{TIS}	Interrupt Period T_{INT}	WTR Timeout Interval (WDT_CLK = 10 KHz) T_{TIS}	WTR Reset Interval (WDT_CLK = 10 KHz) T_{WTR}
000	$2^4 * T_{WDT}$	$1024 * T_{WDT}$	1.6 ms	104 ms
001	$2^6 * T_{WDT}$	$1024 * T_{WDT}$	6.4 ms	108.8 ms
010	$2^8 * T_{WDT}$	$1024 * T_{WDT}$	25.6 ms	128 ms
011	$2^{10} * T_{WDT}$	$1024 * T_{WDT}$	102.4 ms	204.8 ms
100	$2^{12} * T_{WDT}$	$1024 * T_{WDT}$	407 ms	512 ms
101	$2^{14} * T_{WDT}$	$1024 * T_{WDT}$	1.638 s	1.741 s
110	$2^{16} * T_{WDT}$	$1024 * T_{WDT}$	6.553 s	6.6.656 s
111	$2^{18} * T_{WDT}$	$1024 * T_{WDT}$	26.214 s	26.316 s

Table 5.14-1 Watchdog Time-out Interval Selection

Figure 8.3-1 Typical Crystal Application Circuit

8.3.4 External 32.768 KHz XTAL Oscillator

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Oscillator frequency	fL_{XTAL}		32.768		KHz	V_{DD} = 2.5V ~ 5.5V
Temperature	TL_{XTAL}	-40		+85	°C	
Operating current	I_{HXTAL}		TBD		μA	V_{DD} = 5.0V

8.3.5 Internal 22.1184 MHz RC Oscillator

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Supply voltage[1]	V_{HRC}		1.8		V	
Center frequency	F_{HRC}	21.89	22.1184	22.34	MHz	25°C, V_{DD} = 5V
		20.57	22.1184	23.23	MHz	-40°C~+85 °C, V_{DD} = 2.5V~5.5V
		21.78	22.0	22.22	MHz	-40°C~+85 °C, V_{DD} = 2.5V~5.5V 32.768K crystal oscillator Enabled and TRIM_SEL = 1
Operating current	I_{HRC}		TBD		mA	

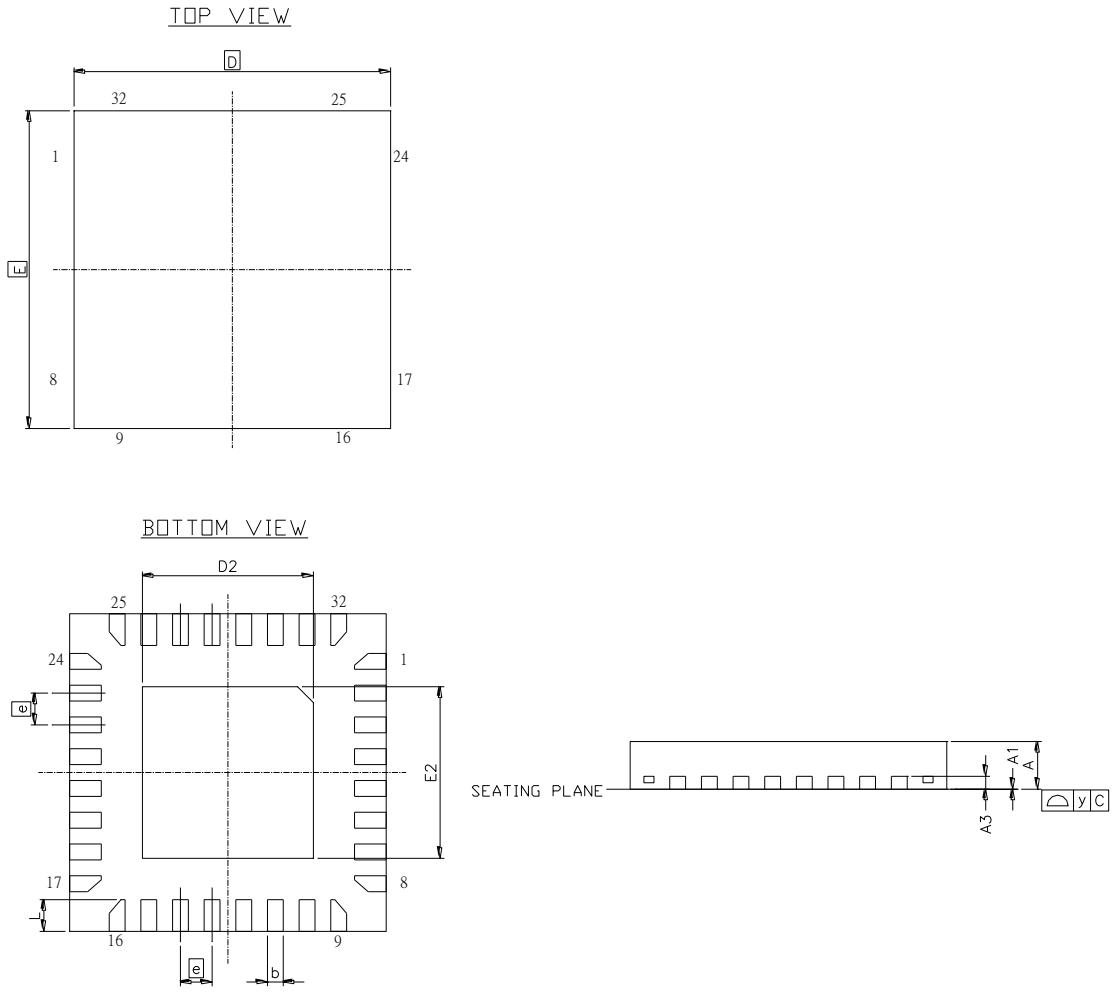
Note: Internal operation voltage comes from LDO.

8.3.6 Internal 10 KHz RC Oscillator

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Supply voltage[1]	V_{LRC}		1.8		V	
Center frequency	F_{LRC}	7	10	13	KHz	25°C, V_{DD} = 5V
		5	10	15	KHz	-40°C = ~+85 °C, V_{DD} = 2.5V~5.5V
Operating current	I_{LRC}		TBD		μA	V_{DD} = 5V

Note: Internal operation voltage comes from LDO.

9.3 33-pin QFN (5mm x 5mm)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
E	5.00 BSC			0.197 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		

SYMBOL	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
DIMENSION (MM)	3.4	3.5	3.6	3.4	3.5	3.6

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.