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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

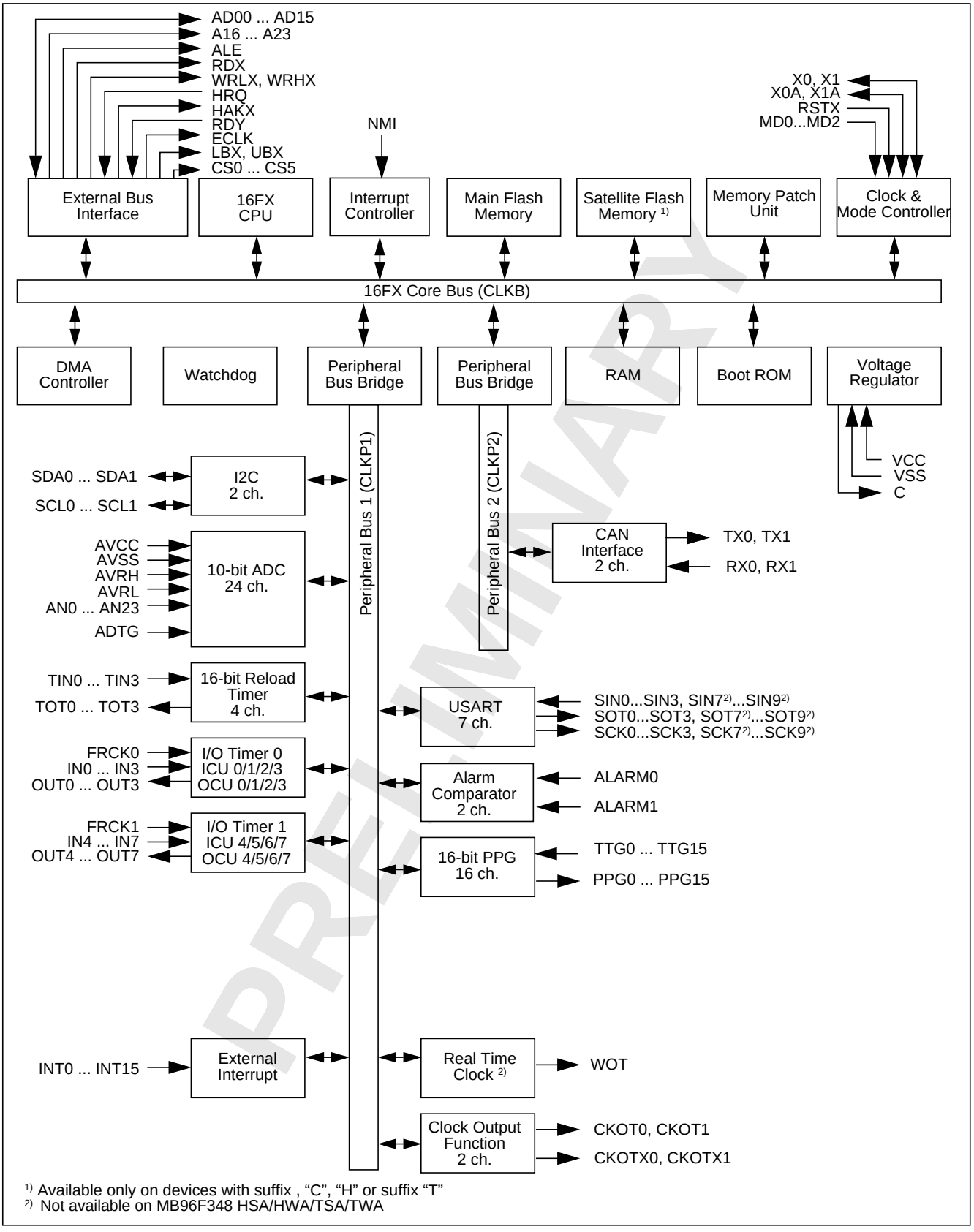
Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/fujitsu/mb96f348hsbpmc-gse2

■ PRODUCT LINEUP

Features		MB96V300	MB9634x
Product type		Evaluation sample	Flash product: MB96F34x Mask ROM product: MB9634x
Product options			
YS		NA	LVD persistently on / Single clock devices
RS			LVD can be disabled / Single clock devices
YW			LVD persistently on / Dual clock devices
RW			LVD can be disabled / Dual clock devices
TS			Satellite Flash / LVD persistently on / Single clock devices
HS			Satellite Flash / LVD can be disabled / Single clock devices
TW			Satellite Flash / LVD persistently on / Dual clock devices
HW			Satellite Flash / LVD can be disabled / Dual clock devices
AS			No CAN / No Satellite Flash / LVD persistently on / Single clock devices
CS			No CAN / /Satellite Flash / LVD can be disabled / Single clock devices
AW			No CAN / No Satellite Flash / LVD persistently on / Dual clock devices
CW			No CAN / Satellite Flash / LVD can be disabled / Dual clock devices
Flash/ ROM	RAM		
128kB	6kB	ROM/Flash memory emulation by external RAM, 92kB internal RAM	MB96344R, MB96344Y
288kB	16kB		MB96F346R, MB96346R, MB96F346Y, MB96346Y, MB96F346A
416kB	16kB		MB96F347R, MB96347R, MB96F347Y, MB96347Y, MB96F347A
544kB	24kB		MB96F348R, MB96F348Y, MB96F348A
Main: 544kB, Sat.: 32kB	24kB		MB96F348C, MB96F348H, MB96F348T
Package		BGA416	FPT-100P-M20 FPT-100P-M22
DMA		16 channels	6 channels
USART		10 channels	7 channels MB96F348 TSA/HSA/TWA/HWA: 4 channels
I2C		2 channels	2 channel
A/D Converter		40 channels	24 channels

Features	MB96V300	MB9634x
A/D Converter Reference Voltage switch	yes	yes
16-bit Reload Timer	6 channels	4 channels
16-bit Free-Running Timer	4 channels	2 channels
16-bit Output Compare	12 channels	8 channels
16-bit Input Capture	12 channels	8 channels
16-bit Programmable Pulse Generator	20 channels	16 channels
CAN Interface (not available on MB963xxA, MB963xxC)	5 channels	2 channels
External Interrupts	16 channels	
Non-Maskable Interrupt	1 channel	
Real Time Clock	1 MB96F348TSA/HSA/TWA/HWA: not available	
I/O Ports	136	80 for part number with suffix "W", 82 for part number with suffix "S"
Alarm comparator	2 channels	
External bus interface	Yes	Multiplexed
Chip select	6 signal	
Clock output function	2 channels	
Low voltage reset	Reset is generated when supply voltage is below minimum.	
On-chip RC-oscillator	Yes	

■ BLOCK DIAGRAM



1) Available only on devices with suffix , “C”, “H” or suffix “T”
2) Not available on MB96F348 HSA/HWA/TSA/TWA

■ PIN FUNCTION DESCRIPTION

Pin Function description (1 / 2)

Pin name	Feature	Description
ADn	External bus	External bus interface (multiplexed mode) address/data input/ output
ADTG	ADC	A/D converter trigger input
ADTG_R	ADC	Relocated A/D converter trigger input
ALARMn	Alarm comparator	Alarm Comparator n input
ALE	External bus	External bus Address Latch Enable output
ANn	ADC	A/D converter channel n input
AVCC	Supply	Analogue circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AVSS	Supply	Analogue circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin.
CKOTn	Clock output function	Clock Output function n output
CKOTXn	Clock output function	Clock Output Function n inverted output
ECLK	External bus	External bus clock output
CSn	External bus	External bus chip select n output
FRCKn	Free Running Timer	Free Running Timer n input
HAKX	External bus	External bus Hold Acknowlegde
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
LBX	External bus	External Bus Interface Lower Byte select strobe output
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
PPGn	PPG	Programmable Pulse Generator n output
PPGn_R	PPG	Relocated Programmable Pulse Generator n output

I/O map (6 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000084H	PPG1 - Duty cycle register		PDUT1		W
000085H	PPG1 - Duty cycle register				W
000086H	PPG1 - Control status register	PCNL1	PCN1		RW
000087H	PPG1 - Control status register	PCNH1			RW
000088H	PPG2 - Timer register		PTMR2		R
000089H	PPG2 - Timer register				R
00008AH	PPG2 - Period setting register		PCSR2		W
00008BH	PPG2 - Period setting register				W
00008CH	PPG2 - Duty cycle register		PDUT2		W
00008DH	PPG2 - Duty cycle register				W
00008EH	PPG2 - Control status register	PCNL2	PCN2		RW
00008FH	PPG2 - Control status register	PCNH2			RW
000090H	PPG3 - Timer register		PTMR3		R
000091H	PPG3 - Timer register				R
000092H	PPG3 - Period setting register		PCSR3		W
000093H	PPG3 - Period setting register				W
000094H	PPG3 - Duty cycle register		PDUT3		W
000095H	PPG3 - Duty cycle register				W
000096H	PPG3 - Control status register	PCNL3	PCN3		RW
000097H	PPG3 - Control status register	PCNH3			RW
000098H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11		RW
000099H	PPG7-PPG4 - General Control register 1 High	GCN1H1			RW
00009AH	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21		RW
00009BH	PPG7-PPG4 - General Control register 2 High	GCN2H1			RW
00009CH	PPG4 - Timer register		PTMR4		R
00009DH	PPG4 - Timer register				R
00009EH	PPG4 - Period setting register		PCSR4		W

I/O map (9 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0000CFH	USART1 - Ext. Status Register	ESCR1			RW
0000D0H	USART1 - Baud Rate Generator Register Low	BGRL1	BGR1		RW
0000D1H	USART1 - Baud Rate Generator Register High	BGRH1			RW
0000D2H	USART1 - Extended Serial Interrupt Register	ESIR1			RW
0000D3H	Reserved				
0000D4H	USART2 - Serial Mode Register	SMR2			RW
0000D5H	USART2 - Serial Control Register	SCR2			RW
0000D6H	USART2 - TX Register	TDR2			W
0000D6H	USART2 - RX Register	RDR2			R
0000D7H	USART2 - Serial Status	SSR2			RW
0000D8H	USART2 - Control/Com. Register	ECCR2			RW
0000D9H	USART2 - Ext. Status Register	ESCR2			RW
0000DAH	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2		RW
0000DBH	USART2 - Baud Rate Generator Register High	BGRH2			RW
0000DCH	USART2 - Extended Serial Interrupt Register	ESIR2			RW
0000DDH	Reserved				
0000DEH	USART3 - Serial Mode Register	SMR3			RW
0000DFH	USART3 - Serial Control Register	SCR3			RW
0000E0H	USART3 - TX Register	TDR3			W
0000E0H	USART3 - RX Register	RDR3			R
0000E1H	USART3 - Serial Status	SSR3			RW
0000E2H	USART3 - Control/Com. Register	ECCR3			RW
0000E3H	USART3 - Ext. Status Register	ESCR3			RW
0000E4H	USART3 - Baud Rate Generator Register Low	BGRL3	BGR3		RW
0000E5H	USART3 - Baud Rate Generator Register High	BGRH3			RW

I/O map (12 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
00012CH	DMA5 - I/O register address pointer low byte	IOAL5	IOA5		RW
00012DH	DMA5 - I/O register address pointer high byte	IOAH5			RW
00012EH	DMA5 - Data counter low byte	DCTL5	DCT5		RW
00012FH	DMA5 - Data counter high byte	DCTH5			RW
000180H	CPU - General Purpose registers (RAM access)	GPR_RAM			RW
000380H	DMA0 - Interrupt select	DISEL0			RW
000381H	DMA1 - Interrupt select	DISEL1			RW
000382H	DMA2 - Interrupt select	DISEL2			RW
000383H	DMA3 - Interrupt select	DISEL3			RW
000384H	DMA4 - Interrupt select	DISEL4			RW
000385H	DMA5 - Interrupt select	DISEL5			RW
000386H - 00038FH	Reserved				
000390H	DMA7-DMA0 - status register	DSRL	DSR		RW
000391H	Reserved				
000392H	DMA7-DMA0 - stop status register	DSSRL	DSSR		RW
000393H	Reserved				
000394H	DMA7-DMA0 - enable register	DERL	DER		RW
000395H - 000398H	Reserved				
000399H	Unused				
0003A0H	Interrupt level register	ILR	ICR		RW
0003A1H	Interrupt Index register	IDX			RW
0003A2H	Interrupt vector Table base register	TBRL	TBR		RW
0003A3H	Interrupt vector Table base register	TBRH			RW
0003A4H	Delayed Interrupt register	DIRR			RW
0003A5H	Non maskable Interrupt register	NMI			RW

I/O map (13 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0003A6H - 0003ADH	Reserved				
0003AEH	ROM mirror control register	ROMM			RW
0003AFH	EDSU configuration register	EDSU			RW
0003B0H	Memory patch control/status register ch 0/1		PFCS0		RW
0003B1H	Memory patch control/status register ch 0/1				RW
0003B2H	Memory patch control/status register ch 2/3		PFCS1		RW
0003B3H	Memory patch control/status register ch 2/3				RW
0003B4H	Memory patch control/status register ch 4/5		PFCS2		RW
0003B5H	Memory patch control/status register ch 4/5				RW
0003B6H	Memory patch control/status register ch 6/7		PFCS3		RW
0003B7H	Memory patch control/status register ch 6/7				RW
0003B8H	Memory Patch function - Patch address 0 low	PFAL0			RW
0003B9H	Memory Patch function - Patch address 0 middle	PFAM0			RW
0003BAH	Memory Patch function - Patch address 0 high	PFAH0			RW
0003BBH	Memory Patch function - Patch address 1 low	PFAL1			RW
0003BCH	Memory Patch function - Patch address 1 middle	PFAM1			RW
0003BDH	Memory Patch function - Patch address 1 high	PFAH1			RW
0003BEH	Memory Patch function - Patch address 2 low	PFAL2			RW
0003BFH	Memory Patch function - Patch address 2 middle	PFAM2			RW

I/O map (20 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0004AEH	P06 - I/O Port Pull-Up resistor Control Register	PUCR06			RW
0004AFH	P07 - I/O Port Pull-Up resistor Control Register	PUCR07			RW
0004B0H	P08 - I/O Port Pull-Up resistor Control Register	PUCR08			RW
0004B1H	P09 - I/O Port Pull-Up resistor Control Register	PUCR09			RW
0004B2H	P10 - I/O Port Pull-Up resistor Control Register	PUCR10			RW
0004B3H - 0004BBH	Reserved				
0004BCH	P00 - I/O Port External Pin State Register	EPSR00			R
0004BDH	P01 - I/O Port External Pin State Register	EPSR01			R
0004BEH	P02 - I/O Port External Pin State Register	EPSR02			R
0004BFH	P03 - I/O Port External Pin State Register	EPSR03			R
0004C0H	P04 - I/O Port External Pin State Register	EPSR04			R
0004C1H	P05 - I/O Port External Pin State Register	EPSR05			R
0004C2H	P06 - I/O Port External Pin State Register	EPSR06			R
0004C3H	P07 - I/O Port External Pin State Register	EPSR07			R
0004C4H	P08 - I/O Port External Pin State Register	EPSR08			R
0004C5H	P09 - I/O Port External Pin State Register	EPSR09			R
0004C6H	P10 - I/O Port External Pin State Register	EPSR10			R
0004C7H - 0004CFH	Reserved				

I/O map (31 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0007A3H	CAN0 - Interrupt Pending Register	INTPND2H0			R
0007A4H - 0007AFH	Reserved				
0007B0H	CAN0 - Message Valid Register	MSGVAL1L0	MSGVAL10	MSGVAL0	R
0007B1H	CAN0 - Message Valid Register	MSGVAL1H0			R
0007B2H	CAN0 - Message Valid Register	MSGVAL2L0	MSGVAL20		R
0007B3H	CAN0 - Message Valid Register	MSGVAL2H0			R
0007B4H - 0007CDH	Reserved				
0007CEH	CAN0 - Output enable register	COER0			RW
0007CFH - 0007FFH	Reserved				
000800H	CAN1 - Control register	CTRLRL1	CTRLR1		RW
000801H	CAN1 - Control register	CTRLRH1			R
000802H	CAN1 - Status register	STATRL1	STATR1		RW
000803H	CAN1 - Status register	STATRH1			R
000804H	CAN1 - Error Counter (Transmit)	ERRCNTL1	ERRCNT1		R
000805H	CAN1 - Error Counter (Receive)	ERRCNTH1			R
000806H	CAN1 - Bit Timing Register	BTRL1	BTR1		RW
000807H	CAN1 - Bit Timing Register	BTRH1			RW
000808H	CAN1 - Interrupt Register	INTRL1	INTR1		R
000809H	CAN1 - Interrupt Register	INTRH1			R
00080AH	CAN1 - Test Register	TESTRL1	TESTR1		RW
00080BH	CAN1 - Test Register	TESTRH1			R
00080CH	CAN1 - BRP Extension register	BRPERL1	BRPER1		RW
00080DH	CAN1 - BRP Extension register	BRPERH1			R
00080EH - 00080FH	Reserved				
000810H	CAN1 - IF1 Command request register	IF1CREQL1	IF1CREQ1		RW

I/O map (32 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000811H	CAN1 - IF1 Command request register	IF1CREQH1			RW
000812H	CAN1 - IF1 Command Mask register	IF1CMSKL1	IF1CMSK1		RW
000813H	CAN1 - IF1 Command Mask register	IF1CMSKH1			R
000814H	CAN1 - IF1 Mask Register	IF1MSK1L1	IF1MSK11		RW
000815H	CAN1 - IF1 Mask Register	IF1MSK1H1			RW
000816H	CAN1 - IF1 Mask Register	IF1MSK2L1	IF1MSK21		RW
000817H	CAN1 - IF1 Mask Register	IF1MSK2H1			RW
000818H	CAN1 - IF1 Arbitration register	IF1ARB1L1	IF1ARB11		RW
000819H	CAN1 - IF1 Arbitration register	IF1ARB1H1			RW
00081AH	CAN1 - IF1 Arbitration register	IF1ARB2L1	IF1ARB21		RW
00081BH	CAN1 - IF1 Arbitration register	IF1ARB2H1			RW
00081CH	CAN1 - IF1 Message Control Register	IF1MCTRL1	IF1MCTR1		RW
00081DH	CAN1 - IF1 Message Control Register	IF1MCTRH1			RW
00081EH	CAN1 - IF1 Data A1	IF1DTA1L1	IF1DTA11		RW
00081FH	CAN1 - IF1 Data A1	IF1DTA1H1			RW
000820H	CAN1 - IF1 Data A2	IF1DTA2L1	IF1DTA21		RW
000821H	CAN1 - IF1 Data A2	IF1DTA2H1			RW
000822H	CAN1 - IF1 Data B1	IF1DTB1L1	IF1DTB11		RW
000823H	CAN1 - IF1 Data B1	IF1DTB1H1			RW
000824H	CAN1 - IF1 Data B2	IF1DTB2L1	IF1DTB21		RW
000825H	CAN1 - IF1 Data B2	IF1DTB2H1			RW
000826H - 00083FH	Reserved				
000840H	CAN1 - IF2 Command request register	IF2CREQL1	IF2CREQ1		RW
000841H	CAN1 - IF2 Command request register	IF2CREQH1			RW
000842H	CAN1 - IF2 Command Mask register	IF2CMSKL1	IF2CMSK1		RW
000843H	CAN1 - IF2 Command Mask register	IF2CMSKH1			R
000844H	CAN1 - IF2 Mask Register	IF2MSK1L1	IF2MSK11		RW
000845H	CAN1 - IF2 Mask Register	IF2MSK1H1			RW
000846H	CAN1 - IF2 Mask Register	IF2MSK2L1	IF2MSK21		RW

Interrupt vector table (2 / 4)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
27	390	EXTINT10	Yes	27	External Interrupt 10
28	38C	EXTINT11	Yes	28	External Interrupt 11
29	388	EXTINT12	Yes	29	External Interrupt 12
30	384	EXTINT13	Yes	30	External Interrupt 13
31	380	EXTINT14	Yes	31	External Interrupt 14
32	37C	EXTINT15	Yes	32	External Interrupt 15
33	378	CAN0	No	33	CAN Controller 0
34	374	CAN1	No	34	CAN Controller 1
35	370	PPG0	Yes	35	Programmable Pulse Generator 0
36	36C	PPG1	Yes	36	Programmable Pulse Generator 1
37	368	PPG2	Yes	37	Programmable Pulse Generator 2
38	364	PPG3	Yes	38	Programmable Pulse Generator 3
39	360	PPG4	Yes	39	Programmable Pulse Generator 4
40	35C	PPG5	Yes	40	Programmable Pulse Generator 5
41	358	PPG6	Yes	41	Programmable Pulse Generator 6
42	354	PPG7	Yes	42	Programmable Pulse Generator 7
43	350	PPG8	Yes	43	Programmable Pulse Generator 8
44	34C	PPG9	Yes	44	Programmable Pulse Generator 9
45	348	PPG10	Yes	45	Programmable Pulse Generator 10
46	344	PPG11	Yes	46	Programmable Pulse Generator 11
47	340	PPG12	Yes	47	Programmable Pulse Generator 12
48	33C	PPG13	Yes	48	Programmable Pulse Generator 13
49	338	PPG14	Yes	49	Programmable Pulse Generator 14
50	334	PPG15	Yes	50	Programmable Pulse Generator 15
51	330	RLT0	Yes	51	Reload Timer 0
52	32C	RLT1	Yes	52	Reload Timer 1
53	328	RLT2	Yes	53	Reload Timer 2
54	324	RLT3	Yes	54	Reload Timer 3
55	320	PPGRLT	Yes	55	Reload Timer 6 - dedicated for PPG

- As a measure against power supply noise, connect a capacitor of about 0.1 µF as a bypass capacitor between VCC and VSS as close as possible to VCC and VSS pins.

7. Crystal Oscillator Circuit

- Noise at X0 or X1 pins may possibly cause abnormal operation. Make sure to provide bypass capacitors with shortest distance to X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.
- It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.
- It is highly recommended to evaluate the quartz/MCU system at the quartz manufacturer.

8. Turn on Sequence of Power Supply to A/D Converter and Analog Inputs

- Make sure to turn the A/D converter power supply (AVCC, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (VCC) on.
- Turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, make sure that the voltage does not exceed AVRH or AVCC (turning the analog and digital power supplies simultaneously on or off is acceptable).

9. Connection of Unused Pins of A/D Converter

- Connect unused pins of A/D converter as AVCC = VCC, AVSS = AVRH = AVRL = VSS.

10. Notes on Energization

- To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2 V to 2.7 V.

11. Stabilization of power supply voltage

- If the power supply voltage varies acutely even within the operation assurance range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, stabilize the power supply voltage so that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

External Bus timing

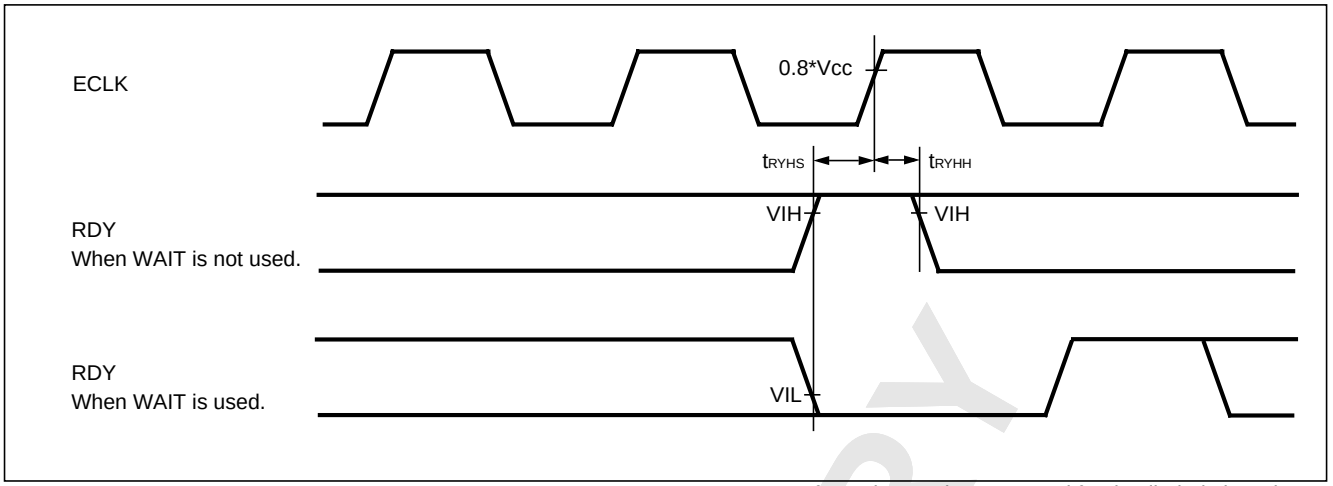
Basic Timing

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive}=5mA,C_L=50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	25	—	ns	
	t_{CHCL}		—	t_{CYC}/2-5	t_{CYC}/2+5	ns	if CLKB duty cycle is 50%
	t_{CLCH}		—	t_{CYC}/2-5	t_{CYC}/2+5	ns	
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX,ECLK	—	-20	20	ns	
	t_{CHCBL}		—	-20	20	ns	
	t_{CLCBH}		—	-20	20	ns	
	t_{CLCBL}		—	-20	20	ns	
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-10	10	ns	
	t_{CHLL}		—	-10	10	ns	
	t_{CLLH}		—	-10	10	ns	
	t_{CLLL}		—	-10	10	ns	
ECLK → address valid time	t_{CHAV}	A[23:16],ECLK	—	-15	15	ns	
	t_{CLAV}		—	-15	15	ns	
ECLK → address valid time	t_{CLADV}	AD[15:0],ECLK	—	-15	15	ns	
	t_{CHADV}		—	-15	15	ns	
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX,WRHX, ECLK	—	-10	10	ns	
	t_{CHRWL}		—	-10	10	ns	
	t_{CLRWH}		—	-10	10	ns	
	t_{CLRWL}		—	-10	10	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive}=5mA,C_L=50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	30	—	ns	
	t_{CHCL}		—	t_{CYC}/2-8	t_{CYC}/2+8	ns	if CLKB duty cycle is 50%
	t_{CLCH}		—	t_{CYC}/2-8	t_{CYC}/2+8	ns	
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX,ECLK	—	-25	25	ns	
	t_{CHCBL}		—	-25	25	ns	
	t_{CLCBH}		—	-25	25	ns	
	t_{CLCBL}		—	-25	25	ns	



Refer to the Hardware Manual for detailed Timing Charts.

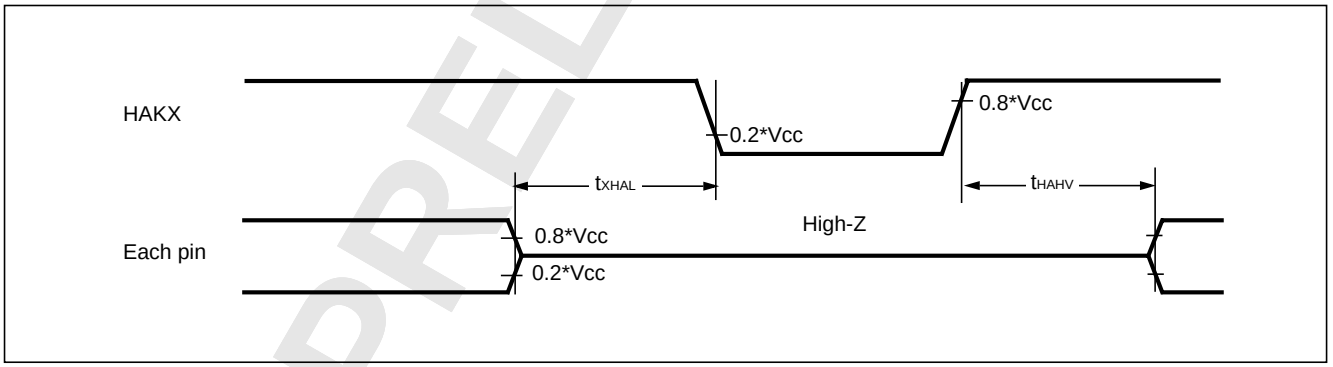
Hold Timing

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive}=5mA,C_l=50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	—	t_{CYC} – 20	t_{CYC} + 20	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 20	t_{CYC} + 20	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive}=5mA,C_l=50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	—	t_{CYC} – 25	t_{CYC} + 25	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 25	t_{CYC} + 25	ns	



Refer to the Hardware Manual for detailed Timing Charts.

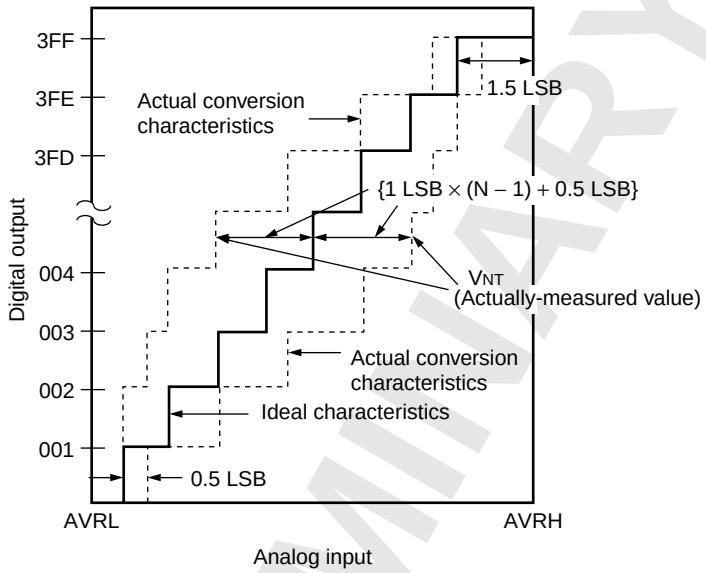
Differential linearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Total error: Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

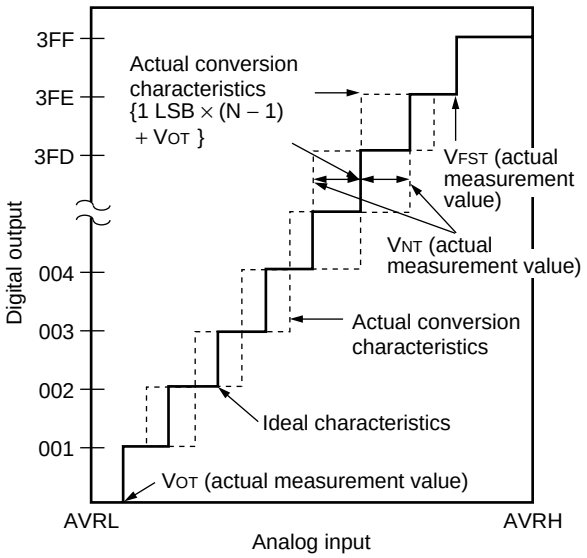
$$1\ \text{LSB} = (\text{Ideal value})\ \frac{AVRH - AVRL}{1024}\ [\text{V}]$$

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

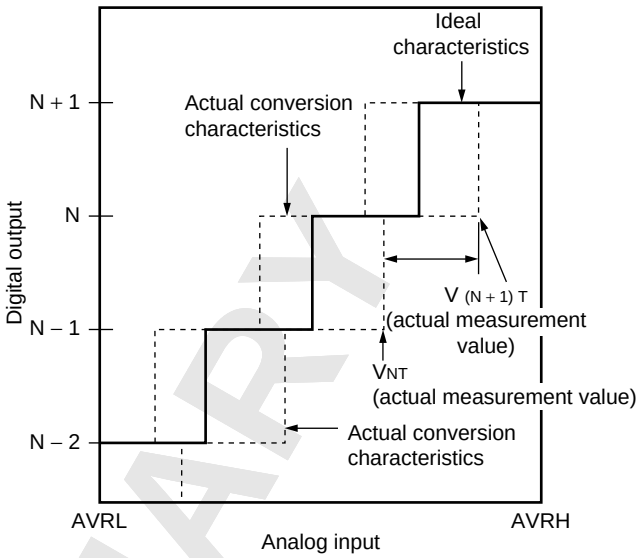
V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

Non linearity error



Differential linearity error



$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage at which digital output transits from "000_H" to "001_H."
V_{FST} : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$."

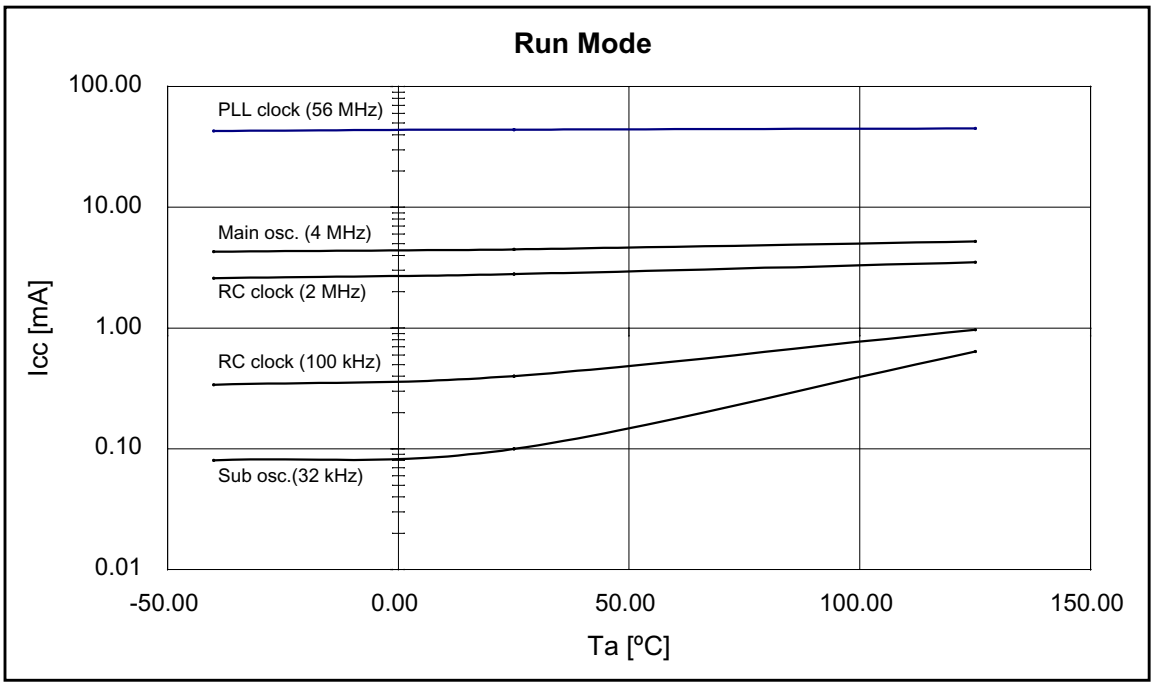
Notes on A/D Converter Section

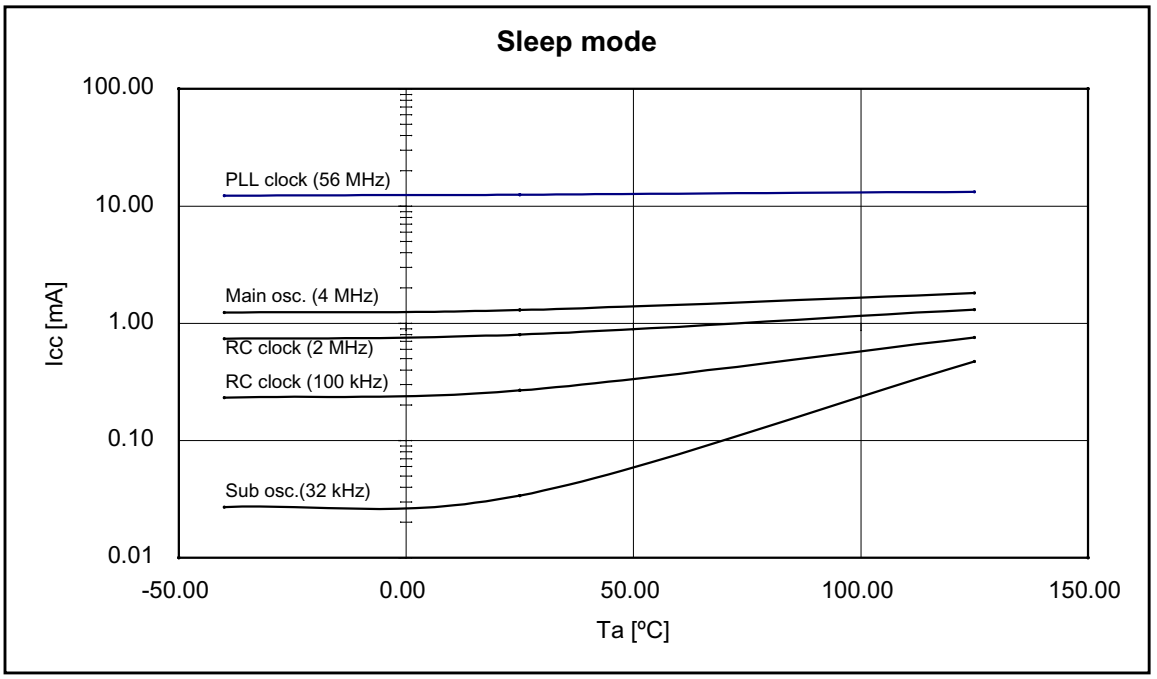
- About the external impedance of the analog input and its sampling time

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

■ EXAMPLE CHARACTERISTICS

The diagrams below show the characteristics of one measured sample of MB96F348HSB with typical process parameters.





Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = 56 MHz CLKP2 = 28 MHz Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100 kHz Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32 kHz Regulator in Low Power Mode A Core Voltage = 1.8 V
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = 56 MHz CLKP2 = 28 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100 kHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32 kHz (CLKB is stopped in this mode) Regulator in Low Power Mode A Core Voltage = 1.8 V

■ REVISION HISTORY

Revision	Date	Modification
1	2007-05-07	Creation
2	2007-05-10	External bus hold timing update
3	2007-05-23	Electrical characteristics updates
4	2007-08-02	Electrical characteristics updates, Product lineup, changes and ordering information
5	2007-09-12	Addition of the electrical charcateristic examples and the LVD characteristics specifications, updates of the DC charcateristics. Pin circuit type drawing modifications.