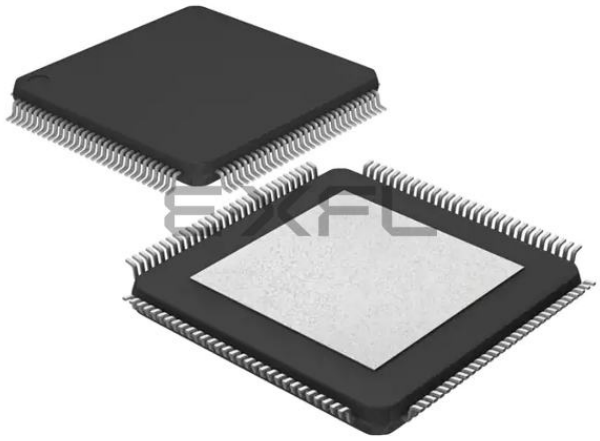

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	CAN, I²C, SPI, SPORT, UART/USART
Clock Rate	150MHz
Non-Volatile Memory	FLASH (512kB)
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP Exposed Pad
Supplier Device Package	120-LQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-cm402cswz-ef

ADSP-CM402F/CM403F/CM407F/CM408F/CM409F

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REVISION HISTORY

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ANALOG FRONT END

The mixed-signal controllers contain two ADCs and two DACs. Control of these data converters is simplified by a powerful on-chip analog-to-digital conversion controller (ADCC) and a digital-to-analog conversion controller (DACC). The ADCC and DACC are integrated seamlessly into the software programming model, and they efficiently manage the configuration and real-time operation of the ADCs and DACs.

For technical details, see ADC/DAC Specifications on Page 68.

The ADCC provides the mechanism to precisely control execution of timing and analog sampling events on the ADCs. The ADCC supports two-channel (one each—ADC0, ADC1) simultaneous sampling of ADC inputs and can deliver 16 channels of ADC data to memory in 3 µs. Conversion data from the ADCs may be either routed via DMA to memory, or to a destination register via the processor. The ADCC can be configured so that the two ADCs sample and convert both analog inputs simultaneously or at different times and may be operated in asynchronous or synchronous modes. The best performance can be achieved in synchronous mode.

Likewise, the DACC interfaces to two DACs and has purpose of managing those DACs. Conversion data to the DACs may be either routed from memory through DMA, or from a source register via the processor.

Functional operation and programming for the ADCC and DACC are described in detail in the *ADSP-CM40x Mixed-Signal Control Processor with ARM Cortex-M4 Hardware Reference*.

ADC and DAC features and performance specifications differ by processor model. Simplified block diagrams of the ADCC/DACC and the ADC/DAC are shown in Figure 2 and Figure 3.

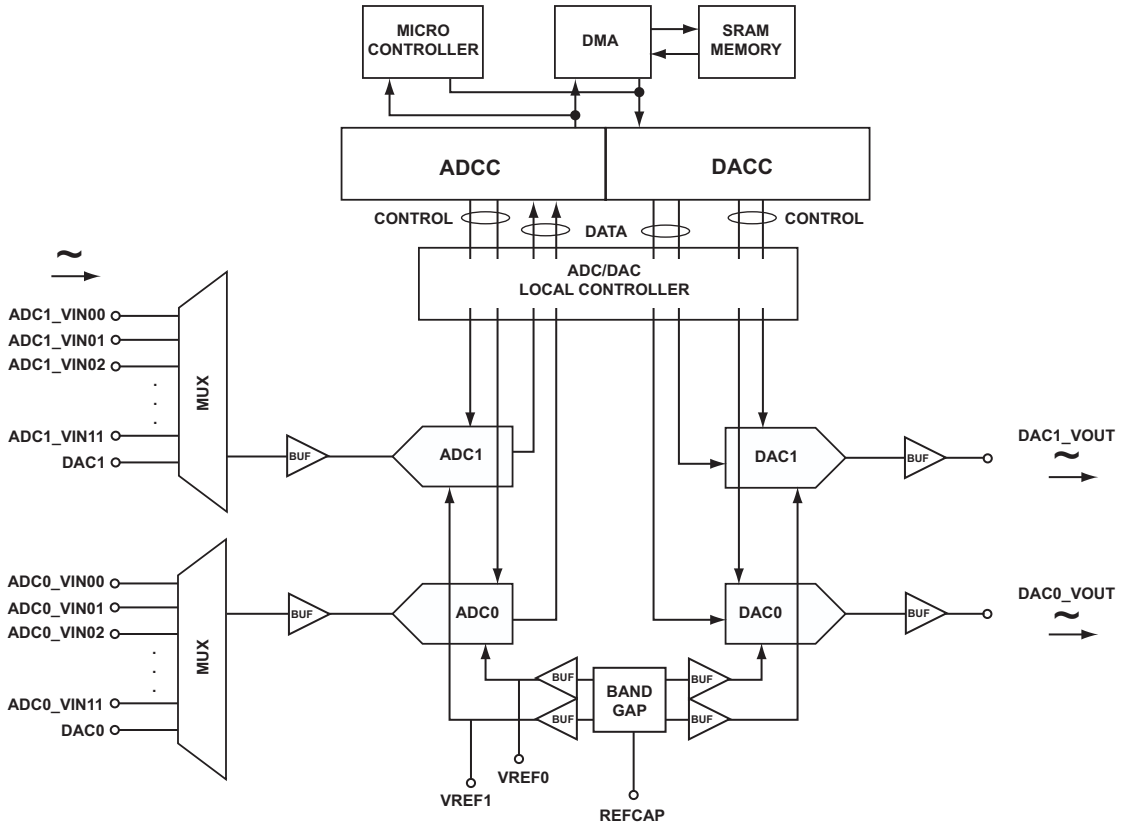

Figure 2. ADSP-CM402F/ADSP-CM403F/ADSP-CM409F Analog Front End Block Diagram

Table 7. ADSP-CM402F/ADSP-CM403F 120-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
CNT0_OUTB	CNT0 Output Divider B	B	PB_14
CNT0_UD	CNT0 Count Up and Direction	B	PB_01
CNT0_ZM	CNT0 Count Zero Marker	B	PB_00
CNT1_DG	CNT1 Count Down and Gate	B	PB_05
CNT1_UD	CNT1 Count Up and Direction	B	PB_04
CNT1_ZM	CNT1 Count Zero Marker	B	PB_03
CPTMR0_IN0	CPTMR0 Capture Timer0 Input 0	B	PB_07
CPTMR0_IN1	CPTMR0 Capture Timer0 Input 1	B	PB_08
CPTMR0_IN2	CPTMR0 Capture Timer0 Input 2	B	PB_09
DAC0_VOUT	Analog Voltage Output 0	Not Muxed	DAC0_VOUT
DAC1_VOUT	Analog Voltage Output 1	Not Muxed	DAC1_VOUT
GND	Digital Ground	Not Muxed	GND
GND_ANA0	Analog Ground return for VDD_ANA0 (see recommended bypass - Figure 4 on Page 6)	Not Muxed	GND_ANA0
GND_ANA1	Analog Ground return for VDD_ANA1 (see recommended bypass - Figure 4 on Page 6)	Not Muxed	GND_ANA1
GND_ANA2	Analog Ground (see recommended bypass - Figure 4 on Page 6)	Not Muxed	GND_ANA2
GND_ANA3	Analog Ground (see recommended bypass - Figure 4 on Page 6)	Not Muxed	GND_ANA3
GND_VREF0	Ground return for VREF0 (see recommended bypass filter - Figure 4 on Page 6)	Not Muxed	GND_VREF0
GND_VREF1	Ground return for VREF1 (see recommended bypass filter - Figure 4 on Page 6)	Not Muxed	GND_VREF1
JTG_TCK/SWCLK	JTAG Clock/Serial Wire Clock	Not Muxed	JTG_TCK/SWCLK
JTG_TDI	JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO/SWO	JTAG Serial Data Out/Serial Wire Trace Output	Not Muxed	JTG_TDO/SWO
JTG_TMS/SWDIO	JTAG Mode Select/Serial Wire Debug Data I/O	Not Muxed	JTG_TMS/SWDIO
$\overline{\text{JTG\_TRST}}$	JTAG Reset	Not Muxed	$\overline{\text{JTG\_TRST}}$
PA_00-PA_15	Port A Positions 0 – 15	A	PA_00 – PA_15
PB_00-PB_15	Port B Positions 0 – 15	B	PB_00 – PB_15
PC_00-PC_07	Port C Positions 0 – 7	C	PC_00 – PC_07
PWM0_AH	PWM0 Channel A High Side	A	PA_02
PWM0_AL	PWM0 Channel A Low Side	A	PA_03
PWM0_BH	PWM0 Channel B High Side	A	PA_04
PWM0_BL	PWM0 Channel B Low Side	A	PA_05
PWM0_CH	PWM0 Channel C High Side	A	PA_06
PWM0_CL	PWM0 Channel C Low Side	A	PA_07
PWM0_DH	PWM0 Channel D High Side	B	PB_00
PWM0_DL	PWM0 Channel D Low Side	B	PB_01
PWM0_SYNC	PWM0 Sync	A	PA_00
$\overline{\text{PWM0\_TRIP0}}$	PWM0 Trip Input 0	A	PA_01
PWM1_AH	PWM1 Channel A High Side	A	PA_12
PWM1_AL	PWM1 Channel A Low Side	A	PA_13
PWM1_BH	PWM1 Channel B High Side	A	PA_14
PWM1_BL	PWM1 Channel B Low Side	A	PA_15
PWM1_CH	PWM1 Channel C High Side	A	PA_08
PWM1_CL	PWM1 Channel C Low Side	A	PA_09
PWM1_DH	PWM1 Channel D High Side	B	PB_02

Table 7. ADSP-CM402F/ADSP-CM403F 120-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PWM1_DL	PWM1 Channel D Low Side	B	PB_03
PWM1_SYNC	PWM1 Sync	A	PA_10
$\overline{\text{PWM1\_TRIP0}}$	PWM1 Trip Input 0	A	PA_11
PWM2_AH	PWM2 Channel A High Side	B	PB_06
PWM2_AL	PWM2 Channel A Low Side	B	PB_07
PWM2_BH	PWM2 Channel B High Side	B	PB_08
PWM2_BL	PWM2 Channel B Low Side	B	PB_09
PWM2_CH	PWM2 Channel C High Side	C	PC_03
PWM2_CL	PWM2 Channel C Low Side	C	PC_04
PWM2_DH	PWM2 Channel D High Side	C	PC_05
PWM2_DL	PWM2 Channel D Low Side	C	PC_06
PWM2_SYNC	PWM2 Sync	B	PB_04
$\overline{\text{PWM2\_TRIP0}}$	PWM2 Trip Input 0	B	PB_05
REFCAP	Output of BandGap Generator Filter Node (see recommended bypass filter - Figure 4 on Page 6)	Not Muxed	REFCAP
SINC0_CLK0	SINC0 Clock 0	B	PB_10
SINC0_CLK1	SINC0 Clock 1	C	PC_07
SINC0_D0	SINC0 Data 0	B	PB_11
SINC0_D1	SINC0 Data 1	B	PB_12
SINC0_D2	SINC0 Data 2	B	PB_13
SINC0_D3	SINC0 Data 3	B	PB_14
SMC0_A01	SMC0 Address 1	B	PB_13
SMC0_A02	SMC0 Address 2	B	PB_14
SMC0_A03	SMC0 Address 3	B	PB_15
SMC0_A04	SMC0 Address 4	C	PC_00
SMC0_A05	SMC0 Address 5	C	PC_01
$\overline{\text{SMC0\_AMS0}}$	SMC0 Memory Select 0	B	PB_11
$\overline{\text{SMC0\_AMS2}}$	SMC0 Memory Select 2	A	PA_07
$\overline{\text{SMC0\_AOE}}$	SMC0 Output Enable	B	PB_12
SMC0_ARDY	SMC0 Asynchronous Ready	B	PB_08
$\overline{\text{SMC0\_ARE}}$	SMC0 Read Enable	B	PB_09
$\overline{\text{SMC0\_AWE}}$	SMC0 Write Enable	B	PB_10
SMC0_D00	SMC0 Data 0	A	PA_08
SMC0_D01	SMC0 Data 1	A	PA_09
SMC0_D02	SMC0 Data 2	A	PA_10
SMC0_D03	SMC0 Data 3	A	PA_11
SMC0_D04	SMC0 Data 4	A	PA_12
SMC0_D05	SMC0 Data 5	A	PA_13
SMC0_D06	SMC0 Data 6	A	PA_14
SMC0_D07	SMC0 Data 7	A	PA_15
SMC0_D08	SMC0 Data 8	B	PB_00
SMC0_D09	SMC0 Data 9	B	PB_01
SMC0_D10	SMC0 Data 10	B	PB_02
SMC0_D11	SMC0 Data 11	B	PB_03
SMC0_D12	SMC0 Data 12	B	PB_04
SMC0_D13	SMC0 Data 13	B	PB_05

Table 7. ADSP-CM402F/ADSP-CM403F 120-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_D14	SMC0 Data 14	B	PB_06
SMC0_D15	SMC0 Data 15	B	PB_07
SPI0_CLK	SPI0 Clock	C	PC_03
SPI0_D2	SPI0 Data 2	B	PB_10
SPI0_D3	SPI0 Data 3	B	PB_11
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_04
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_05
SPI0_RDY	SPI0 Ready	C	PC_02
$\overline{\text{SPI0\_SEL1}}$	SPI0 Slave Select Output 1	C	PC_06
$\overline{\text{SPI0\_SEL2}}$	SPI0 Slave Select Output 2	B	PB_13
$\overline{\text{SPI0\_SEL3}}$	SPI0 Slave Select Output 3	B	PB_14
$\overline{\text{SPI0\_SS}}$	SPI0 Slave Select Input	B	PB_14
SPT0_ACLK	SPORT0 Channel A Clock	B	PB_00
SPT0_AD0	SPORT0 Channel A Data 0	B	PB_02
SPT0_AD1	SPORT0 Channel A Data 1	B	PB_03
SPT0_AFS	SPORT0 Channel A Frame Sync	B	PB_01
SPT0_ATDV	SPORT0 Channel A Transmit Data Valid	B	PB_04
SPT1_ACLK	SPORT1 Channel A Clock	A	PA_00
SPT1_AD0	SPORT1 Channel A Data 0	A	PA_02
SPT1_AD1	SPORT1 Channel A Data 1	A	PA_03
SPT1_AFS	SPORT1 Channel A Frame Sync	A	PA_01
SPT1_ATDV	SPORT1 Channel A Transmit Data Valid	B	PB_15
SPT1_BCLK	SPORT1 Channel B Clock	A	PA_04
SPT1_BD0	SPORT1 Channel B Data 0	A	PA_06
SPT1_BD1	SPORT1 Channel B Data 1	A	PA_07
SPT1_BFS	SPORT1 Channel B Frame Sync	A	PA_05
SPT1_BTDV	SPORT1 Channel B Transmit Data Valid	C	PC_00
SYS_BMODE0	Boot Mode Control 0	Not Muxed	SYS_BMODE0
SYS_BMODE1	Boot Mode Control 1	Not Muxed	SYS_BMODE1
SYS_CLKIN	Clock/Crystal Input	Not Muxed	SYS_CLKIN
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
SYS_DSWAKE0	Deep Sleep Wake-up 0	C	PC_06
SYS_DSWAKE1	Deep Sleep Wake-up 1	C	PC_07
SYS_DSWAKE2	Deep Sleep Wake-up 2	B	PB_14
SYS_DSWAKE3	Deep Sleep Wake-up 3	B	PB_13
$\overline{\text{SYS\_FAULT}}$	System Fault Output	Not Muxed	$\overline{\text{SYS\_FAULT}}$
$\overline{\text{SYS\_HWRST}}$	Processor Hardware Reset Control	Not Muxed	$\overline{\text{SYS\_HWRST}}$
$\overline{\text{SYS\_NMI}}$	Nonmaskable Interrupt	Not Muxed	$\overline{\text{SYS\_NMI}}$
$\overline{\text{SYS\_RESOUT}}$	Reset Output	Not Muxed	$\overline{\text{SYS\_RESOUT}}$
SYS_XTAL	Crystal Output	Not Muxed	SYS_XTAL
TM0_ACI1	TIMER0 Alternate Capture Input 1	B	PB_10
TM0_ACI2	TIMER0 Alternate Capture Input 2	B	PB_08
TM0_ACI3	TIMER0 Alternate Capture Input 3	B	PB_12
TM0_ACI4	TIMER0 Alternate Capture Input 4	B	PB_15
TM0_ACI5	TIMER0 Alternate Capture Input 5	C	PC_01
TM0_ACLK0	TIMER0 Alternate Clock 0	B	PB_13

Table 11. ADSP-CM407F/ADSP-CM408F 176-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_D06	SMC0 Data 6	A	PA_14
SMC0_D06	SMC0 Data 6	C	PC_14
SMC0_D07	SMC0 Data 7	A	PA_15
SMC0_D07	SMC0 Data 7	C	PC_15
SMC0_D08	SMC0 Data 8	B	PB_00
SMC0_D08	SMC0 Data 8	D	PD_00
SMC0_D09	SMC0 Data 9	B	PB_01
SMC0_D09	SMC0 Data 9	D	PD_01
SMC0_D10	SMC0 Data 10	B	PB_02
SMC0_D10	SMC0 Data 10	D	PD_02
SMC0_D11	SMC0 Data 11	B	PB_03
SMC0_D11	SMC0 Data 11	D	PD_03
SMC0_D12	SMC0 Data 12	B	PB_04
SMC0_D12	SMC0 Data 12	D	PD_04
SMC0_D13	SMC0 Data 13	B	PB_05
SMC0_D13	SMC0 Data 13	D	PD_05
SMC0_D14	SMC0 Data 14	B	PB_06
SMC0_D14	SMC0 Data 14	D	PD_06
SMC0_D15	SMC0 Data 15	B	PB_07
SMC0_D15	SMC0 Data 15	D	PD_07
SPI0_CLK	SPI0 Clock	C	PC_03
SPI0_D2	SPI0 Data 2	B	PB_10
SPI0_D3	SPI0 Data 3	B	PB_11
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_04
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_05
SPI0_RDY	SPI0 Ready	C	PC_02
$\overline{\text{SPI0\_SEL1}}$	SPI0 Slave Select Output 1	C	PC_06
$\overline{\text{SPI0\_SEL2}}$	SPI0 Slave Select Output 2	B	PB_13
$\overline{\text{SPI0\_SEL3}}$	SPI0 Slave Select Output 3	B	PB_14
$\overline{\text{SPI0\_SS}}$	SPI0 Slave Select Input	B	PB_14
SPI1_CLK	SPI1 Clock	C	PC_12
SPI1_MISO	SPI1 Master In, Slave Out	C	PC_13
SPI1_MOSI	SPI1 Master Out, Slave In	C	PC_14
$\overline{\text{SPI1\_SEL1}}$	SPI1 Slave Select Output 1	C	PC_15
$\overline{\text{SPI1\_SEL2}}$	SPI1 Slave Select Output 2	B	PB_06
$\overline{\text{SPI1\_SEL3}}$	SPI1 Slave Select Output 3	B	PB_07
$\overline{\text{SPI1\_SS}}$	SPI1 Slave Select Input	C	PC_15
SPT0_ACLK	SPORT0 Channel A Clock	B	PB_00
SPT0_ACLK	SPORT0 Channel A Clock	E	PE_00
SPT0_AD0	SPORT0 Channel A Data 0	B	PB_02
SPT0_AD0	SPORT0 Channel A Data 0	E	PE_02
SPT0_AD1	SPORT0 Channel A Data 1	B	PB_03
SPT0_AD1	SPORT0 Channel A Data 1	E	PE_03
SPT0_AFS	SPORT0 Channel A Frame Sync	B	PB_01
SPT0_AFS	SPORT0 Channel A Frame Sync	E	PE_01
SPT0_ATDV	SPORT0 Channel A Transmit Data Valid	B	PB_04

Table 11. ADSP-CM407F/ADSP-CM408F 176-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SPT0_BCLK	SPORT0 Channel B Clock	C	PC_08
SPT0_BD0	SPORT0 Channel B Data 0	C	PC_10
SPT0_BD1	SPORT0 Channel B Data 1	C	PC_11
SPT0_BFS	SPORT0 Channel B Frame Sync	C	PC_09
SPT0_BTDV	SPORT0 Channel B Transmit Data Valid	B	PB_12
SPT1_ACLK	SPORT1 Channel A Clock	A	PA_00
SPT1_AD0	SPORT1 Channel A Data 0	A	PA_02
SPT1_AD1	SPORT1 Channel A Data 1	A	PA_03
SPT1_AFS	SPORT1 Channel A Frame Sync	A	PA_01
SPT1_ATDV	SPORT1 Channel A Transmit Data Valid	B	PB_15
SPT1_BCLK	SPORT1 Channel B Clock	A	PA_04
SPT1_BD0	SPORT1 Channel B Data 0	A	PA_06
SPT1_BD1	SPORT1 Channel B Data 1	A	PA_07
SPT1_BFS	SPORT1 Channel B Frame Sync	A	PA_05
SPT1_BTDV	SPORT1 Channel B Transmit Data Valid	C	PC_00
SYS_BMODE0	Boot Mode Control 0	Not Muxed	SYS_BMODE0
SYS_BMODE1	Boot Mode Control 1	Not Muxed	SYS_BMODE1
SYS_CLKIN	Clock/Crystal Input	Not Muxed	SYS_CLKIN
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
SYS_DSWAKE0	Deep Sleep Wake-up 0	C	PC_06
SYS_DSWAKE1	Deep Sleep Wake-up 1	C	PC_07
SYS_DSWAKE2	Deep Sleep Wake-up 2	B	PB_14
SYS_DSWAKE3	Deep Sleep Wake-up 3	B	PB_13
$\overline{\text{SYS\_FAULT}}$	System Fault Output	Not Muxed	$\overline{\text{SYS\_FAULT}}$
$\overline{\text{SYS\_HWRST}}$	Processor Hardware Reset Control	Not Muxed	$\overline{\text{SYS\_HWRST}}$
$\overline{\text{SYS\_NMI}}$	Nonmaskable Interrupt	Not Muxed	$\overline{\text{SYS\_NMI}}$
$\overline{\text{SYS\_RESOUT}}$	Reset Output	Not Muxed	$\overline{\text{SYS\_RESOUT}}$
SYS_XTAL	Crystal Output	Not Muxed	SYS_XTAL
TM0_ACI1	TIMER0 Alternate Capture Input 1	B	PB_10
TM0_ACI1	TIMER0 Alternate Capture Input 1	D	PD_13
TM0_ACI2	TIMER0 Alternate Capture Input 2	B	PB_08
TM0_ACI2	TIMER0 Alternate Capture Input 2	D	PD_12
TM0_ACI3	TIMER0 Alternate Capture Input 3	B	PB_12
TM0_ACI3	TIMER0 Alternate Capture Input 3	D	PD_11
TM0_ACI4	TIMER0 Alternate Capture Input 4	B	PB_15
TM0_ACI4	TIMER0 Alternate Capture Input 4	D	PD_10
TM0_ACI5	TIMER0 Alternate Capture Input 5	C	PC_01
TM0_ACI5	TIMER0 Alternate Capture Input 5	D	PD_09
TM0_ACLK0	TIMER0 Alternate Clock 0	B	PB_13
TM0_ACLK1	TIMER0 Alternate Clock 1	B	PB_11
TM0_ACLK2	TIMER0 Alternate Clock 2	A	PA_11
TM0_ACLK3	TIMER0 Alternate Clock 3	A	PA_10
TM0_ACLK4	TIMER0 Alternate Clock 4	A	PA_09
TM0_ACLK5	TIMER0 Alternate Clock 5	A	PA_08
TM0_CLK	TIMER0 Clock	B	PB_06
TM0_CLK	TIMER0 Clock	D	PD_08

Table 18. ADSP-CM409F 212-Ball BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_D03	SMC0 Data 3	C	PC_11
SMC0_D04	SMC0 Data 4	A	PA_12
SMC0_D04	SMC0 Data 4	C	PC_12
SMC0_D05	SMC0 Data 5	A	PA_13
SMC0_D05	SMC0 Data 5	C	PC_13
SMC0_D06	SMC0 Data 6	A	PA_14
SMC0_D06	SMC0 Data 6	C	PC_14
SMC0_D07	SMC0 Data 7	A	PA_15
SMC0_D07	SMC0 Data 7	C	PC_15
SMC0_D08	SMC0 Data 8	B	PB_00
SMC0_D08	SMC0 Data 8	D	PD_00
SMC0_D09	SMC0 Data 9	B	PB_01
SMC0_D09	SMC0 Data 9	D	PD_01
SMC0_D10	SMC0 Data 10	B	PB_02
SMC0_D10	SMC0 Data 10	D	PD_02
SMC0_D11	SMC0 Data 11	B	PB_03
SMC0_D11	SMC0 Data 11	D	PD_03
SMC0_D12	SMC0 Data 12	B	PB_04
SMC0_D12	SMC0 Data 12	D	PD_04
SMC0_D13	SMC0 Data 13	B	PB_05
SMC0_D13	SMC0 Data 13	D	PD_05
SMC0_D14	SMC0 Data 14	B	PB_06
SMC0_D14	SMC0 Data 14	D	PD_06
SMC0_D15	SMC0 Data 15	B	PB_07
SMC0_D15	SMC0 Data 15	D	PD_07
SPI0_CLK	SPI0 Clock	C	PC_03
SPI0_D2	SPI0 Data 2	B	PB_10
SPI0_D3	SPI0 Data 3	B	PB_11
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_04
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_05
SPI0_RDY	SPI0 Ready	C	PC_02
$\overline{\text{SPI0\_SEL1}}$	SPI0 Slave Select Output 1	C	PC_06
$\overline{\text{SPI0\_SEL2}}$	SPI0 Slave Select Output 2	B	PB_13
$\overline{\text{SPI0\_SEL3}}$	SPI0 Slave Select Output 3	B	PB_14
$\overline{\text{SPI0\_SS}}$	SPI0 Slave Select Input	B	PB_14
SPI1_CLK	SPI1 Clock	C	PC_12
SPI1_MISO	SPI1 Master In, Slave Out	C	PC_13
SPI1_MOSI	SPI1 Master Out, Slave In	C	PC_14
$\overline{\text{SPI1\_SEL1}}$	SPI1 Slave Select Output 1	C	PC_15
$\overline{\text{SPI1\_SEL2}}$	SPI1 Slave Select Output 2	B	PB_06
$\overline{\text{SPI1\_SEL3}}$	SPI1 Slave Select Output 3	B	PB_07
$\overline{\text{SPI1\_SS}}$	SPI1 Slave Select Input	C	PC_15
SPT0_ACLK	SPORT0 Channel A Clock	B	PB_00
SPT0_ACLK	SPORT0 Channel A Clock	E	PE_00
SPT0_AD0	SPORT0 Channel A Data 0	B	PB_02
SPT0_AD0	SPORT0 Channel A Data 0	E	PE_02

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
ADC1_VIN01	a	na	none	none	none	VDD_ANA	Desc: Channel 1 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN02	a	na	none	none	none	VDD_ANA	Desc: Channel 2 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN03	a	na	none	none	none	VDD_ANA	Desc: Channel 3 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN04	a	na	none	none	none	VDD_ANA	Desc: Channel 4 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN05	a	na	none	none	none	VDD_ANA	Desc: Channel 5 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN06	a	na	none	none	none	VDD_ANA	Desc: Channel 6 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN07	a	na	none	none	none	VDD_ANA	Desc: Channel 7 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN08	a	na	none	none	none	VDD_ANA	Desc: Channel 8 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN09	a	na	none	none	none	VDD_ANA	Desc: Channel 9 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN10	a	na	none	none	none	VDD_ANA	Desc: Channel 10 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN11	a	na	none	none	none	VDD_ANA	Desc: Channel 11 Single-Ended Analog Input for ADC1 Notes: No notes.
BYP_A0	a	na	none	none	H	VDD_ANA	Desc: On-chip Analog Power Regulation Bypass Filter Node for ADC0 (see recommended bypass - Figure 4 on Page 6) Notes: This pin should never be loaded with resistive or inductive load or connected to anything but the recommended capacitor.
BYP_A1	a	na	none	none	H	VDD_ANA	Desc: On-chip Analog Power Regulation Bypass Filter Node for ADC1 (see recommended bypass - Figure 4 on Page 6) Notes: This pin should never be loaded with resistive or inductive load or connected to anything but the recommended capacitor.
BYP_D0	a	na	none	none	H	VDD_EXT	Desc: On-chip Digital Power Regulation Bypass Filter Node for Analog Subsystem (see recommended bypass - Figure 4 on Page 6) Notes: This pin should never be loaded with resistive or inductive load or connected to anything but the recommended capacitor.
DAC0_VOUT	a	na	none	none	L	VDD_ANA	Desc: Analog Voltage Output 0 Notes: No notes.
DAC1_VOUT	a	na	none	none	L	VDD_ANA	Desc: Analog Voltage Output 1 Notes: No notes.
GND	g	na	none	none	none	VDD_EXT and VDD_INT	Desc: Digital Ground Notes: No notes.
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground returns for VDD_ANA domain Notes: No notes.
GND_ANA0	g	na	none	none	none	VDD_ANA	Desc: Analog Ground return for VDD_ANA0 (see recommended bypass - Figure 4 on Page 6) Notes: No notes

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
GND_ANA1	g	na	none	none	none	VDD_ANA	Desc: Analog Ground return for VDD_ANA1 (see recommended bypass - Figure 4 on Page 6) Notes: No notes.
GND_ANA2	g	na	none	none	none	VDD_ANA	Desc: Analog Ground (see recommended bypass - Figure 4 on Page 6) Notes: No notes.
GND_ANA3	g	na	none	none	none	VDD_ANA	Desc: Analog Ground (see recommended bypass - Figure 4 on Page 6) Notes: No notes.
GND_VREF0	g	na	none	none	none	VDD_ANA	Desc: Ground return for VREF0 (see recommended bypass filter - Figure 4 on Page 6) Notes: No notes.
GND_VREF1	g	na	none	none	none	VDD_ANA	Desc: Ground return for VREF1 (see recommended bypass filter - Figure 4 on Page 6) Notes: No notes.
JTG_TCK/SWCLK	I/O	na	pd	pd	none	VDD_EXT	Desc: JTAG Clock/Serial Wire Clock Notes: No notes.
JTG_TDI	I/O	na	pu	pu	none	VDD_EXT	Desc: JTAG Serial Data In Notes: No notes.
JTG_TDO/SWO	I/O	A	none	none	none	VDD_EXT	Desc: JTAG Serial Data Out/Serial Wire Trace Output Notes: No notes.
JTG_TMS/SWDIO	I/O	A	pu	pu	none	VDD_EXT	Desc: JTAG Mode Select/Serial Wire Debug Data I/O Notes: No notes.
$\overline{\text{JTG\_TRST}}$	I/O	A	pu	pu	none	VDD_EXT	Desc: JTAG Reset Notes: Requires pull-up if using TRACE functionality; otherwise pull-down should be connected.
PA_00	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 0 | PWM0 Sync | SPORT1 Channel A Clock Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_01	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 1 | PWM0 Trip Input 0 | SPORT1 Channel A Frame Sync Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_02	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 2 | PWM0 Channel A High Side | SPORT1 Channel A Data 0 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_03	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 3 | PWM0 Channel A Low Side | SPORT1 Channel A Data 1 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_04	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 4 | PWM0 Channel B High Side | SPORT1 Channel B Clock Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PA_15	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 15 | PWM1 Channel B Low Side | TM0 Timer 3 | SMC0 Data 7 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_00	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 0 | PWM0 Channel D High Side | Embedded Trace Module Clock | SPORT0 Channel A Clock | SMC0 Data 8 | CNT0 Count Zero Marker Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_01	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 1 | PWM0 Channel D Low Side | Embedded Trace Module Data 0 | SPORT0 Channel A Frame Sync | SMC0 Data 9 | CNT0 Count Up and Direction Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_02	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 2 | PWM1 Channel D High Side | Embedded Trace Module Data 1 | SPORT0 Channel A Data 0 | SMC0 Data 10 | CNT0 Count Down and Gate Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_03	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 3 | PWM1 Channel D Low Side | Embedded Trace Module Data 2 | SPORT0 Channel A Data 1 | SMC0 Data 11 | CNT1 Count Zero Marker Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_04	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 4 | PWM2 Sync | UART0 Request to Send | SPORT0 Channel A Transmit Data Valid | SMC0 Data 12 | CNT1 Count Up and Direction Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_05	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 5 | PWM2 Trip Input 0 | UART0 Clear to Send | TM0 Timer 7 | SMC0 Data 13 | CNT1 Count Down and Gate Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_06	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 6 | PWM2 Channel A High Side | TM0 Common Clock | SPI1 Slave Select Output 2 | SMC0 Data 14 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_07	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 7 | PWM2 Channel A Low Side | TM0 Timer 0 | SPI1 Slave Select Output 3 | SMC0 Data 15 | Capture Timer0 Input 0 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Throughput					ADC0_$V_{IN, 00–11}$, ADC1_$V_{IN, 00–11}$
Conversion Rate			2.63	MSPS	
Acquisition time		150		ns	
AC ACCURACY					ADC0_$V_{IN, 00–11}$, ADC1_$V_{IN, 00–11}$
Characteristic					
ADSP-CM403F/ADSP-CM408F/ ADSP-CM409F					
Signal-to-Noise Ratio (SNR)[1]	80.25	81.25		dB	
Signal-to-(Noise + Distortion) Ratio (SINAD)[1]	80	81		dB	
Total Harmonic Distortion (THD)[1]		–92		dB	
Spurious-Free Dynamic Range (SFDR)[1]		90		dBc	
Dynamic Range	82	83		dB	$V_{IN} = V_{REF}/2$ (dc)
Effective Number of Bits (ENOB)	13.0	13.2		Bits	
ADSP-CM402F/ADSP-CM407F					
Signal-to-Noise Ratio (SNR)[1]	73	74		dB	
Signal-to-(Noise + Distortion) Ratio (SINAD)[1]	72	73		dB	
Total Harmonic Distortion (THD)[1]		–88		dB	
Spurious-Free Dynamic Range (SFDR)[1]		88		dBc	
Dynamic Range	74.5	75.5		dB	$V_{IN} = V_{REF}/2$ (dc)
Effective Number of Bits (ENOB)	11.6	11.8		Bits	
Channel-to-Channel Isolation		–95		dB	Any channel pair referenced on same ADC Selected channel = 1 kHz, unselected channel = 10 kHz
ADC-to-ADC Isolation		–100		dB	Any channel pair referenced on opposite ADC

[1] f_{IN} = 1 kHz, 0 V to 2.5 V input, 2.63 MSPS.

ADC Typical Performance Characteristics

V_{DD_ANA} = 3.3 V, V_{REF} = 2.5 V, T_J = 25°C, unless otherwise noted.

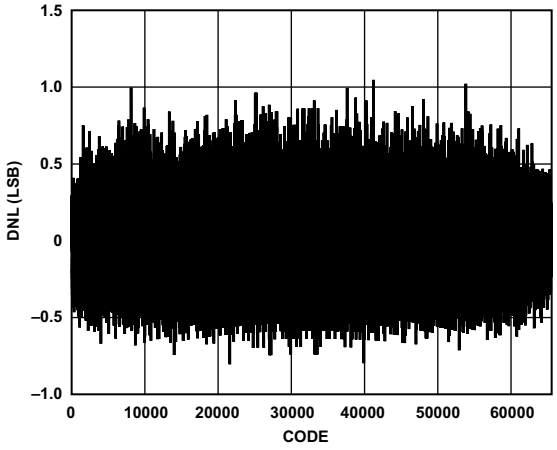

Figure 12. DNL vs. Code

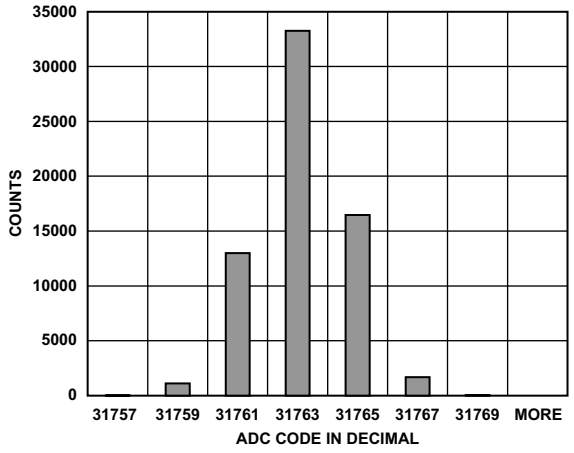

Figure 13. Histogram of DC Input at Code Center (Internal Reference)

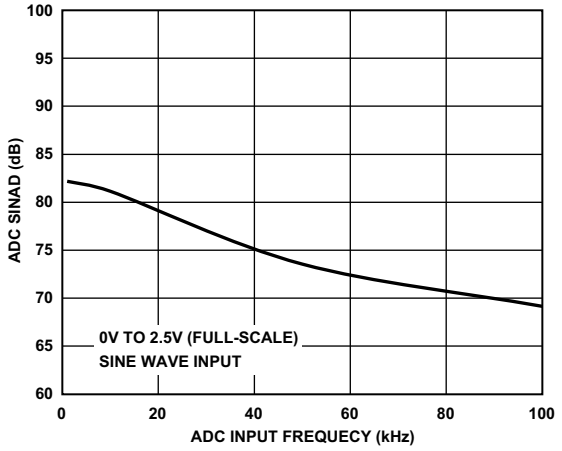

Figure 14. SINAD vs. Frequency, 0 V to 2.5 V Sine Wave Input

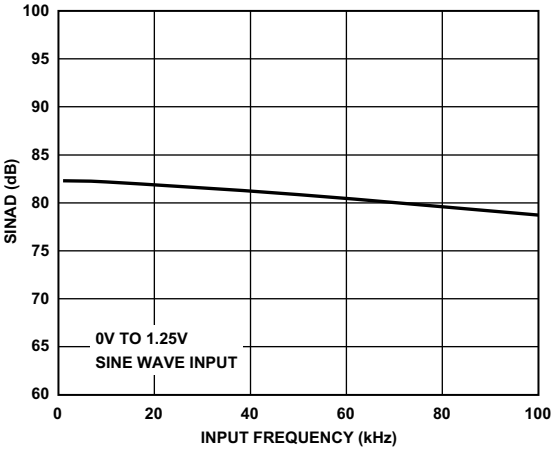

Figure 15. SINAD vs. Frequency, 0 V to 1.25 V Sine Wave Input

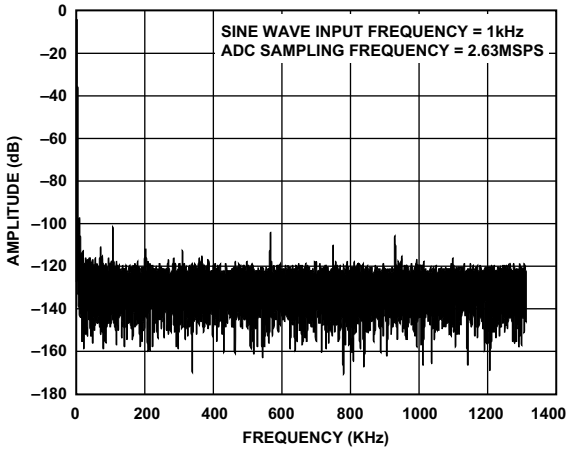

Figure 16. FFT Plot (Internal Reference)

FLASH SPECIFICATIONS

The Flash features include:

- 100,000 ERASE cycles per sector
- 20 years data retention

Flash PROGRAM/ERASE SUSPEND Command

Table 29 lists parameters for the Flash suspend command.

Table 29. Suspend Parameters

Parameter	Condition	Typ	Max	Unit
Erase to Suspend[1]	Sector erase or erase resume to erase suspend	700	–	µs
Program to Suspend[1]	Program resume to program suspend	5	–	µs
Subsector Erase to Suspend[1]	Subsector erase or subsector erase resume to erase suspend	50	–	µs
Suspend Latency[2]	Program	7	–	µs
Suspend Latency[2]	Subsector erase	15	–	µs
Suspend Latency[3]	Erase	15	–	µs

[1] Timing is not internally controlled.
[2] Any read command accepted.
[3] Any command except the following are accepted: sector, subsector, or bulk erase; write status register.

Flash AC Characteristics and Operating Conditions

Table 30 identifies Flash specific operating conditions.

Table 30. AC Characteristics and Operating Conditions

Parameter	Symbol	Min	Typ[1]	Max	Unit
Clock Frequency for All Commands other than Read (SPI-ER, QIO-SPI Protocol), T_J = 105°C	f_C	DC	–	100	MHz
Clock Frequency for All Commands other than Read (SPI-ER, QIO-SPI Protocol), T_J = 125°C	f_C	DC	–	97	MHz
Clock Frequency for Read Commands, T_J = 105°C	f_R	DC	–	50	MHz
Clock Frequency for Read Commands, T_J = 125°C	f_R	DC	–	45	MHz
Page Program Cycle Time (256 bytes)[2]	t_{PP}	–	0.5	5	ms
Page Program Cycle Time (n bytes)[2, 3]	t_{PP}	–	int(n/8) × 0.015	5	ms
Subsector Erase Cycle Time	t_{SSE}	–	0.3	1.5	sec
Sector Erase Cycle Time	t_{SE}	–	0.7	3	sec
Bulk Erase Cycle Time	t_{BE}	–	170	250	sec

[1] Typical values given for T_J = 25°C.
[2] When using the page program command to program consecutive bytes, optimized timings are obtained with one sequence including all the bytes vs. several sequences of only a few bytes (1 < n < 256).
[3] int(A) corresponds to the upper integer part of A. For example int(12/8) = 2, int(32/8) = 4 int(15.3) = 16.

The SPT_TDV output signal becomes active in SPORT multichannel mode. During transmit slots (enabled with active channel selection registers) the SPT_TDV is asserted for communication with external devices.

Table 45. Serial Ports—Transmit Data Valid (TDV)

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DRDVEN}	Data-Valid Enable Delay from Drive Edge of External Clock[1]	2		ns
t_{DFDVEN}	Data-Valid Disable Delay from Drive Edge of External Clock[1]		14	ns
t_{DRDVIN}	Data-Valid Enable Delay from Drive Edge of Internal Clock[1]	–1		ns
t_{DFDVIN}	Data-Valid Disable Delay from Drive Edge of Internal Clock[1]		3.5	ns

[1] Referenced to drive edge.

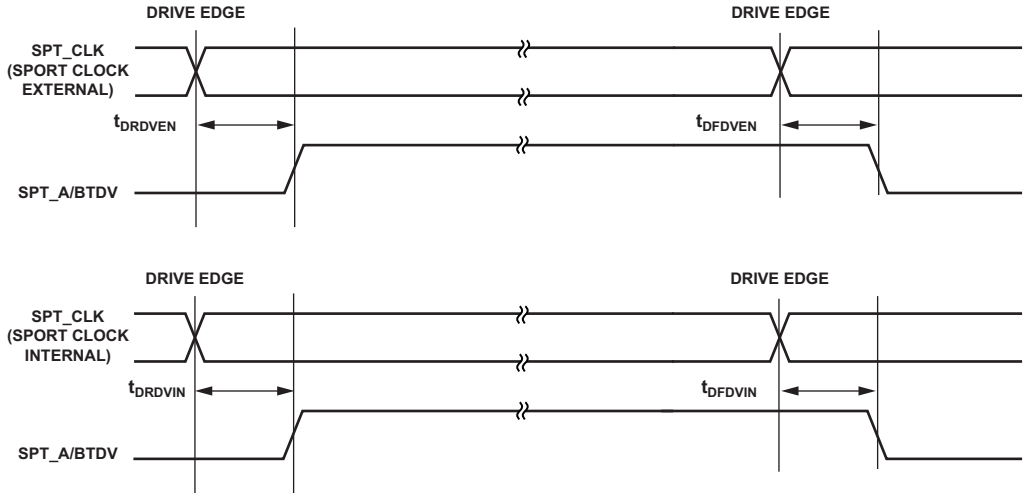

Figure 33. Serial Ports—Transmit Data Valid Internal and External Clock

Serial Peripheral Interface (SPI) Port—Master Timing

Table 47 and Figure 35 describe serial peripheral interface (SPI) port master operations.When internally generated, the programmed SPI clock ($f_{SPICLKPROG}$) frequency in MHz is set by the following equation where BAUD is a field in the SPI_CLK register that can be set from 0 to 65,535:

$$f_{SPICLKPROG} = \frac{f_{SCLK}}{(BAUD + 1)}$$

$$t_{SPICLKPROG} = \frac{1}{f_{SPICLKPROG}}$$

Note that:

- In dual mode data transmit, the SPI_MISO signal is also an output.
- In quad mode data transmit, the SPI_MISO, SPI_D2, and SPI_D3 signals are also outputs.
- In dual mode data receive, the SPI_MOSI signal is also an input.
- In quad mode data receive, the SPI_MOSI, SPI_D2, and SPI_D3 signals are also inputs.

Table 47. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SPI_CLK Edge (Data Input Setup)	3.2		ns
t_{HSPIDM}	SPI_CLK Sampling Edge to Data Input Invalid	1.3		ns
Switching Characteristics				
t_{SDSCIM}	$\overline{\text{SPI\_SEL}}$ low to First SPI_CLK Edge for CPHA = 1[1]	[t_{SCLK} – 2] or [18]		ns
	$\overline{\text{SPI\_SEL}}$ low to First SPI_CLK Edge for CPHA = 0[1]	[1.5 × t_{SCLK} – 2] or [13]		ns
t_{SPICHM}	SPI_CLK High Period [2]	0.5 × $t_{SPICLKPROG}$ – 1		ns
t_{SPICLM}	SPI_CLK Low Period [2]	0.5 × $t_{SPICLKPROG}$ – 1		ns
t_{SPICLK}	SPI_CLK Period[2]	$t_{SPICLKPROG}$ – 1		ns
t_{HDSM}	Last SPI_CLK Edge to $\overline{\text{SPI\_SEL}}$ High for CPHA = 1[1]	[1.5 × t_{SCLK} –2] or [13]		ns
	Last SPI_CLK Edge to $\overline{\text{SPI\_SEL}}$ High for CPHA = 0[1]	[t_{SCLK} –2] or [18]		ns
t_{SPITDM}	Sequential Transfer Delay[1, 3]	[t_{SCLK} – 1] or [19]		ns
$t_{DDSPIDM}$	SPI_CLK Edge to Data Out Valid (Data Out Delay)		2.6	ns
$t_{HDSPIDM}$	SPI_CLK Edge to Data Out Invalid (Data Out Hold)	–1.5		ns

[1] Whichever is greater.
[2] See Table 27 Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{SPICLKPROG}$.
[3] Applies to sequential mode with STOP ≥ 1.

Serial Peripheral Interface (SPI) Port—SPI_RDY Master Timing

SPI_RDY is used to provide flow control. The CPOL and CPHA bits are set in SPI_CTL, while LEADX, LAGX, and STOP are in SPI_DLY.

Table 52. SPI Port—SPI_RDY Master Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SRDYSCKM0}$	Minimum Setup Time for SPI_RDY De-assertion in Master Mode Before Last Valid SPI_CLK Edge of Valid Data Transfer to Block Subsequent Transfer with CPHA = 0	$(2 + 2 \times BAUD^{1}) \times t_{SCLK} + 10$		ns
$t_{SRDYSCKM1}$	Minimum Setup Time for SPI_RDY De-assertion in Master Mode Before Last Valid SPI_CLK Edge of Valid Data Transfer to Block Subsequent Transfer with CPHA = 1	$(2 + 2 \times BAUD^{1}) \times t_{SCLK} + 10$		ns
Switching Characteristics				
$t_{SRDYSCKM}$	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA/CPOL = 0 and BAUD = 0 (STOP, LEAD, LAG = 0)	$4.5 \times t_{SCLK}$	$5.5 \times t_{SCLK} + 10$	ns
	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA/CPOL = 1 and BAUD = 0 (STOP, LEAD, LAG = 0)	$4 \times t_{SCLK}$	$5 \times t_{SCLK} + 10$	ns
	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA/CPOL = 0 and BAUD ≥ 1 (STOP, LEAD, LAG = 0)	$(1 + 1.5 \times BAUD^{1}) \times t_{SCLK}$	$(2 + 2.5 \times BAUD^{1}) \times t_{SCLK} + 10$	ns
	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA/CPOL = 1 and BAUD ≥ 1 (STOP, LEAD, LAG = 0)	$(1 + 1 \times BAUD^{1}) \times t_{SCLK}$	$(2 + 2 \times BAUD^{1}) \times t_{SCLK} + 10$	ns

[1] BAUD value set using the SPI_CLK.BAUD bits. BAUD value = SPI_CLK.BAUD bits + 1.

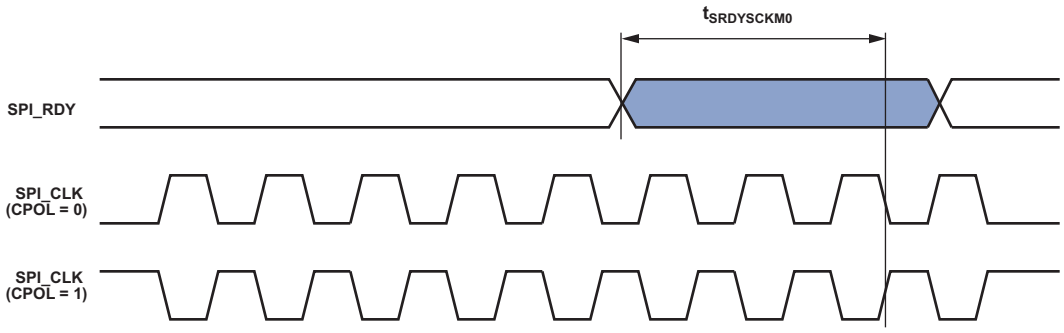

Figure 41. SPI_RDY Setup Before SPI_CLK with CPHA = 0

Table 63. 10/100 Ethernet MAC Controller (EMAC) Timing: RMII Station Management

Parameter[1]		Min	Max	Unit
Timing Requirements				
t_{MDIOS}	ETHx_MDIO Input Valid to ETHx_MDC Rising Edge (Setup)	14		ns
t_{MDCIH}	ETHx_MDC Rising Edge to ETHx_MDIO Input Invalid (Hold)	0		ns
Switching Characteristics				
t_{MDCOV}	ETHx_MDC Falling Edge to ETHx_MDIO Output Valid		t_{SCLK} + 5	ns
t_{MDCOH}	ETHx_MDC Falling Edge to ETHx_MDIO Output Invalid (Hold)	t_{SCLK} – 2.5		ns

[1] ETHx_MDC/ETHx_MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. ETHx_MDC is an output clock whose minimum period is programmable as a multiple of the system clock SCLK. ETHx_MDIO is a bidirectional data line.

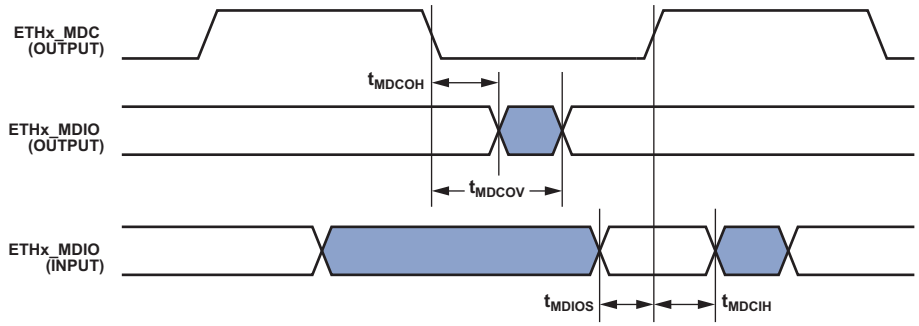

Figure 54. 10/100 Ethernet MAC Controller Timing: RMII Station Management

Debug Interface (JTAG Emulation Port) Timing

Table 67 and Figure 58 provide I/O timing, related to the debug interface (JTAG emulator port).

Table 67. JTAG Emulation Port Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	JTG_TCK Period	20		ns
t_{STAP}	JTG_TDI, JTG_TMS Setup Before JTG_TCK High	4		ns
t_{HTAP}	JTG_TDI, JTG_TMS Hold After JTG_TCK High	4		ns
t_{SSYS}	System Inputs Setup Before JTG_TCK High[1]	12		ns
t_{HSYS}	System Inputs Hold After JTG_TCK High[1]	5		ns
t_{TRSTW}	$\overline{\text{JTG\_TRST}}$ Pulse Width (Measured in JTG_TCK cycles)[2]	4		t_{TCK}
Switching Characteristics				
t_{DTDO}	JTG_TDO Delay from JTG_TCK Low		13.5	ns
t_{DSYS}	System Outputs Delay After JTG_TCK Low[3]		17	ns

[1] System inputs = PA_xx, PB_xx, PC_xx, PD_xx, PE_xx, PF_xx, SYS_BMODEx, $\overline{\text{SYS\_HWRST}}$, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_NMI}}$, TWI0_SCL, TWI0_SDA, USB_ID.
[2] 50 MHz maximum.
[3] System outputs = PA_xx, PB_xx, PC_xx, PD_xx, PE_xx, PF_xx, $\overline{\text{SMC0\_AMS0}}$, $\overline{\text{SMC0\_ARE}}$, $\overline{\text{SMC0\_AWE}}$, SYS_CLKOUT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_RESOUT}}$.

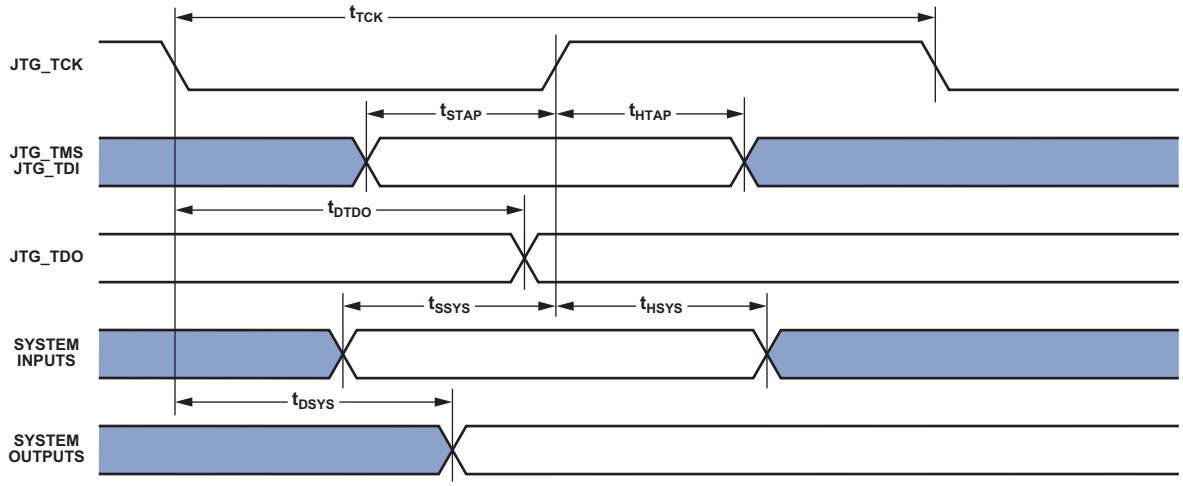

Figure 58. JTAG Emulation Port Timing

Table 76. ADSP-CM409F 212-Ball BGA Ball Assignments (Alphabetical by Ball Name) (Continued)

Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.
GND	B02	PA_07	G01	PD_13	C13	VDD_EXT	D08
GND	C03	PA_08	G03	PD_14	A14	VDD_EXT	D09
GND	C14	PA_09	F01	PD_15	B14	VDD_EXT	D10
GND	H07	PA_10	D01	PE_00	A15	VDD_EXT	D11
GND	H08	PA_11	D02	PE_01	B16	VDD_EXT	L03
GND	H09	PA_12	E03	PE_02	A16	VDD_EXT	R07
GND	J07	PA_13	D03	PE_03	A17	VDD_EXT	R09
GND	J08	PA_14	A02	PE_04	V17	VDD_EXT	T04
GND	J09	PA_15	B04	PE_05	V16	VDD_EXT	T05
GND	K07	PB_00	A03	PE_06	U16	VDD_EXT	T14
GND	K08	PB_01	B05	PE_07	V15	VDD_EXT	T15
GND	K09	PB_02	B07	PE_08	U15	VDD_INT	D07
GND	L07	PB_03	A07	PE_09	U14	VDD_INT	D12
GND	L08	PB_04	C08	PE_10	V14	VDD_INT	H03
GND	L09	PB_05	B08	PE_11	T13	VDD_INT	R08
GND	R11	PB_06	A08	PE_12	V13	VDD_INT	R10
GND	T03	PB_07	C09	PE_13	V11	VDD_VREG	J03
GND	U02	PB_08	B09	PE_14	U11	VREF0	H16
GND	V01	PB_09	A09	PE_15	T10	VREF1	L16
GND_ANA	A18	PB_10	C10	PF_00	U10	VREG_BASE	K03
GND_ANA	B17	PB_11	T12	PF_01	V10		
GND_ANA	C16	PB_12	U13	PF_02	T09		
GND_ANA	F16	PB_13	U12	PF_03	U09		
GND_ANA	H11	PB_14	V12	PF_04	V09		