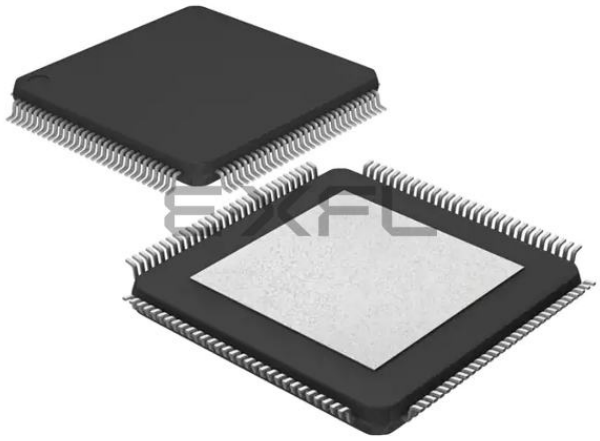

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	CAN, I²C, SPI, SPORT, UART/USART
Clock Rate	100MHz
Non-Volatile Memory	FLASH (256kB)
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP Exposed Pad
Supplier Device Package	120-LQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-cm402cswz-ff

PROCESSOR INFRASTRUCTURE

The following sections provide information on the primary infrastructure components of the ADSP-CM40xF processors.

DMA Controllers (DDEs)

The processor contains 17 independent and concurrently operating peripheral DMA channels plus two MDMA streams. DDE Channel 0 to Channel 16 are for peripherals and Channel 17 to Channel 20 are for MDMA.

System Event Controller (SEC)

The SEC manages the enabling and routing of system fault sources through its integrated fault management unit.

Trigger Routing Unit (TRU)

The TRU provides system-level sequence control without core intervention. The TRU maps trigger masters (generators of triggers) to trigger slaves (receivers of triggers). Slave endpoints can be configured to respond to triggers in various ways. Common applications enabled by the TRU include:

- Initiating the ADC sampling periodically in each PWM period or based on external events
- Automatically triggering the start of a DMA sequence after a sequence from another DMA channel completes
- Software triggering
- Synchronization of concurrent activities

Pin Interrupts (PINT)

Every port pin on the processor can request interrupts in either an edge-sensitive or a level-sensitive manner with programmable polarity. Interrupt functionality is decoupled from GPIO operation. Six system-level interrupt channels (PINT0 to PINT5) are reserved for this purpose. Each of these interrupt channels can manage up to 32 interrupt pins. The assignment from pin to interrupt is not performed on a pin-by-pin basis. Rather, groups of eight pins (half ports) can be flexibly assigned to interrupt channels.

Every pin interrupt channel features a special set of 32-bit memory-mapped registers that enable half-port assignment and interrupt management. This includes masking, identification, and clearing of requests. These registers also enable access to the respective pin states and use of the interrupt latches, regardless of whether the interrupt is masked or not. Most control registers feature multiple MMR address entries to write-one-to-set or write-one-to-clear them individually.

General-Purpose I/O (GPIO)

Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers:

- GPIO direction control register—Specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers —A write one to modify mechanism allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins.
- GPIO interrupt mask registers—Allow each individual GPIO pin to function as an interrupt to the processor. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers—Specify whether individual pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant.

Pin Multiplexing

The processor supports a flexible multiplexing scheme that multiplexes the GPIO pins with various peripherals. A maximum of five peripherals plus GPIO functionality is shared by each GPIO pin. All GPIO pins have a bypass path feature—that is, when the output enable and the input enable of a GPIO pin are both active, the data signal before the pad driver is looped back to the receive path for the same GPIO pin.

For more information, see:

- ADSP-CM402F/ADSP-CM403F GPIO Multiplexing for 120-Lead LQFP on Page 27.
- ADSP-CM407F/ADSP-CM408F GPIO Multiplexing for 176-Lead LQFP on Page 37.
- ADSP-CM409F GPIO Multiplexing for 212-Ball BGA on Page 48.

MEMORY ARCHITECTURE

The internal and external memory of the ADSP-CM40xF processor is shown in Figure 7 and described in the following sections.

ARM Cortex-M4 Memory Subsystem

The memory map of the ADSP-CM40xF family is based on the Cortex-M4 model from ARM. By retaining the standardized memory mapping, it becomes easier to port applications across M4 platforms. Only the physical implementation of memories inside the model differs from other vendors.

ADSP-CM40xF application development is typically based on memory blocks across CODE/SRAM and external memory regions. Sufficient internal memory is available via internal SRAM and internal flash. Additional external memory devices may be interfaced via the SMC asynchronous memory port, as well as through the SPI0 serial memory interface.

Code Region

Accesses in this region (0x0000_0000 to 0x1FFF_FFFF) are performed by the core on its ICODE and DCODE interfaces, and they target the memory and cache resources within the Cortex-M4F platform integration component.

- **Boot ROM.** A 32K byte boot ROM executed at system reset. This space supports read-only access by the M4F core only. Note that ROM memory contents cannot be modified by the user.

System Region

Accesses in this region (0xE000_0000 to 0xF7FF_FFFF) are performed by the ARM Cortex-M4F core on its SYS interface, and are handled within the Cortex-M4F platform. The MPU may be programmed to limit access to this space to privileged mode only.

- **CoreSight ROM.** The ROM table entries point to the debug components of the processor.
- **ARM PPB Peripherals.** This space is defined by ARM and occupies the bottom 256K byte of the SYS region (0xE000_0000 to 0xE004_0000). The space supports read/write access by the M4F core to the ARM core's internal peripherals (MPU, ITM, DWT, FPB, SCS, TPIU, ETM) and the CoreSight ROM. It is not accessible by system DMA.
- **Platform Control Registers.** This space has registers within the Cortex-M4F platform integration component that control the ARM core, its memory, and the code cache. It is accessible by the M4F core via its SYS port (but is not accessible by system DMA).

Static Memory Controller (SMC)

The SMC can be programmed to control up to four banks of external memories or memory-mapped devices, with very flexible timing parameters. On ADSP-CM407F/CM408F/CM409F processors, each bank can occupy a 32M byte segment regardless of the size of the device used.

Booting (BOOT)

The processor has several mechanisms for automatically loading internal and external memory after a reset. The boot mode is defined by the SYS_BMODE input pins dedicated for this purpose. There are two categories of boot modes. In master boot modes, the processor actively loads data from a serial memory. In slave boot modes, the processor receives data from external host devices.

The boot modes are shown in Table 2. These modes are implemented by the SYS_BMODE bits of the RCU_CTL register and are sampled during power-on resets and software-initiated resets.

Table 2. Boot Modes

SYS_BMODE[1:0] Setting	Description
00	No Boot/Idle. The processor does not boot. Rather the boot kernel executes an IDLE instruction.
01	Flash Boot. Boot from integrated Flash memory through the SPI2.
10	SPI Slave Boot. Boot through the SPI0 peripheral configured as a slave.
11	UART Boot. Boot through the UART0 peripheral configured as a slave.

SYSTEM ACCELERATION

The following sections describe the system acceleration blocks of the ADSP-CM40xF processors.

Harmonic Analysis Engine (HAE)

The harmonic analysis engine (HAE) block receives 8 kHz input samples from two source signals whose frequencies are between 45 Hz and 65 Hz. The HAE will then process the input samples and produce output results. The output results consist of power quality measurements of the fundamental and up to 12 selectable harmonics.

Sinus Cardinalis Filter (SINC)

The SINC module processes four bit streams using a pair of configurable SINC filters for each bitstream. The purpose of the primary SINC filter of each pair is to produce the filtered and decimated output for the pair. The output may be decimated to any integer rate between 8 and 256 times lower than the input rate. Greater decimation allows greater removal of noise and therefore greater ENOB.

Optional additional filtering outside the SINC module may be used to further increase ENOB. The primary SINC filter output is accessible through transfer to processor memory, or to another peripheral, via DMA.

Each of the four channels is also provided with a low-latency secondary filter with programmable positive and negative overrange detection comparators. These limit detection events can be used to interrupt the core, generate a trigger, or signal a system fault.

SECURITY FEATURES

The processor provides lightweight security functionality which protects sensitive data and IP located in the internal flash memory. It includes password-protected slave boot modes (SPI and UART), as well as password-protected JTAG/SWD debug interfaces. One of the safeguards of the security feature is the ability to perform bulk erase of the entire flash memory. Another security measure provides the ability to control which boot modes are allowed so as to protect the flash contents from untrusted or non-secure boot modes. Programs can enable or disable security features depending upon the secure header configured in internal flash memory.

CAUTION
This product includes security features that can be used to protect embedded nonvolatile memory contents and prevent execution of unauthorized code. When security is enabled on this device (either by the ordering party or the subsequent receiving parties), the ability of Analog Devices to conduct failure analysis on returned devices is limited. Contact Analog Devices for details on the failure analysis limitations for this device.

The timer unit can be used in conjunction with the UARTs and the CAN controller to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timer can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to external signals. Timer events can also trigger other peripherals via the TRU (for instance, to signal a fault).

Watchdog Timer (WDT)

The core includes a 32-bit timer, which may be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state, via generation of a general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error. Optionally, the fault management unit (FMU) can directly initiate the processor reset upon the watchdog expiry event.

Capture Timer (CPTMR)

The processor includes three instants of capture timers (CPTMR) to capture total on time. Each capture timer captures total on time of the input signal between two leading edges of the input trigger signal. Capture timer inputs to all the timers come from external pins and the input trigger signal comes from trigger routing unit (TRU).

The core of the timer is a 32-bit counter which is reset at leading edge of the trigger and counts when the input signal level is active. The total on time of the input signal is captured from the counter at the leading edge of the trigger pulse. Capture timer can generate data interrupts to the processor core at leading edges of trigger pulses and status interrupts to indicate counter overflow condition.

3-Phase Pulse Width Modulator Unit (PWM)

The pulse width modulator (PWM) unit provides duty cycle and phase control capabilities to a resolution of one system clock cycle (SCLK). The heightened precision PWM (HPPWM) module provides increased performance to the PWM unit by increasing its resolution by several bits, resulting in enhanced precision levels. Additional features include:

- 16-bit center-based PWM generation unit
- Programmable PWM pulse width
- Single/double update modes
- Programmable dead time and switching frequency
- Twos-complement implementation which permits smooth transition to full on and full off states
- Dedicated asynchronous PWM trip signal

The eight PWM output signals (per PWM unit) consist of four high-side drive signals and four low-side drive signals. The polarity of a generated PWM signal can be set with software, so that either active high or active low PWM patterns can be produced.

Each PWM block integrates a flexible and programmable 3-phase PWM waveform generator that can be programmed to generate the required switching patterns to drive a 3-phase voltage source inverter for ac induction motor (ACIM) or permanent magnet synchronous motor (PMSM) control. In addition, the PWM block contains special functions that considerably simplify the generation of the required PWM switching patterns for control of the electronically commutated motor (ECM) or permanent magnet synchronous motor (PMSM) control. Software can enable a special mode for switched reluctance motors (SRM).

Each PWM unit features a dedicated asynchronous trip pin which (when brought low) instantaneously places all PWM outputs in the off state.

Serial Ports (SPORTs)

The synchronous serial ports provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices, Inc., audio codecs, ADCs, and DACs. The serial ports are made up of two data lines per direction, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels.For full-duplex operation, two half SPORTs can work in conjunction with clock and frame sync signals shared internally through the SPMUX block. In some operation modes, SPORT supports gated clock.

Serial ports operate in six modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode
- Right-justified mode

General-Purpose Counters

The 32-bit counter can operate in general-purpose up/down count modes and can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumbwheels. Count direction is either controlled by a level-sensitive input pin or by two edge detectors.

A third counter input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumb wheels. All three pins have a programmable debouncing circuit.

The GP counter can also support a programmable M/N frequency scaling of the CNT_CUD and CNT_CDG pins onto output pins in quadrature encoding mode.

Internal signals forwarded to each general-purpose timer enable these timers to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmable count values are exceeded.

Serial Peripheral Interface Ports (SPI)

The processor contains the SPI-compatible port that allows the processor to communicate with multiple SPI-compatible devices.

In its simplest mode, the SPI interface uses three pins for transferring data: two data pins master output-slave input and master input-slave output (SPI_MOSI and SPI_MISO) and a clock pin, SPI_CLK. A SPI chip select input pin ($\overline{\text{SPI\_SS}}$) lets other SPI devices select the processor, and three SPI chip select output pins (SPI_SELn) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI provides a full-duplex, synchronous serial interface, which supports both master and slave modes and multimaster environments.

In a multimaster or multislave SPI system, the MOSI and MISO data output pins can be configured to behave as open drain outputs (using the ODM bit) to prevent contention and possible damage to pin drivers. An external pull-up resistor is required on both the MOSI and MISO pins when this option is selected.

When ODM is set and the SPI is configured as a master, the MOSI pin is three-stated when the data driven out on MOSI is a logic high. The MOSI pin is not three-stated when the driven data is a logic low. Similarly, when ODM is set and the SPI is configured as a slave, the MISO pin is three-stated if the data driven out on MISO is a logic high.

The SPI port's baud rate and clock phase/polarities are programmable, and it has integrated DMA channels for both transmit and receive data streams.

Universal Asynchronous Receiver/Transmitter Ports (UART)

The processor provides full-duplex universal asynchronous receiver/transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, and none, even, or odd parity. Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multi-drop bus (MDB) systems. A frame is terminated by one, one and a half, two or two and a half stop bits.

The UART ports support automatic hardware flow control through the clear to send (CTS) input and request to send (RTS) output with programmable assertion FIFO levels.

To help support the local interconnect network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable inter-frame space.

The capabilities of the UARTs are further extended with support for the infrared data association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

2-Wire Controller Interface (TWI)

The processor includes a 2-wire interface (TWI) module for providing a simple exchange method of control data between multiple devices. The TWI module is compatible with the widely used I^2C bus standard. The TWI module offers the capabilities of simultaneous master and slave operation and support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (TWI_SCL) and data (TWI_SDA) and supports the protocol at speeds up to 400k bits/sec. The TWI interface pins are compatible with 5 V logic levels.

Additionally, the TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

Controller Area Network (CAN)

The CAN controller implements the CAN 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well suited for control applications due to its capability to communicate reliably over a network. This is because the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The CAN controller offers the following features:

- 32 mailboxes (8 receive only, 8 transmit only, 16 configurable for receive or transmit).
- Dedicated acceptance masks for each mailbox.
- Additional data filtering on first two bytes.
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats.
- Support for remote frames.
- Active or passive network support.
- Interrupts, including: TX complete, RX complete, error and global.

An additional crystal is not required to supply the CAN clock, as the CAN clock is derived from a system clock through a programmable divider.

10/100 Ethernet MAC (EMAC)

The processor can directly connect to a network by way of an embedded fast Ethernet media access controller (MAC) that supports both 10-BaseT (10M bits/sec) and 100-BaseT (100M bits/sec) operation. The 10/100 Ethernet MAC peripheral on the processor is fully compliant to the IEEE 802.3-2002 standard. It

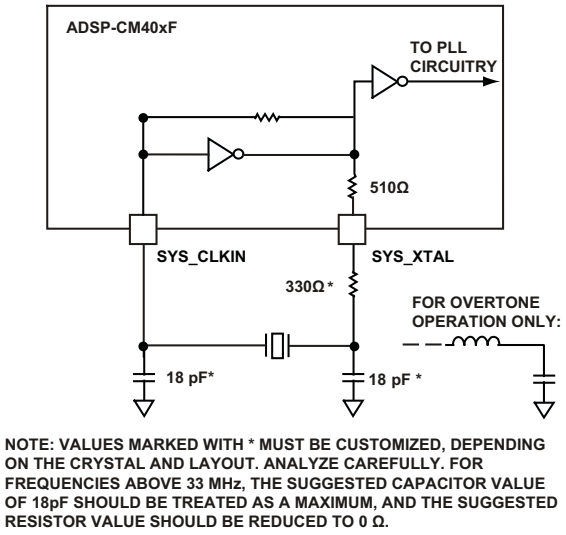

Figure 8. External Crystal Connection

The two capacitors and the 330 Ω series resistor shown in Figure 8 fine tune phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 8 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over temperature range.

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit as shown in Figure 8. A design procedure for third-overtone operation is discussed in detail in application note (EE-168) "Using Third Overtone Crystals with the ADSP-218x DSP" (www.analog.com/ee-168).

Oscillator Watchdog

A programmable oscillator watchdog unit is provided to allow verification of proper startup and harmonic mode of the external crystal. This allows the user to specify the expected frequency of oscillation, and to enable detection of non-oscillation and improper-oscillation faults. These events can be routed to the SYS_FAULT output pin and/or to cause a reset of the part.

Clock Generation Unit (CGU)

The clock generation unit (CGU) generates all on-chip clocks and synchronization signals. Multiplication factors are programmed to the PLLs to define the PLLCLK frequency. Programmable values divide the PLLCLK frequency to generate the core clock (CCLK), the system clocks (SCLK), and the output clock (OCLK). This is illustrated in Figure 10 on Page 64.

Writing to the CGU control registers does not affect the behavior of the PLL immediately. Registers are first programmed with a new value, and the PLL logic executes the changes so that it transitions smoothly from the current conditions to the new ones.

SYS_CLKIN oscillations start when power is applied to the VDD_EXT pins. The rising edge of SYS_HWRST can be applied as soon as all voltage supplies are within specifications (see Operating Conditions on Page 64), and SYS_CLKIN oscillations are stable.

Clock Out/External Clock

A SYS_CLKOUT output pin has programmable options to output divided-down versions of the on-chip clocks, including USB clocks. By default, the SYS_CLKOUT pin drives a buffered version of the SYS_CLKIN input. Clock generation faults (for example PLL unlock) may trigger a reset by hardware.

SYS_CLKOUT can be used to output one of several different clocks used on the processor. The clocks shown in Table 4 can be outputs from SYS_CLKOUT.

Table 4. SYS_CLKOUT Source and Divider Options

Clock Source	Divider
CCLK (Core Clock)	By 4
OCLK (Output Clock)	Programmable
USBCLK	Programmable
CLKBUF	None, direct from SYS_CLKIN

Power Management

As shown in Table 5 and Figure 4 on Page 6, the processor requires three different power domains, VDD_INT, VDD_EXT, and VDD_ANA. By isolating the internal logic of the processor into its own power domain, separate from other I/O, the processor can take advantage of dynamic power management without affecting the other I/O devices. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate Specifications table for processor operating conditions; even if the feature/peripheral is not used.

The dynamic power management feature of the processor allows the processor's core clock frequency (f_{CCLK}) to be dynamically controlled.

Table 5. Power Domains

Power Domain	V_{DD} Range
All Internal Logic	V_{DD_INT}
Digital I/O	V_{DD_EXT}
Analog	V_{DD_ANA}

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation. For more information on power pins, see Operating Conditions on Page 64.

Table 7. ADSP-CM402F/ADSP-CM403F 120-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
CNT0_OUTB	CNT0 Output Divider B	B	PB_14
CNT0_UD	CNT0 Count Up and Direction	B	PB_01
CNT0_ZM	CNT0 Count Zero Marker	B	PB_00
CNT1_DG	CNT1 Count Down and Gate	B	PB_05
CNT1_UD	CNT1 Count Up and Direction	B	PB_04
CNT1_ZM	CNT1 Count Zero Marker	B	PB_03
CPTMR0_IN0	CPTMR0 Capture Timer0 Input 0	B	PB_07
CPTMR0_IN1	CPTMR0 Capture Timer0 Input 1	B	PB_08
CPTMR0_IN2	CPTMR0 Capture Timer0 Input 2	B	PB_09
DAC0_VOUT	Analog Voltage Output 0	Not Muxed	DAC0_VOUT
DAC1_VOUT	Analog Voltage Output 1	Not Muxed	DAC1_VOUT
GND	Digital Ground	Not Muxed	GND
GND_ANA0	Analog Ground return for VDD_ANA0 (see recommended bypass - Figure 4 on Page 6)	Not Muxed	GND_ANA0
GND_ANA1	Analog Ground return for VDD_ANA1 (see recommended bypass - Figure 4 on Page 6)	Not Muxed	GND_ANA1
GND_ANA2	Analog Ground (see recommended bypass - Figure 4 on Page 6)	Not Muxed	GND_ANA2
GND_ANA3	Analog Ground (see recommended bypass - Figure 4 on Page 6)	Not Muxed	GND_ANA3
GND_VREF0	Ground return for VREF0 (see recommended bypass filter - Figure 4 on Page 6)	Not Muxed	GND_VREF0
GND_VREF1	Ground return for VREF1 (see recommended bypass filter - Figure 4 on Page 6)	Not Muxed	GND_VREF1
JTG_TCK/SWCLK	JTAG Clock/Serial Wire Clock	Not Muxed	JTG_TCK/SWCLK
JTG_TDI	JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO/SWO	JTAG Serial Data Out/Serial Wire Trace Output	Not Muxed	JTG_TDO/SWO
JTG_TMS/SWDIO	JTAG Mode Select/Serial Wire Debug Data I/O	Not Muxed	JTG_TMS/SWDIO
$\overline{\text{JTG\_TRST}}$	JTAG Reset	Not Muxed	$\overline{\text{JTG\_TRST}}$
PA_00-PA_15	Port A Positions 0 – 15	A	PA_00 – PA_15
PB_00-PB_15	Port B Positions 0 – 15	B	PB_00 – PB_15
PC_00-PC_07	Port C Positions 0 – 7	C	PC_00 – PC_07
PWM0_AH	PWM0 Channel A High Side	A	PA_02
PWM0_AL	PWM0 Channel A Low Side	A	PA_03
PWM0_BH	PWM0 Channel B High Side	A	PA_04
PWM0_BL	PWM0 Channel B Low Side	A	PA_05
PWM0_CH	PWM0 Channel C High Side	A	PA_06
PWM0_CL	PWM0 Channel C Low Side	A	PA_07
PWM0_DH	PWM0 Channel D High Side	B	PB_00
PWM0_DL	PWM0 Channel D Low Side	B	PB_01
PWM0_SYNC	PWM0 Sync	A	PA_00
$\overline{\text{PWM0\_TRIP0}}$	PWM0 Trip Input 0	A	PA_01
PWM1_AH	PWM1 Channel A High Side	A	PA_12
PWM1_AL	PWM1 Channel A Low Side	A	PA_13
PWM1_BH	PWM1 Channel B High Side	A	PA_14
PWM1_BL	PWM1 Channel B Low Side	A	PA_15
PWM1_CH	PWM1 Channel C High Side	A	PA_08
PWM1_CL	PWM1 Channel C Low Side	A	PA_09
PWM1_DH	PWM1 Channel D High Side	B	PB_02

Table 18. ADSP-CM409F 212-Ball BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_D03	SMC0 Data 3	C	PC_11
SMC0_D04	SMC0 Data 4	A	PA_12
SMC0_D04	SMC0 Data 4	C	PC_12
SMC0_D05	SMC0 Data 5	A	PA_13
SMC0_D05	SMC0 Data 5	C	PC_13
SMC0_D06	SMC0 Data 6	A	PA_14
SMC0_D06	SMC0 Data 6	C	PC_14
SMC0_D07	SMC0 Data 7	A	PA_15
SMC0_D07	SMC0 Data 7	C	PC_15
SMC0_D08	SMC0 Data 8	B	PB_00
SMC0_D08	SMC0 Data 8	D	PD_00
SMC0_D09	SMC0 Data 9	B	PB_01
SMC0_D09	SMC0 Data 9	D	PD_01
SMC0_D10	SMC0 Data 10	B	PB_02
SMC0_D10	SMC0 Data 10	D	PD_02
SMC0_D11	SMC0 Data 11	B	PB_03
SMC0_D11	SMC0 Data 11	D	PD_03
SMC0_D12	SMC0 Data 12	B	PB_04
SMC0_D12	SMC0 Data 12	D	PD_04
SMC0_D13	SMC0 Data 13	B	PB_05
SMC0_D13	SMC0 Data 13	D	PD_05
SMC0_D14	SMC0 Data 14	B	PB_06
SMC0_D14	SMC0 Data 14	D	PD_06
SMC0_D15	SMC0 Data 15	B	PB_07
SMC0_D15	SMC0 Data 15	D	PD_07
SPI0_CLK	SPI0 Clock	C	PC_03
SPI0_D2	SPI0 Data 2	B	PB_10
SPI0_D3	SPI0 Data 3	B	PB_11
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_04
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_05
SPI0_RDY	SPI0 Ready	C	PC_02
$\overline{\text{SPI0\_SEL1}}$	SPI0 Slave Select Output 1	C	PC_06
$\overline{\text{SPI0\_SEL2}}$	SPI0 Slave Select Output 2	B	PB_13
$\overline{\text{SPI0\_SEL3}}$	SPI0 Slave Select Output 3	B	PB_14
$\overline{\text{SPI0\_SS}}$	SPI0 Slave Select Input	B	PB_14
SPI1_CLK	SPI1 Clock	C	PC_12
SPI1_MISO	SPI1 Master In, Slave Out	C	PC_13
SPI1_MOSI	SPI1 Master Out, Slave In	C	PC_14
$\overline{\text{SPI1\_SEL1}}$	SPI1 Slave Select Output 1	C	PC_15
$\overline{\text{SPI1\_SEL2}}$	SPI1 Slave Select Output 2	B	PB_06
$\overline{\text{SPI1\_SEL3}}$	SPI1 Slave Select Output 3	B	PB_07
$\overline{\text{SPI1\_SS}}$	SPI1 Slave Select Input	C	PC_15
SPT0_ACLK	SPORT0 Channel A Clock	B	PB_00
SPT0_ACLK	SPORT0 Channel A Clock	E	PE_00
SPT0_AD0	SPORT0 Channel A Data 0	B	PB_02
SPT0_AD0	SPORT0 Channel A Data 0	E	PE_02

ADSP-CM40xF DESIGNER QUICK REFERENCE

Table 25 provides a quick reference summary of pin related information for circuit board design. The columns in this table provide the following information:

- Signal Name: The Signal Name column in the table includes the signal name for every pin and (where applicable) the GPIO multiplexed pin function for every pin.
- Pin Type: The Type column in the table identifies the I/O type or supply type of the pin. The abbreviations used in this column are na (none), I/O (input/output), a (analog), s (supply), and g (ground).
- Driver Type: The Driver Type column in the table identifies the driver type used by the pin. The driver types are defined in the output drive currents section of this data sheet.
- Internal Termination: The Int Term column in the table specifies the termination present when the processor is not in the reset state. The abbreviations used in this column are wk (weak keeper, weakly retains previous value driven on the pin), pu (pull-up), or pd (pull-down).
- Reset Termination: The Reset Term column in the table specifies the termination present when the processor is in the reset state. The abbreviations used in this column are wk (weak keeper, weakly retains previous value driven on the pin), pu (pull-up), or pd (pull-down).
- Reset Drive: The Reset Drive column in the table specifies the active drive on the signal when the processor is in the reset state.
- Power Domain: The Power Domain column in the table specifies the power supply domain in which the signal resides.
- Description and Notes: The Description and Notes column in the table identifies any special requirements or characteristics for the signal. If no special requirements are listed the signal may be left unconnected if it is not used. Also, for multiplexed general-purpose I/O pins, this column identifies the functions available on the pin.

Table 25. ADSP-CM40xF Designer Quick Reference

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
ADC0_VIN00	a	na	none	none	none	VDD_ANA	Desc: Channel 0 Single-Ended Analog Input for ADC0 Notes: No notes.
ADC0_VIN01	a	na	none	none	none	VDD_ANA	Desc: Channel 1 Single-Ended Analog Input for ADC0 Notes: No notes.
ADC0_VIN02	a	na	none	none	none	VDD_ANA	Desc: Channel 2 Single-Ended Analog Input for ADC0 Notes: No notes.
ADC0_VIN03	a	na	none	none	none	VDD_ANA	Desc: Channel 3 Single-Ended Analog Input for ADC0 Notes: No notes.
ADC0_VIN04	a	na	none	none	none	VDD_ANA	Desc: Channel 4 Single-Ended Analog Input for ADC0 Notes: No notes.
ADC0_VIN05	a	na	none	none	none	VDD_ANA	Desc: Channel 5 Single-Ended Analog Input for ADC0 Notes: No notes.
ADC0_VIN06	a	na	none	none	none	VDD_ANA	Desc: Channel 6 Single-Ended Analog Input for ADC0 Notes: No notes.
ADC0_VIN07	a	na	none	none	none	VDD_ANA	Desc: Channel 7 Single-Ended Analog Input for ADC0 Notes: No notes.
ADC0_VIN08	a	na	none	none	none	VDD_ANA	Desc: Channel 8 Single-Ended Analog Input for ADC0 Notes: No notes.
ADC0_VIN09	a	na	none	none	none	VDD_ANA	Desc: Channel 9 Single-Ended Analog Input for ADC0 Notes: No notes.
ADC0_VIN10	a	na	none	none	none	VDD_ANA	Desc: Channel 10 Single-Ended Analog Input for ADC0 Notes: No notes.
ADC0_VIN11	a	na	none	none	none	VDD_ANA	Desc: Channel 11 Single-Ended Analog Input for ADC0 Notes: No notes.
ADC1_VIN00	a	na	none	none	none	VDD_ANA	Desc: Channel 0 Single-Ended Analog Input for ADC1 Notes: No notes.

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
ADC1_VIN01	a	na	none	none	none	VDD_ANA	Desc: Channel 1 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN02	a	na	none	none	none	VDD_ANA	Desc: Channel 2 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN03	a	na	none	none	none	VDD_ANA	Desc: Channel 3 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN04	a	na	none	none	none	VDD_ANA	Desc: Channel 4 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN05	a	na	none	none	none	VDD_ANA	Desc: Channel 5 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN06	a	na	none	none	none	VDD_ANA	Desc: Channel 6 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN07	a	na	none	none	none	VDD_ANA	Desc: Channel 7 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN08	a	na	none	none	none	VDD_ANA	Desc: Channel 8 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN09	a	na	none	none	none	VDD_ANA	Desc: Channel 9 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN10	a	na	none	none	none	VDD_ANA	Desc: Channel 10 Single-Ended Analog Input for ADC1 Notes: No notes.
ADC1_VIN11	a	na	none	none	none	VDD_ANA	Desc: Channel 11 Single-Ended Analog Input for ADC1 Notes: No notes.
BYP_A0	a	na	none	none	H	VDD_ANA	Desc: On-chip Analog Power Regulation Bypass Filter Node for ADC0 (see recommended bypass - Figure 4 on Page 6) Notes: This pin should never be loaded with resistive or inductive load or connected to anything but the recommended capacitor.
BYP_A1	a	na	none	none	H	VDD_ANA	Desc: On-chip Analog Power Regulation Bypass Filter Node for ADC1 (see recommended bypass - Figure 4 on Page 6) Notes: This pin should never be loaded with resistive or inductive load or connected to anything but the recommended capacitor.
BYP_D0	a	na	none	none	H	VDD_EXT	Desc: On-chip Digital Power Regulation Bypass Filter Node for Analog Subsystem (see recommended bypass - Figure 4 on Page 6) Notes: This pin should never be loaded with resistive or inductive load or connected to anything but the recommended capacitor.
DAC0_VOUT	a	na	none	none	L	VDD_ANA	Desc: Analog Voltage Output 0 Notes: No notes.
DAC1_VOUT	a	na	none	none	L	VDD_ANA	Desc: Analog Voltage Output 1 Notes: No notes.
GND	g	na	none	none	none	VDD_EXT and VDD_INT	Desc: Digital Ground Notes: No notes.
GND_ANA	g	na	none	none	none	VDD_ANA	Desc: Analog Ground returns for VDD_ANA domain Notes: No notes.
GND_ANA0	g	na	none	none	none	VDD_ANA	Desc: Analog Ground return for VDD_ANA0 (see recommended bypass - Figure 4 on Page 6) Notes: No notes

SPECIFICATIONS

For information about product specifications, contact your Analog Devices representative.

OPERATING CONDITIONS

Parameter		Test Conditions/Comments	Min	Nominal	Max	Unit
V_{DD_INT}	Digital Internal Supply Voltage	$f_{CCLK} \le 240$ MHz	1.14	1.2	1.26	V
V_{DD_EXT}[1]	Digital External Supply Voltage		3.13	3.3	3.47	V
V_{DD_ANA}[1]	Analog Supply Voltage		3.13	3.3	3.47	V
V_{IH}[2]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	2.0			V
V_{IH_CLKIN}[3]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	2.2			V
V_{IHTWI}[4, 5]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	0.7 × $V_{VBUSTWI}$		$V_{VBUSTWI}$	V
V_{IL}[2]	Low Level Input Voltage	V_{DD_EXT} = 3.13 V			0.8	V
V_{ILTWI}[4, 5]	Low Level Input Voltage	V_{DD_EXT} = 3.13 V			0.3 × $V_{VBUSTWI}$	V
T_J	Junction Temperature	$T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C

[1] Must remain powered (even if the associated function is not used).
[2] Parameter value applies to all input and bidirectional signals except TWI signals and USB0 signals.
[3] Parameter applies to SYS_CLKIN signal.
[4] Parameter applies to TWI_SDA and TWI_SCL.
[5] TWI signals are pulled up to V_{BUSTWI}. See Table 26.

Table 26. TWI_VSEL Selections and V_{DD_EXT}/V_{BUSTWI}

TWI_DT Setting	V_{DD_EXT} Nominal	V_{BUSTWI} Min	V_{BUSTWI} Nom	V_{BUSTWI} Max	Unit
TWI000[1]	3.30	3.13	3.30	3.47	V
TWI100	3.30	4.75	5.00	5.25	V

[1] Designs must comply with the V_{DD_EXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

Clock Related Operating Conditions

Table 27 describes the core clock, system clock, and peripheral clock timing requirements. The data presented in the tables applies to all speed grades found in the Ordering Guide on Page 124 except where expressly noted. Figure 10 provides a graphical representation of the various clocks and their available multiplier or divider values.

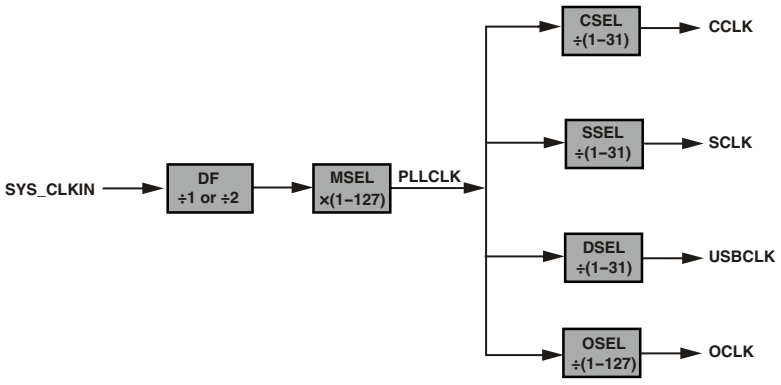

Figure 10. Clock Relationships and Divider Values

DAC Specifications

Typical values assume V_{DD_ANA} = 3.3 V, V_{REF} = 2.5 V.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG OUTPUT					DAC0_VOUT, DAC1_VOUT
Characteristic					
Output Voltage Range		0.1 to 2.5		V	
Output Impedance		0.6		Ω	Normal operation
		2		Ω	DAC @ full scale
		10		Ω	DAC @ zero scale
Update Rate			50	kHz	
Short Circuit Current to GND		30		mA	
Short Circuit Current to V_{DD}		30		mA	
STATIC PERFORMANCE					
DC ACCURACY					R_L = 500 Ω, C_L = 100 pF
Characteristic					
Resolution		12		Bits	
Differential Nonlinearity (DNL)		±0.99	–0.99/+1.2	LSB	Guaranteed monotonic
Integral Nonlinearity (INL)		±2.0	±3.5	LSB	
Offset Error		±1.0		mV	Measured at Code 0x000
Gain Error		±4.0		% FSR	% of full scale, measured at Code 0xFFF
DC Isolation			50	uV	Static output of DAC0_VOUT while DAC1_VOUT toggles 0 to full scale
DYNAMIC PERFORMANCE					
AC ACCURACY					R_L = 500 Ω, C_L = 100 pF
Characteristic					
Signal-to-Noise Ratio (SNR)		67	65	dB	
Signal-to-(Noise + Distortion) Ratio (SINAD)		62	59	dB	
Total Harmonic Distortion		63		dB	
Dynamic Range		68		dB	
Settling Time		1.5		µs	From ¼ to ¾ full scale
Slew Rate		1.5		V/µs	
D/A Glitch Energy		8		nV-s	Measured when code changes from 0x7FF to 0x800

DAC Typical Performance Characteristics

V_{DD_ANA} = 3.3 V, V_{REF} = 2.5 V, T_J = 25°C, unless otherwise noted.

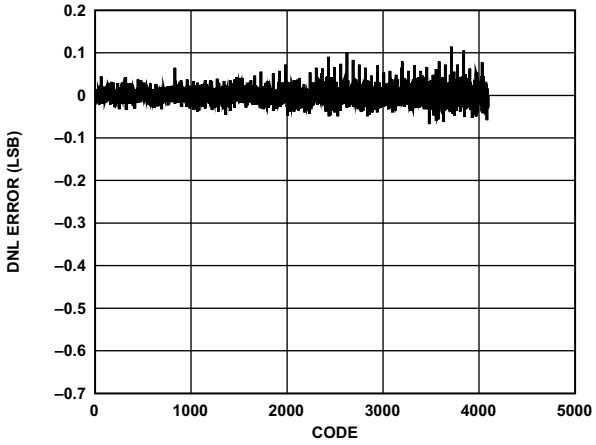

Figure 21. DAC DNL Error vs. Code

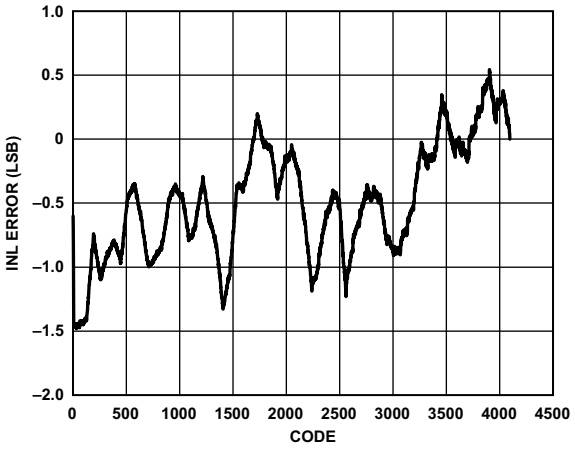

Figure 22. DAC INL Error vs. Code

FLASH SPECIFICATIONS

The Flash features include:

- 100,000 ERASE cycles per sector
- 20 years data retention

Flash PROGRAM/ERASE SUSPEND Command

Table 29 lists parameters for the Flash suspend command.

Table 29. Suspend Parameters

Parameter	Condition	Typ	Max	Unit
Erase to Suspend[1]	Sector erase or erase resume to erase suspend	700	–	µs
Program to Suspend[1]	Program resume to program suspend	5	–	µs
Subsector Erase to Suspend[1]	Subsector erase or subsector erase resume to erase suspend	50	–	µs
Suspend Latency[2]	Program	7	–	µs
Suspend Latency[2]	Subsector erase	15	–	µs
Suspend Latency[3]	Erase	15	–	µs

[1] Timing is not internally controlled.
[2] Any read command accepted.
[3] Any command except the following are accepted: sector, subsector, or bulk erase; write status register.

Flash AC Characteristics and Operating Conditions

Table 30 identifies Flash specific operating conditions.

Table 30. AC Characteristics and Operating Conditions

Parameter	Symbol	Min	Typ[1]	Max	Unit
Clock Frequency for All Commands other than Read (SPI-ER, QIO-SPI Protocol), T_J = 105°C	f_C	DC	–	100	MHz
Clock Frequency for All Commands other than Read (SPI-ER, QIO-SPI Protocol), T_J = 125°C	f_C	DC	–	97	MHz
Clock Frequency for Read Commands, T_J = 105°C	f_R	DC	–	50	MHz
Clock Frequency for Read Commands, T_J = 125°C	f_R	DC	–	45	MHz
Page Program Cycle Time (256 bytes)[2]	t_{PP}	–	0.5	5	ms
Page Program Cycle Time (n bytes)[2, 3]	t_{PP}	–	int(n/8) × 0.015	5	ms
Subsector Erase Cycle Time	t_{SSE}	–	0.3	1.5	sec
Sector Erase Cycle Time	t_{SE}	–	0.7	3	sec
Bulk Erase Cycle Time	t_{BE}	–	170	250	sec

[1] Typical values given for T_J = 25°C.
[2] When using the page program command to program consecutive bytes, optimized timings are obtained with one sequence including all the bytes vs. several sequences of only a few bytes (1 < n < 256).
[3] int(A) corresponds to the upper integer part of A. For example int(12/8) = 2, int(32/8) = 4 int(15.3) = 16.

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 31 may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 31. Absolute Maximum Ratings

Parameter	Rating
Internal Supply Voltage (V_{DD_INT})	–0.33 V to +1.32 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.33 V to +3.63 V
Analog Supply Voltage (V_{DD_ANA})	–0.33 V to +3.63 V
Digital Input Voltage[1, 2]	–0.33 V to +3.63 V
TWI Digital Input Voltage[1, 2, 3]	–0.33 V to +5.50 V
Digital Output Voltage Swing	–0.33 V to V_{DD_EXT} + 0.5 V
Analog Input Voltage[4]	–0.33 V to +3.63 V
Voltage Reference Input Voltage (V_{REF0}, V_{REF1})[4]	–0.33 V to +2.75 V
USB0_Dx Input	–0.33 V to +5.25 V
USB0_VBUS Input Voltage	–0.33 V to +6.00 V
I_{OH}/I_{OL} Current per Signal[1]	6 mA (max)
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	+125°C

[1] Applies to 100% transient duty cycle. For other duty cycles, see Table 32.
[2] Applies only when V_{DD_EXT} is within specifications. When V_{DD_EXT} is outside specifications, the range is V_{DD_EXT} ± 0.2 V.
[3] Applies to pins TWI_SCL and TWI_SDA.
[4] Applies only when V_{DD_ANA} is within specification. When V_{DD_ANA} is outside specifications, the range is V_{DD_ANA} ± 0.2 V.

Table 32. Maximum Duty Cycle for Input Transient Voltage[1]

Maximum Duty Cycle (%)[2]	V_{IN} Min (V)[3]	V_{IN} Max (V)[3]
100	–0.33	+3.63
50	–0.46	+3.78
40	–0.52	+3.85
25	–0.63	+3.96
20	–0.67	+3.99
15	–0.70	+4.03
10	–0.73	+4.07

[1] Applies to all signal pins with the exception of SYS_CLKIN, SYS_XTAL, USB0_DP, USB0_DM, USB0_VBUS, and TWI signals.
[2] Applies only when V_{DD_EXT} is within specifications. When V_{DD_EXT} is outside specifications, the range is V_{DD_EXT} ± 0.2 V.
[3] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the specified voltages, and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 23 and Table 33 provides details about package branding. For a complete listing of product availability, see Ordering Guide on Page 124.

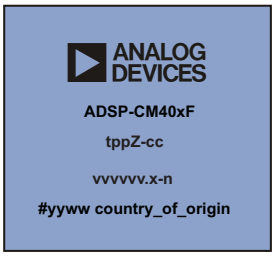

Figure 23. Product Information on Package[1]

[1] Exact brand may differ, depending on package type.

Table 33. Package Brand Information

Brand Key	Field Description
ADSP-CM40xF	Product model
t	Temperature range
pp	Package type
Z	RoHS compliant designation
cc	See Ordering Guide
vvvvvv.x	Assembly lot code
n	Silicon revision
yyww	Date code

The SPT_TDV output signal becomes active in SPORT multichannel mode. During transmit slots (enabled with active channel selection registers) the SPT_TDV is asserted for communication with external devices.

Table 45. Serial Ports—Transmit Data Valid (TDV)

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DRDVEN}	Data-Valid Enable Delay from Drive Edge of External Clock[1]	2		ns
t_{DFDVEN}	Data-Valid Disable Delay from Drive Edge of External Clock[1]		14	ns
t_{DRDVIN}	Data-Valid Enable Delay from Drive Edge of Internal Clock[1]	–1		ns
t_{DFDVIN}	Data-Valid Disable Delay from Drive Edge of Internal Clock[1]		3.5	ns

[1] Referenced to drive edge.

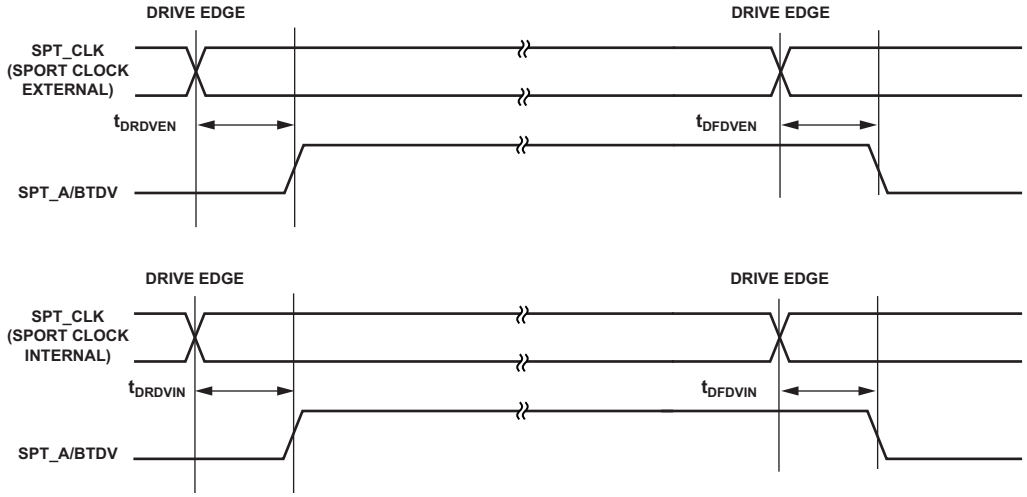

Figure 33. Serial Ports—Transmit Data Valid Internal and External Clock

Serial Peripheral Interface (SPI) Port—SPI_RDY Slave Timing

Table 49. SPI Port—SPI_RDY Slave Timing

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DSPISCKRDYSR}$	SPI_RDY De-assertion from Last Input SPI_CLK Edge in Slave Mode Receive	$3 \times t_{SCLK}$	$4 \times t_{SCLK} + 10$	ns
$t_{DSPISCKRDYST}$	SPI_RDY De-assertion from Last Input SPI_CLK Edge in Slave Mode Transmit	$4 \times t_{SCLK}$	$5 \times t_{SCLK} + 10$	ns

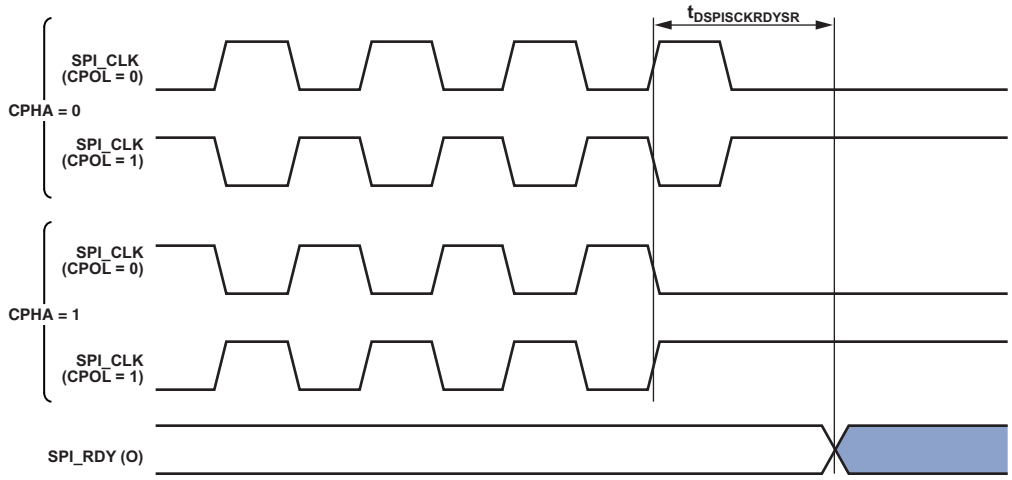

Figure 37. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Receive (FCCH = 0)

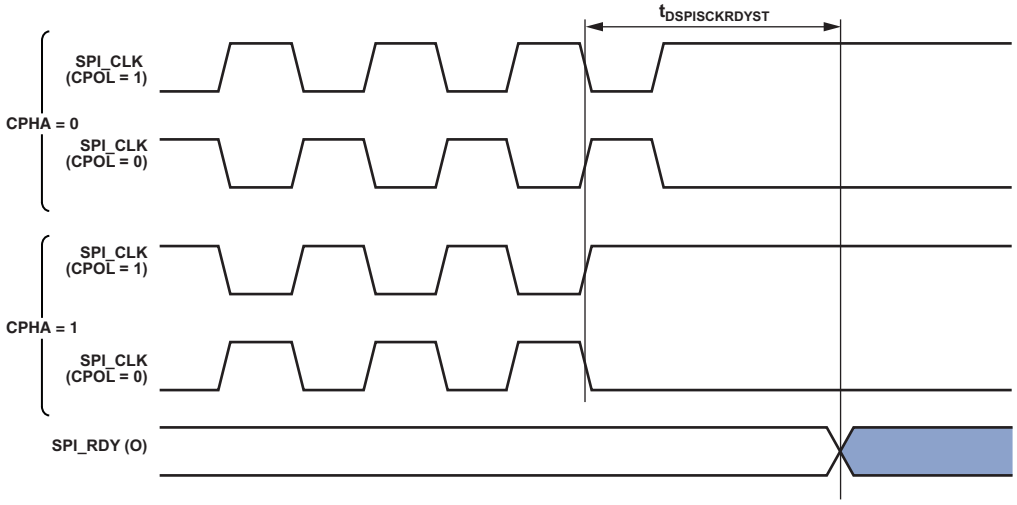

Figure 38. SPI_RDY De-assertion from Valid Input SPI_CLK Edge in Slave Mode Transmit (FCCH = 1)

10/100 Ethernet MAC Controller (EMAC) Timing

Table 61 through Table 63 and Figure 52 through Figure 54 describe the 10/100 Ethernet MAC controller operations. Note the externally generated Ethernet MAC clock is called $f_{REFCLKEXT}$:

$$t_{REFCLKEXT} = \frac{1}{f_{REFCLKEXT}}$$

Table 61. 10/100 Ethernet MAC Controller (EMAC) Timing: RMII Receive Signal

Parameter[1]		Min	Max	Unit
Timing Requirements				
t_{REFCLK}	ETHx_REFCLK Period[2]	$t_{REFCLKEXT}$ – 1%		ns
$t_{REFCLKW}$	ETHx_REFCLK Width[2]	$t_{REFCLKEXT}$ × 35%	$t_{REFCLKEXT}$ × 65%	ns
$t_{REFCLKIS}$	Rx Input Valid to RMII ETHx_REFCLK Rising Edge (Data In Setup)	4		ns
$t_{REFCLKIH}$	RMII ETHx_REFCLK Rising Edge to Rx Input Invalid (Data In Hold)	2.0		ns

[1] RMII inputs synchronous to RMII REF_CLK are ERxDx, RMII CRS_DV, and ERxER.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external REF_CLK. For the external REF_CLK maximum frequency see the $t_{REFCLKEXT}$ specification in Table 27 Clock Related Operating Conditions.

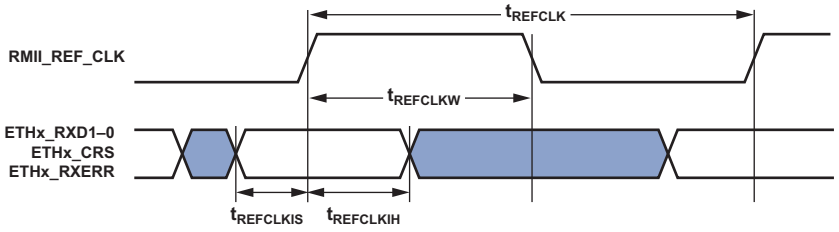

Figure 52. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal

Table 62. 10/100 Ethernet MAC Controller (EMAC) Timing: RMII Transmit Signal

Parameter[1]		Min	Max	Unit
Switching Characteristics				
$t_{REFCLKOV}$	RMII ETHx_REFCLK Rising Edge to Transmit Output Valid (Data Out Valid)		14	ns
$t_{REFCLKOH}$	RMII ETHx_REFCLK Rising Edge to Transmit Output Invalid (Data Out Hold)	2		ns

[1] RMII outputs synchronous to RMII REF_CLK are ETxDx.

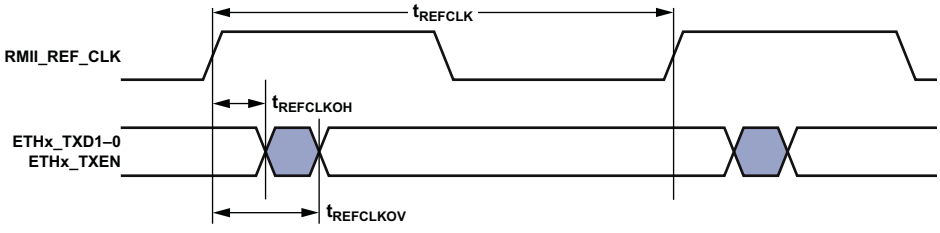

Figure 53. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

Table 63. 10/100 Ethernet MAC Controller (EMAC) Timing: RMII Station Management

Parameter[1]		Min	Max	Unit
Timing Requirements				
t_{MDIOS}	ETHx_MDIO Input Valid to ETHx_MDC Rising Edge (Setup)	14		ns
t_{MDCIH}	ETHx_MDC Rising Edge to ETHx_MDIO Input Invalid (Hold)	0		ns
Switching Characteristics				
t_{MDCOV}	ETHx_MDC Falling Edge to ETHx_MDIO Output Valid		t_{SCLK} + 5	ns
t_{MDCOH}	ETHx_MDC Falling Edge to ETHx_MDIO Output Invalid (Hold)	t_{SCLK} – 2.5		ns

[1] ETHx_MDC/ETHx_MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. ETHx_MDC is an output clock whose minimum period is programmable as a multiple of the system clock SCLK. ETHx_MDIO is a bidirectional data line.

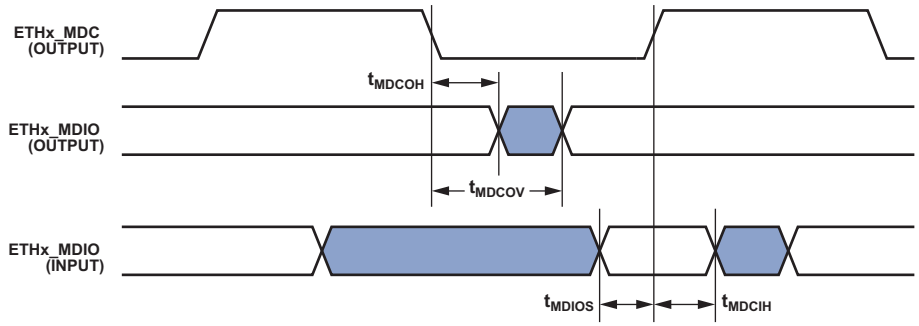

Figure 54. 10/100 Ethernet MAC Controller Timing: RMII Station Management

PROCESSOR TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 59 shows the measurement point for ac measurements (except output enable/disable). The measurement point V_{MEAS} is $V_{DD\_EXT}/2$ for V_{DD_EXT} (nominal) = 3.3 V.

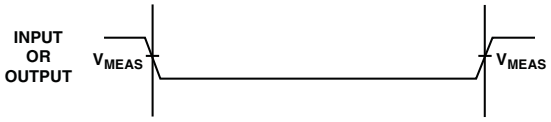

Figure 59. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time, t_{ENA}, is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 60. If multiple pins are enabled, the measurement value is that of the first pin to start driving.

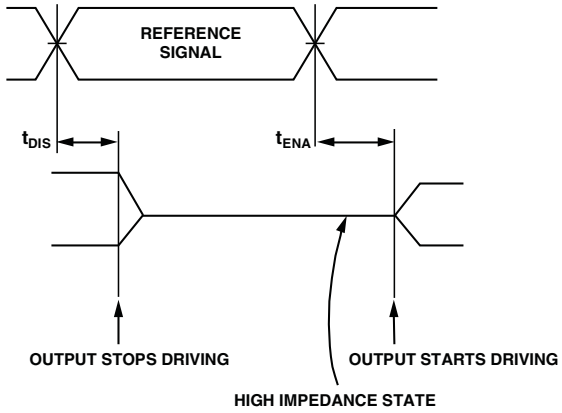

Figure 60. Output Enable/Disable

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time, t_{DIS}, is the interval from when a reference signal reaches a high or low voltage level to the point when the output stops driving as shown on the left side of Figure 60.

OUTPUT DRIVE CURRENTS

Figure 61 and Figure 62 show typical current-voltage characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

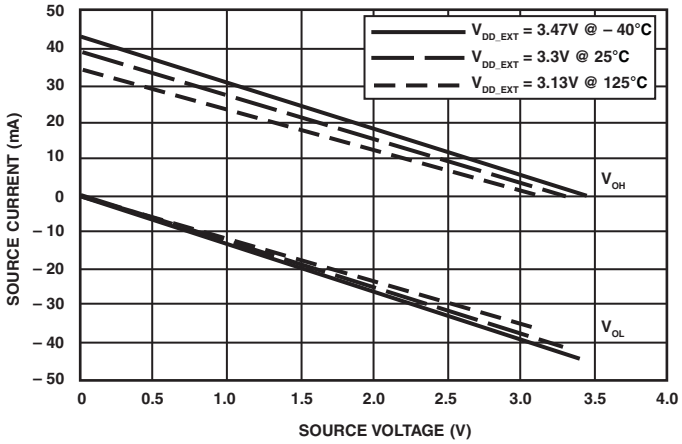

Figure 61. Driver Type A Current

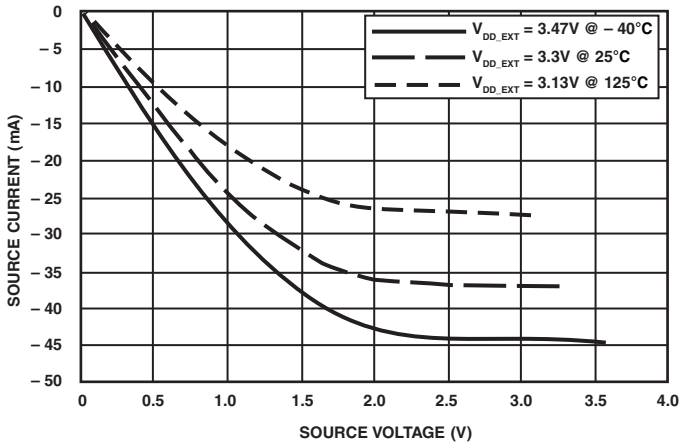

Figure 62. Driver Type B Current

Capacitive Loading

Output delay, hold, enable, and disable times are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 63). V_{LOAD} is equal to $(V_{DD\_EXT})/2$.

ADSP-CM402F/ADSP-CM403F 120-LEAD LQFP LEAD ASSIGNMENTS

Table 71 lists the 120-lead LQFP package by lead number and
Table 72 lists the 120-lead LQFP package by pin name.

Table 71. ADSP-CM402F/ADSP-CM403F120-Lead LQFP Lead Assignments (Numerical by Lead Number)

Lead No.	Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.	Pin Name
1	PA_13	32	JTG_TRST	63	ADC1_VIN05	94	DAC0_VOUT
2	VDD_EXT	33	JTG_TDO/SWO	64	ADC1_VIN06	95	VDD_EXT
3	PA_12	34	JTG_TMS/SWDIO	65	ADC1_VIN07	96	VDD_INT
4	PA_11	35	PC_07	66	ADC1_VIN08	97	VDD_EXT
5	PA_10	36	VDD_EXT	67	ADC1_VIN09	98	GND
6	PA_09	37	PC_06	68	ADC1_VIN10	99	SYS_NMI
7	PA_08	38	PC_05	69	ADC1_VIN11	100	VDD_EXT
8	PA_07	39	PC_04	70	VDD_ANA1	101	VDD_EXT
9	VDD_EXT	40	PC_03	71	GND_ANA1	102	PB_10
10	PA_06	41	PC_02	72	BYP_A1	103	PB_08
11	PA_05	42	PC_01	73	VREF1	104	PB_09
12	PA_04	43	VDD_EXT	74	GND_VREF1	105	PB_06
13	PA_03	44	VDD_INT	75	REFCAP	106	PB_07
14	PA_02	45	PC_00	76	GND_VREF0	107	PB_05
15	PA_01	46	PB_14	77	VREF0	108	VDD_INT
16	VDD_INT	47	PB_15	78	BYP_A0	109	VDD_EXT
17	VDD_EXT	48	PB_13	79	GND_ANA0	110	PB_04
18	SYS_RESOUT	49	VDD_EXT	80	VDD_ANA0	111	PB_03
19	PA_00	50	PB_11	81	ADC0_VIN11	112	PB_02
20	SYS_FAULT	51	PB_12	82	ADC0_VIN10	113	PB_01
21	SYS_HWRST	52	GND	83	ADC0_VIN09	114	PB_00
22	VDD_EXT	53	VDD_EXT	84	ADC0_VIN08	115	PA_15
23	SYS_XTAL	54	VDD_INT	85	ADC0_VIN07	116	VDD_EXT
24	SYS_CLKIN	55	BYP_D0	86	ADC0_VIN06	117	PA_14
25	VREG_BASE	56	DAC1_VOUT	87	ADC0_VIN05	118	SYS_CLKOUT
26	VDD_VREG	57	ADC1_VIN00	88	ADC0_VIN04	119	SYS_BMODE1
27	VDD_EXT	58	ADC1_VIN01	89	ADC0_VIN03	120	SYS_BMODE0
28	TWI0_SCL	59	ADC1_VIN02	90	GND_ANA2	121	GND
29	TWI0_SDA	60	ADC1_VIN03	91	ADC0_VIN02		
30	JTG_TDI	61	GND_ANA3	92	ADC0_VIN01		
31	JTG_TCK/SWCLK	62	ADC1_VIN04	93	ADC0_VIN00		

* Pin no. 121 is the GND supply (see Figure 66) for the processor; this pad **must** connect to GND.