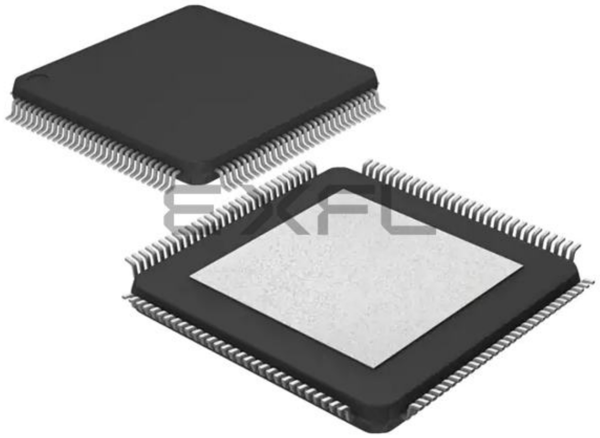

Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	CAN, I²C, SPI, SPORT, UART/USART
Clock Rate	150MHz
Non-Volatile Memory	FLASH (512kB)
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP Exposed Pad
Supplier Device Package	120-LQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-cm403cswz-ef

The GP counter can also support a programmable M/N frequency scaling of the CNT_CUD and CNT_CDG pins onto output pins in quadrature encoding mode.

Internal signals forwarded to each general-purpose timer enable these timers to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmable count values are exceeded.

Serial Peripheral Interface Ports (SPI)

The processor contains the SPI-compatible port that allows the processor to communicate with multiple SPI-compatible devices.

In its simplest mode, the SPI interface uses three pins for transferring data: two data pins master output-slave input and master input-slave output (SPI_MOSI and SPI_MISO) and a clock pin, SPI_CLK. A SPI chip select input pin ($\overline{\text{SPI\_SS}}$) lets other SPI devices select the processor, and three SPI chip select output pins (SPI_SELn) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI provides a full-duplex, synchronous serial interface, which supports both master and slave modes and multimaster environments.

In a multimaster or multislave SPI system, the MOSI and MISO data output pins can be configured to behave as open drain outputs (using the ODM bit) to prevent contention and possible damage to pin drivers. An external pull-up resistor is required on both the MOSI and MISO pins when this option is selected.

When ODM is set and the SPI is configured as a master, the MOSI pin is three-stated when the data driven out on MOSI is a logic high. The MOSI pin is not three-stated when the driven data is a logic low. Similarly, when ODM is set and the SPI is configured as a slave, the MISO pin is three-stated if the data driven out on MISO is a logic high.

The SPI port's baud rate and clock phase/polarities are programmable, and it has integrated DMA channels for both transmit and receive data streams.

Universal Asynchronous Receiver/Transmitter Ports (UART)

The processor provides full-duplex universal asynchronous receiver/transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, and none, even, or odd parity. Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multi-drop bus (MDB) systems. A frame is terminated by one, one and a half, two or two and a half stop bits.

The UART ports support automatic hardware flow control through the clear to send (CTS) input and request to send (RTS) output with programmable assertion FIFO levels.

To help support the local interconnect network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable inter-frame space.

The capabilities of the UARTs are further extended with support for the infrared data association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

2-Wire Controller Interface (TWI)

The processor includes a 2-wire interface (TWI) module for providing a simple exchange method of control data between multiple devices. The TWI module is compatible with the widely used I^2C bus standard. The TWI module offers the capabilities of simultaneous master and slave operation and support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (TWI_SCL) and data (TWI_SDA) and supports the protocol at speeds up to 400k bits/sec. The TWI interface pins are compatible with 5 V logic levels.

Additionally, the TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

Controller Area Network (CAN)

The CAN controller implements the CAN 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well suited for control applications due to its capability to communicate reliably over a network. This is because the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The CAN controller offers the following features:

- 32 mailboxes (8 receive only, 8 transmit only, 16 configurable for receive or transmit).
- Dedicated acceptance masks for each mailbox.
- Additional data filtering on first two bytes.
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats.
- Support for remote frames.
- Active or passive network support.
- Interrupts, including: TX complete, RX complete, error and global.

An additional crystal is not required to supply the CAN clock, as the CAN clock is derived from a system clock through a programmable divider.

10/100 Ethernet MAC (EMAC)

The processor can directly connect to a network by way of an embedded fast Ethernet media access controller (MAC) that supports both 10-BaseT (10M bits/sec) and 100-BaseT (100M bits/sec) operation. The 10/100 Ethernet MAC peripheral on the processor is fully compliant to the IEEE 802.3-2002 standard. It

Table 7. ADSP-CM402F/ADSP-CM403F 120-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PWM1_DL	PWM1 Channel D Low Side	B	PB_03
PWM1_SYNC	PWM1 Sync	A	PA_10
PWM1_TRIP0	PWM1 Trip Input 0	A	PA_11
PWM2_AH	PWM2 Channel A High Side	B	PB_06
PWM2_AL	PWM2 Channel A Low Side	B	PB_07
PWM2_BH	PWM2 Channel B High Side	B	PB_08
PWM2_BL	PWM2 Channel B Low Side	B	PB_09
PWM2_CH	PWM2 Channel C High Side	C	PC_03
PWM2_CL	PWM2 Channel C Low Side	C	PC_04
PWM2_DH	PWM2 Channel D High Side	C	PC_05
PWM2_DL	PWM2 Channel D Low Side	C	PC_06
PWM2_SYNC	PWM2 Sync	B	PB_04
PWM2_TRIP0	PWM2 Trip Input 0	B	PB_05
REFCAP	Output of BandGap Generator Filter Node (see recommended bypass filter - Figure 4 on Page 6)	Not Muxed	REFCAP
SINC0_CLK0	SINC0 Clock 0	B	PB_10
SINC0_CLK1	SINC0 Clock 1	C	PC_07
SINC0_D0	SINC0 Data 0	B	PB_11
SINC0_D1	SINC0 Data 1	B	PB_12
SINC0_D2	SINC0 Data 2	B	PB_13
SINC0_D3	SINC0 Data 3	B	PB_14
SMC0_A01	SMC0 Address 1	B	PB_13
SMC0_A02	SMC0 Address 2	B	PB_14
SMC0_A03	SMC0 Address 3	B	PB_15
SMC0_A04	SMC0 Address 4	C	PC_00
SMC0_A05	SMC0 Address 5	C	PC_01
SMC0_AMS0	SMC0 Memory Select 0	B	PB_11
SMC0_AMS2	SMC0 Memory Select 2	A	PA_07
SMC0_AOE	SMC0 Output Enable	B	PB_12
SMC0_ARDY	SMC0 Asynchronous Ready	B	PB_08
SMC0_ARE	SMC0 Read Enable	B	PB_09
SMC0_AWE	SMC0 Write Enable	B	PB_10
SMC0_D00	SMC0 Data 0	A	PA_08
SMC0_D01	SMC0 Data 1	A	PA_09
SMC0_D02	SMC0 Data 2	A	PA_10
SMC0_D03	SMC0 Data 3	A	PA_11
SMC0_D04	SMC0 Data 4	A	PA_12
SMC0_D05	SMC0 Data 5	A	PA_13
SMC0_D06	SMC0 Data 6	A	PA_14
SMC0_D07	SMC0 Data 7	A	PA_15
SMC0_D08	SMC0 Data 8	B	PB_00
SMC0_D09	SMC0 Data 9	B	PB_01
SMC0_D10	SMC0 Data 10	B	PB_02
SMC0_D11	SMC0 Data 11	B	PB_03
SMC0_D12	SMC0 Data 12	B	PB_04
SMC0_D13	SMC0 Data 13	B	PB_05

Table 16. Signal Multiplexing for Port E (176-Lead LQFP)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PE_00			SMC0_A14	SPT0_ACLK	
PE_01			SMC0_A15	SPT0_AFS	
PE_02			SMC0_A16	SPT0_AD0	
PE_03			SMC0_A17	SPT0_AD1	
PE_04			SMC0_A18		
PE_05			SMC0_A19		
PE_06		ETH0_PTPCLKIN	SMC0_A20		
PE_07		ETH0_PTPAUXIN	SMC0_A21		
PE_08		ETH0_PTPPPS	SMC0_A22		CNT2_ZM
PE_09		ETH0_CRS	SMC0_A23		CNT2_UD
PE_10		ETH0_MDIO	$\overline{\text{SMC0\_AMS1}}$		CNT2_DG
PE_11	ETH0_MDC		SMC0_A24		CNT3_ZM
PE_12	ETH0_TXD0				CNT3_UD
PE_13	ETH0_TXD1				CNT3_DG
PE_14	ETH0_TXEN	CNT1_OUTA			
PE_15	ETH0_REFCLK	CNT1_OUTB			

Table 17. Signal Multiplexing for Port F (176-Lead LQFP)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PF_00	ETH0_RXD0	CNT0_OUTA			
PF_01	ETH0_RXD1	CNT0_OUTB			
PF_02	USB0_VBC	TRACE_D03	$\overline{\text{SMC0\_ABE1}}$		
PF_03			$\overline{\text{SMC0\_AOE}}$		
PF_04			SMC0_ARDY		
PF_05			SMC0_A01		
PF_06			SMC0_A02		
PF_07			SMC0_A03		
PF_08			SMC0_A04		
PF_09			SMC0_A05		
PF_10			$\overline{\text{SMC0\_ABE0}}$		

Table 18. ADSP-CM409F 212-Ball BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_A03	SMC0 Address 3	F	PF_07
SMC0_A04	SMC0 Address 4	C	PC_00
SMC0_A04	SMC0 Address 4	F	PF_08
SMC0_A05	SMC0 Address 5	C	PC_01
SMC0_A05	SMC0 Address 5	F	PF_09
SMC0_A06	SMC0 Address 6	D	PD_08
SMC0_A07	SMC0 Address 7	D	PD_09
SMC0_A08	SMC0 Address 8	D	PD_10
SMC0_A09	SMC0 Address 9	D	PD_11
SMC0_A10	SMC0 Address 10	D	PD_12
SMC0_A11	SMC0 Address 11	D	PD_13
SMC0_A12	SMC0 Address 12	D	PD_14
SMC0_A13	SMC0 Address 13	D	PD_15
SMC0_A14	SMC0 Address 14	E	PE_00
SMC0_A15	SMC0 Address 15	E	PE_01
SMC0_A16	SMC0 Address 16	E	PE_02
SMC0_A17	SMC0 Address 17	E	PE_03
SMC0_A18	SMC0 Address 18	E	PE_04
SMC0_A19	SMC0 Address 19	E	PE_05
SMC0_A20	SMC0 Address 20	E	PE_06
SMC0_A21	SMC0 Address 21	E	PE_07
SMC0_A22	SMC0 Address 22	E	PE_08
SMC0_A23	SMC0 Address 23	E	PE_09
SMC0_A24	SMC0 Address 24	E	PE_11
SMC0_ABE0	SMC0 Byte Enable 0	F	PF_10
SMC0_ABE1	SMC0 Byte Enable 1	F	PF_02
SMC0_AMS0	SMC0 Memory Select 0	B	PB_11
SMC0_AMS0	SMC0 Memory Select 0	Not Muxed	SMC0_AMS0
SMC0_AMS1	SMC0 Memory Select 1	E	PE_10
SMC0_AMS2	SMC0 Memory Select 2	A	PA_07
SMC0_AMS3	SMC0 Memory Select 3	C	PC_11
SMC0_AOE	SMC0 Output Enable	B	PB_12
SMC0_AOE	SMC0 Output Enable	F	PF_03
SMC0_ARDY	SMC0 Asynchronous Ready	B	PB_08
SMC0_ARDY	SMC0 Asynchronous Ready	F	PF_04
SMC0_ARE	SMC0 Read Enable	B	PB_09
SMC0_ARE	SMC0 Read Enable	Not Muxed	SMC0_ARE
SMC0_AWE	SMC0 Write Enable	B	PB_10
SMC0_AWE	SMC0 Write Enable	Not Muxed	SMC0_AWE
SMC0_D00	SMC0 Data 0	A	PA_08
SMC0_D00	SMC0 Data 0	C	PC_08
SMC0_D01	SMC0 Data 1	A	PA_09
SMC0_D01	SMC0 Data 1	C	PC_09
SMC0_D02	SMC0 Data 2	A	PA_10
SMC0_D02	SMC0 Data 2	C	PC_10
SMC0_D03	SMC0 Data 3	A	PA_11

ADSP-CM409F GPIO MULTIPLEXING FOR 212-BALL BGA

Table 19 through Table 24 identify the pin functions that are multiplexed on the general-purpose I/O pins of the 212-ball BGA package.

Table 19. Signal Multiplexing for Port A (212-Ball BGA)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PA_00	PWM0_SYNC		SPT1_ACLK		
PA_01	PWM0_TRIP0		SPT1_AFS		
PA_02	PWM0_AH		SPT1_AD0		
PA_03	PWM0_AL		SPT1_AD1		
PA_04	PWM0_BH		SPT1_BCLK		
PA_05	PWM0_BL		SPT1_BFS		
PA_06	PWM0_CH		SPT1_BD0		
PA_07	PWM0_CL	SMC0_AMS2	SPT1_BD1		
PA_08	PWM1_CH		SMC0_D00		TM0_ACLK5
PA_09	PWM1_CL		SMC0_D01		TM0_ACLK4
PA_10	PWM1_SYNC		SMC0_D02		TM0_ACLK3
PA_11	PWM1_TRIP0	UART1_CTS	SMC0_D03		TM0_ACLK2
PA_12	PWM1_AH	TM0_TMR4	SMC0_D04		
PA_13	PWM1_AL	TM0_TMR5	SMC0_D05		
PA_14	PWM1_BH	TM0_TMR6	SMC0_D06		
PA_15	PWM1_BL	TM0_TMR3	SMC0_D07		

Table 20. Signal Multiplexing for Port B (212-Ball BGA)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PB_00	PWM0_DH	TRACE_CLK	SPT0_ACLK	SMC0_D08	CNT0_ZM
PB_01	PWM0_DL	TRACE_D00	SPT0_AFS	SMC0_D09	CNT0_UD
PB_02	PWM1_DH	TRACE_D01	SPT0_AD0	SMC0_D10	CNT0_DG
PB_03	PWM1_DL	TRACE_D02	SPT0_AD1	SMC0_D11	CNT1_ZM
PB_04	PWM2_SYNC	UART0_RTS	SPT0_ATDV	SMC0_D12	CNT1_UD
PB_05	PWM2_TRIP0	UART0_CTS	TM0_TMR7	SMC0_D13	CNT1_DG
PB_06	PWM2_AH	TM0_CLK	SPI1_SEL2	SMC0_D14	
PB_07	PWM2_AL	TM0_TMR0	SPI1_SEL3	SMC0_D15	CPTMR0_IN0
PB_08	PWM2_BH	TM0_TMR1	UART1_RX	SMC0_ARDY	TM0_ACI2/ CPTMR0_IN1
PB_09	PWM2_BL	TM0_TMR2	UART1_TX	SMC0_ARE	CPTMR0_IN2
PB_10	SINC0_CLK0	SPI0_D2	CAN1_RX	SMC0_AWE	TM0_ACI1
PB_11	SINC0_D0	SPI0_D3	CAN1_TX	SMC0_AMS0	TM0_ACLK1
PB_12	SINC0_D1	SPT0_BTDV	UART2_RX	SMC0_AOE	TM0_ACI3
PB_13	SINC0_D2	CNT0_OUTA	SPI0_SEL2	SMC0_A01	TM0_ACLK0/ SYS_DSWAKE3
PB_14	SINC0_D3	CNT0_OUTB	SPI0_SEL3	SMC0_A02	SPI0_SS/ SYS_DSWAKE2
PB_15	CAN0_RX	SPT1_ATDV	UART1_RX	SMC0_A03	TM0_ACI4

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PE_14	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 14 | ETH0 Transmit Enable | CNT1 Output Divider A Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PE_15	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 15 | ETH0 Reference Clock | CNT1 Output Divider B Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PF_00	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PF Position 0 | ETH0 Receive Data 0 | CNT0 Output Divider A Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PF_01	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PF Position 1 | ETH0 Receive Data 1 | CNT0 Output Divider B Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PF_02	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PF Position 2 | USB0 VBUS Control | Embedded Trace Module Data 3 | SMC0 Byte Enable 1 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PF_03	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PF Position 3 | SMC0 Output Enable Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PF_04	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PF Position 4 | SMC0 Asynchronous Ready Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PF_05	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PF Position 5 | SMC0 Address 1 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PF_06	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PF Position 6 | SMC0 Address 2 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PF_07	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PF Position 7 | SMC0 Address 3 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PF_08	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PF Position 8 | SMC0 Address 4 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PF_09	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PF Position 9 | SMC0 Address 5 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PF_10	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PF Position 10 | SMC0 Byte Enable 0 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
REFCAP	a	na	none	none	none	VDD_ANA	Desc: Output of BandGap Generator Filter Node (see recommended bypass filter - Figure 4 on Page 6) Notes: No notes.
SMC0_AMS0	I/O	A	pu	pu	none	VDD_EXT	Desc: SMC0 Memory Select 0 Notes: No notes.
SMC0_ARE	I/O	A	pu	pu	none	VDD_EXT	Desc: SMC0 Read Enable Notes: No notes.
SMC0_AWE	I/O	A	pu	pu	none	VDD_EXT	Desc: SMC0 Write Enable Notes: No notes.
SYS_BMODE0	I/O	na	none	none	none	VDD_EXT	Desc: Boot Mode Control 0 Notes: No notes.
SYS_BMODE1	I/O	na	none	none	none	VDD_EXT	Desc: Boot Mode Control 1 Notes: No notes.
SYS_CLKIN	I/O	na	none	none	none	VDD_EXT	Desc: Clock/Crystal Input Notes: No notes.
SYS_CLKOUT	I/O	na	pu	none	L	VDD_EXT	Desc: Processor Clock Output Notes: No notes.
SYS_FAULT	I/O	A	none	none	none	VDD_EXT	Desc: System Fault Output Notes: Open drain, requires an external pull-up resistor.
SYS_HWRST	I/O	na	none	none	none	VDD_EXT	Desc: Processor Hardware Reset Control Notes: No notes.
SYS_NMI	I/O	A	none	none	none	VDD_EXT	Desc: Non-maskable Interrupt Notes: Requires an external pull-up resistor.
SYS_RESOUT	I/O	A	pu	none	L	VDD_EXT	Desc: Reset Output Notes: No notes.
SYS_XTAL	a	na	none	none	none	VDD_EXT	Desc: Crystal Output Notes: Leave unconnected if an oscillator is used to provide SYS_CLKIN. Active during reset.
TWI0_SCL	I/O	B	none	none	none	VDD_EXT	Desc: TWI0 Serial Clock Notes: Open drain, requires external pullup resistor. Consult Version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
TWI0_SDA	I/O	B	none	none	none	VDD_EXT	Desc: TWI0 Serial Data Notes: en drain, requires external pullup resistor. Consult Version 2.1 of the I2C specification for the proper resistor value. If TWI is not used, connect to ground.
USB0_DM	I/O	D	none	none	none	VDD_EXT	Desc: USB0 Data – Notes: Pull low if not using USB.
USB0_DP	I/O	D	none	none	none	VDD_EXT	Desc: USB0 Data + Notes: Pull low if not using USB.

DAC Specifications

Typical values assume V_{DD_ANA} = 3.3 V, V_{REF} = 2.5 V.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG OUTPUT					DAC0_VOUT, DAC1_VOUT
Characteristic					
Output Voltage Range		0.1 to 2.5		V	
Output Impedance		0.6		Ω	Normal operation
		2		Ω	DAC @ full scale
		10		Ω	DAC @ zero scale
Update Rate			50	kHz	
Short Circuit Current to GND		30		mA	
Short Circuit Current to V_{DD}		30		mA	
STATIC PERFORMANCE					
DC ACCURACY					R_L = 500 Ω, C_L = 100 pF
Characteristic					
Resolution		12		Bits	
Differential Nonlinearity (DNL)		±0.99	−0.99/+1.2	LSB	Guaranteed monotonic
Integral Nonlinearity (INL)		±2.0	±3.5	LSB	
Offset Error		±1.0		mV	Measured at Code 0x000
Gain Error		±4.0		% FSR	% of full scale, measured at Code 0xFFF
DC Isolation			50	uV	Static output of DAC0_VOUT while DAC1_VOUT toggles 0 to full scale
DYNAMIC PERFORMANCE					
AC ACCURACY					R_L = 500 Ω, C_L = 100 pF
Characteristic					
Signal-to-Noise Ratio (SNR)		67	65	dB	
Signal-to-(Noise + Distortion) Ratio (SINAD)		62	59	dB	
Total Harmonic Distortion		63		dB	
Dynamic Range		68		dB	
Settling Time		1.5		µs	From ¼ to ¾ full scale
Slew Rate		1.5		V/µs	
D/A Glitch Energy		8		nV-s	Measured when code changes from 0x7FF to 0x800

ADC Typical Performance Characteristics

V_{DD_ANA} = 3.3 V, V_{REF} = 2.5 V, T_J = 25°C, unless otherwise noted.

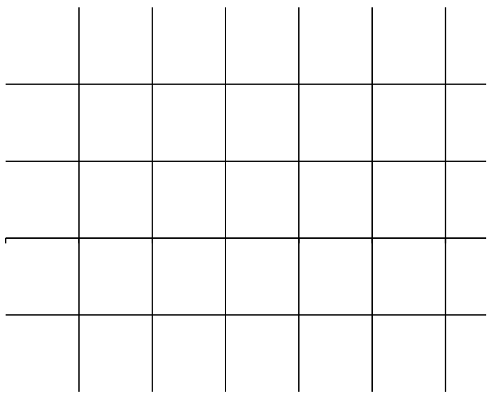

Figure 12. DNL vs. Code

Figure 13. Histogram of DC Input at Code Center (Internal Reference)

10/100 Ethernet MAC Controller (EMAC) Timing

Table 61 through Table 63 and Figure 52 through Figure 54 describe the 10/100 Ethernet MAC controller operations. Note the externally generated Ethernet MAC clock is called $f_{REFCLKEXT}$:

$$t_{REFCLKEXT} = \frac{1}{f_{REFCLKEXT}}$$

Table 61. 10/100 Ethernet MAC Controller (EMAC) Timing: RMII Receive Signal

Parameter[1]		Min	Max	Unit
Timing Requirements				
t_{REFCLK}	ETHx_REFCLK Period[2]	$t_{REFCLKEXT}$ – 1%		ns
$t_{REFCLKW}$	ETHx_REFCLK Width[2]	$t_{REFCLKEXT}$ × 35%	$t_{REFCLKEXT}$ × 65%	ns
$t_{REFCLKIS}$	Rx Input Valid to RMII ETHx_REFCLK Rising Edge (Data In Setup)	4		ns
$t_{REFCLKIH}$	RMII ETHx_REFCLK Rising Edge to Rx Input Invalid (Data In Hold)	2.0		ns

[1] RMII inputs synchronous to RMII REF_CLK are ERxDx, RMII CRS_DV, and ERxER.

[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external REF_CLK. For the external REF_CLK maximum frequency see the $t_{REFCLKEXT}$ specification in Table 27 Clock Related Operating Conditions.

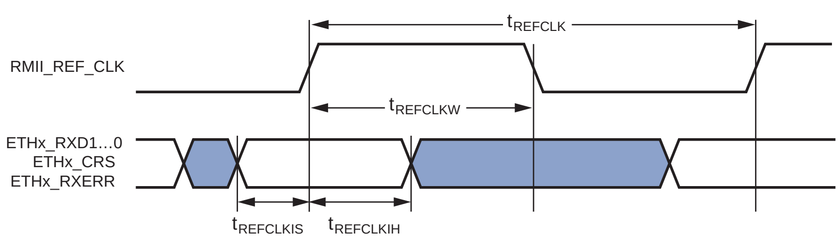

Figure 52. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal

Table 62. 10/100 Ethernet MAC Controller (EMAC) Timing: RMII Transmit Signal

Parameter[1]		Min	Max	Unit
Switching Characteristics				
$t_{REFCLKOV}$	RMII ETHx_REFCLK Rising Edge to Transmit Output Valid (Data Out Valid)		14	ns
$t_{REFCLKOH}$	RMII ETHx_REFCLK Rising Edge to Transmit Output Invalid (Data Out Hold)	2		ns

[1] RMII outputs synchronous to RMII REF_CLK are ETxDx.

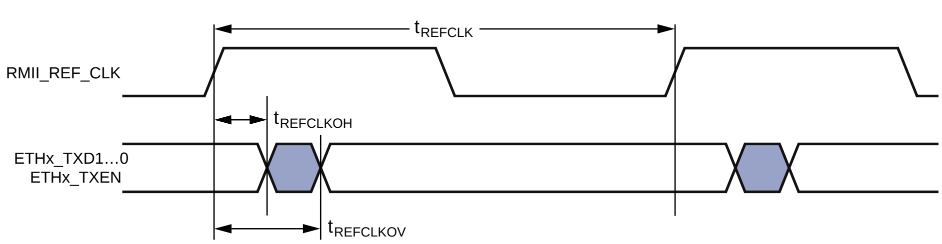

Figure 53. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

Sinus Cardinalis (SINC) Filter Timing

The programmed sinus cardinalis (SINC) filter clock ($f_{SINCLKPROG}$) frequency in MHz is set by the following equation where MDIV is a field in the CLK control register that can be set from 4 to 63:

$$f_{SINCLKPROG} = \frac{f_{SCLK}}{MDIV}$$

$$t_{SINCLKPROG} = \frac{1}{f_{SINCLKPROG}}$$

Table 64. SINC Filter Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSINC}	SINC0_Dx Setup Before SINC0_CLKx Rise	9		ns
t_{HSINC}	SINC0_Dx Hold After SINC0_CLKx Rise	0		ns
Switching Characteristics				
t_{SINCLK}	SINC0_CLKx Period[1]	$t_{SINCLKPROG} - 2.5$		ns
$t_{SINCLKW}$	SINC0_CLKx Width[1]	$0.5 \times t_{SINCLKPROG} - 2.5$		ns

[1] See Table 27 Clock Related Operating Conditions for details on the minimum period that may be programmed for $t_{SINCLKPROG}$.

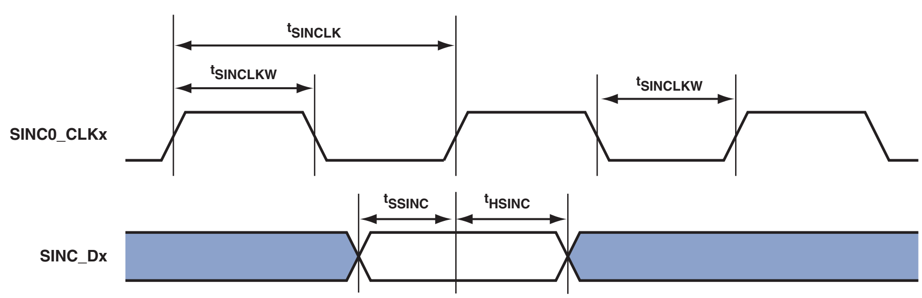

Figure 55. SINC Filter Timing

Values of T_{JA} are provided for package comparison and printed circuit board design considerations. T_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + T_{JA}\ uP_D$$

where:

T_A = Ambient temperature (°C).

Values of T_{JC} are provided for package comparison and printed circuit board design considerations when an external heat sink is required.

In Table 68 and Table 69, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Figure 65 shows the top view of the 120-lead LQFP package lead configuration and Figure 66 shows the bottom view of the 120-lead LQFP package lead configuration.

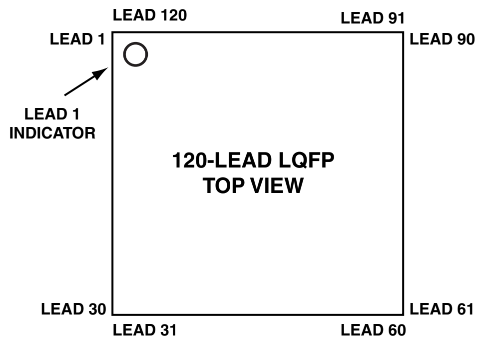

Figure 65. 120-Lead LQFP Lead Configuration (Top View)

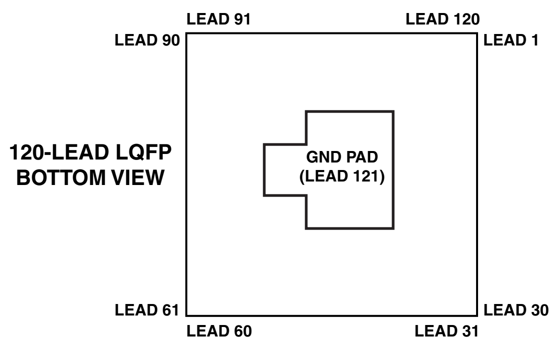

Figure 66. 120-Lead LQFP Lead Configuration (Bottom View)

Table 74. ADSP-CM407F/ADSP-CM408F 176-Lead LQFP Lead Assignments (Alphabetical by Pin Name) (Continued)

Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.
GND_ANA2	124	PC_04	54	PF_01	70	VDD_EXT	125
GND_ANA3	96	PC_05	51	PF_02	69	VDD_EXT	129
GND_VREF0	111	PC_06	52	PF_03	68	VDD_EXT	136
GND_VREF1	109	PC_07	49	PF_04	67	VDD_EXT	137
JTG_TCK/SWCLK	45	PC_08	39	PF_05	61	VDD_EXT	144
JTG_TDI	44	PC_09	40	PF_06	58	VDD_EXT	150
JTG_TDO/SWO	47	PC_10	38	PF_07	59	VDD_EXT	158
JTG_TMS/SWDIO	48	PC_11	10	PF_08	55	VDD_EXT	165
$\overline{\text{JTG\_TRST}}$	46	PC_12	11	PF_09	56	VDD_EXT	172
PA_00	25	PC_13	9	PF_10	53	VDD_INT	22
PA_01	21	PC_14	7	REFCAP	110	VDD_INT	65
PA_02	20	PC_15	5	$\overline{\text{SMC0\_AMS0}}$	147	VDD_INT	94
PA_03	19	PD_00	169	$\overline{\text{SMC0\_ARE}}$	149	VDD_INT	128
PA_04	18	PD_01	166	$\overline{\text{SMC0\_AWE}}$	148	VDD_INT	157
PA_05	17	PD_02	167	SYS_BMODE0	176	VDD_VREG	32
PA_06	16	PD_03	163	SYS_BMODE1	175	VREF0	112
PA_07	14	PD_04	164	SYS_CLKIN	30	VREF1	108
PA_08	13	PD_05	161	SYS_CLKOUT	174	VREG_BASE	31
PA_09	12	PD_06	146	$\overline{\text{SYS\_FAULT}}$	26		
PA_10	6	PD_07	145	$\overline{\text{SYS\_HWRST}}$	27		
PA_11	4	PD_08	142	$\overline{\text{SYS\_NMI}}$	132		

* Pin no. 177 is the GND supply (see Figure 68) for the processor; this pad **must** connect to GND.

OUTLINE DIMENSIONS

Dimensions in Figure 70 (for the 120-lead LQFP), Figure 71 (for the 176-lead LQFP) and Figure 72 (for the 212-ball BGA) are shown in millimeters.

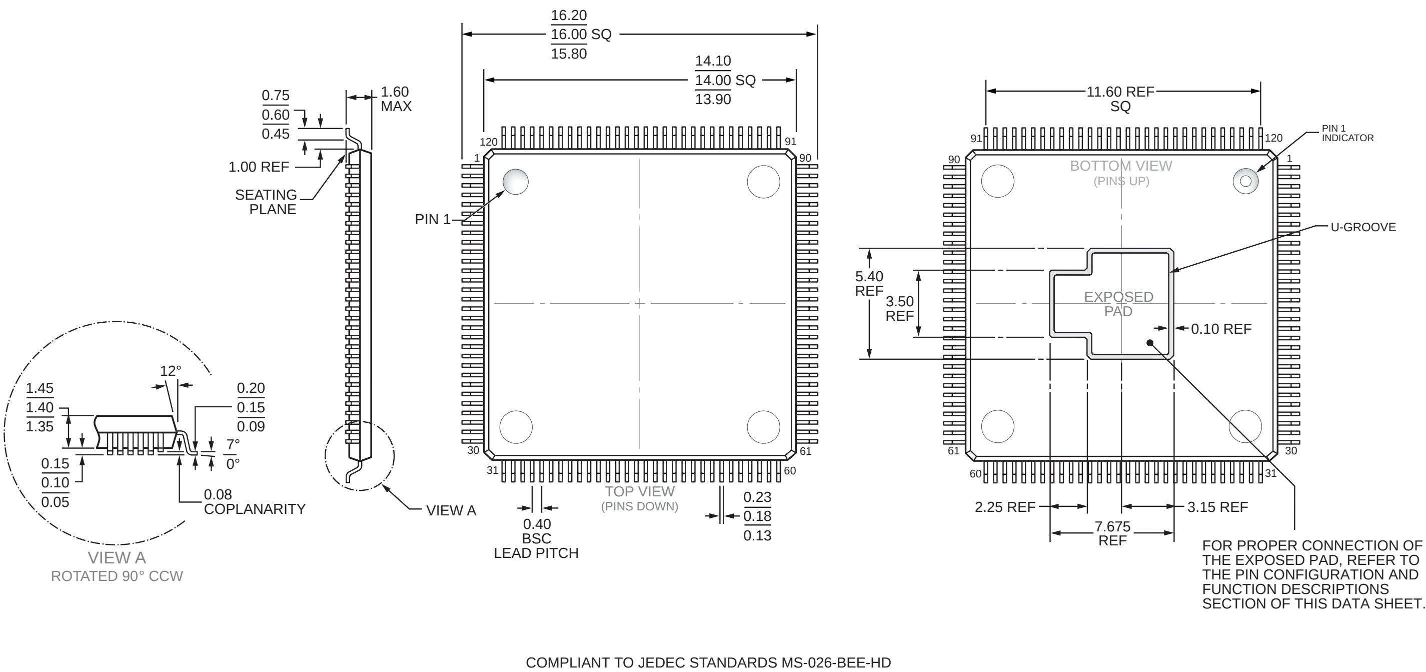

Figure 70. 120-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP][1]
(SW-120-3)
Dimensions shown in millimeters

[1] For information relating to the SW-120-3 package's exposed pad, see the table endnote in ADSP-CM402F/ADSP-CM403F 120-Lead LQFP Lead Assignments on Page 110.