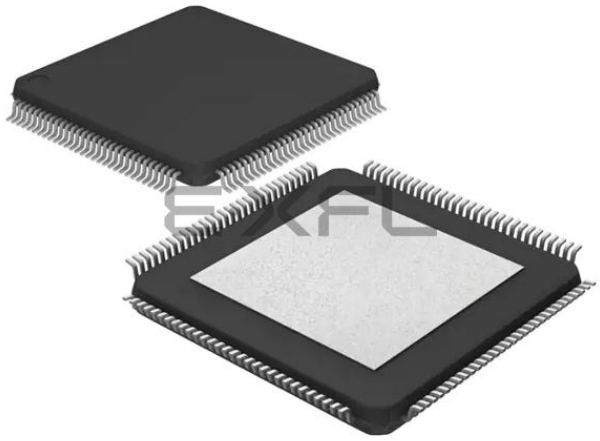

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	CAN, I²C, SPI, SPORT, UART/USART
Clock Rate	100MHz
Non-Volatile Memory	FLASH (256kB)
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP Exposed Pad
Supplier Device Package	120-LQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-cm403cswz-ff

registers with associated hardware. These four SWU match groups operate independently, but share common event (interrupt and trigger) outputs.

DEVELOPMENT TOOLS

The ADSP-CM40xF processor is supported with a set of highly sophisticated and easy-to-use development tools for embedded applications. For more information, see the Analog Devices website.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-CM40xF processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *ADSP-CM40x Mixed-Signal Control Processor with ARM Cortex-M4 Hardware Reference*
- *ADSP-CM402F/CM403F/CM407F/CM408F/CM409F Anomaly Sheet*

This data sheet describes the ARM Cortex-M4 core and memory architecture used on the ADSP-CM40xF processor, but does not provide detailed programming information for the ARM processor. For more information about programming the ARM processor, visit the ARM Infocenter web page.

The applicable documentation for programming the ARM Cortex-M4 processor include:

- *Cortex®-M4 Devices Generic User Guide*
- *CoreSight™ ETM™-M4 Technical Reference Manual*
- *Cortex®-M4 Technical Reference Manual*

RELATED SIGNAL CHAINS

A signal chain is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (http:\\www.analog.com\circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

SECURITY FEATURES DISCLAIMER

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ADSP-CM40xF DETAILED SIGNAL DESCRIPTIONS

Table 6 provides a detailed description of each pin.

Table 6. ADSP-CM40xF Detailed Signal Description

Signal Name	Direction	Description
ADC_VINnn	Input	**Channel nn.** Single-Ended Analog Input for ADCs. nn = 00 to 11 for each ADC
BYP_An		**On-chip Analog Power Regulation Bypass Filter Node for ADC.** Connect to decoupling capacitors. n = 0, 1
BYP_D0		**On-chip Digital Power Regulation Bypass Filter Node for Analog Subsystem.** Connect to decoupling capacitors.
CAN_RX	Input	**CAN Receive.** Typically an external CAN transceiver's RX output.
CAN_TX	Output	**CAN Transmit.** Typically an external CAN transceiver's TX input.
CNT_OUTA	Output	**Counter Output Divider A.** Frequency scaled output in Quadrature encoder mode of GP Counter
CNT_OUTB	Output	**Counter Output Divider B.** Frequency scaled output in Quadrature encoder mode of GP Counter
CNT_DG	Input	**CNT Count Down and Gate.** Depending on the mode of operation this input acts either as a count down signal or a gate signal. Count Down: This input causes the GP counter to decrement. Gate: Stops the GP counter from incrementing or decrementing.
CNT_UD	Input	**Count Up and Direction.** Depending on the mode of operation this input acts either as a count up signal or a direction signal. Count Up: This input causes the GP counter to increment. Direction: Selects whether the GP counter is incrementing or decrementing.
CNT_ZM	Input	**Count Zero Marker.** Input that connects to the zero marker output of a rotary device or detects the pressing of a push button.
CPTMR_INn	Input	**Capture Timer Input Pins.** n = 0, 1, 2
DACn_VOUT	Output	**DAC Output.** Analog voltage output. n = 0, 1
ETH_CRS	Input	**EMAC Carrier Sense.** Multiplexed on alternate clock cycles. CRS: Asserted by the PHY when either the transmit or receive medium is not idle. De-asserted when both are idle. RXDV: Asserted by the PHY when the data on RXDn is valid.
ETH_MDC	Output	**EMAC Management Channel Clock.** Clocks the MDC input of the PHY.
ETH_MDIO	I/O	**EMAC Management Channel Serial Data.** Bidirectional data bus for PHY control.
ETH_PTPAUXIN	Input	**EMAC PTP Auxiliary Trigger Input.** Assert this signal to take an auxiliary snapshot of the time and store it in the auxiliary time stamp FIFO.
ETH_PTPCLKIN	Input	**EMAC PTP Clock Input.** Optional external PTP clock input.
ETH_PTPPPS	Output	**EMAC PTP Pulse-Per-Second Output.** When the Advanced Time Stamp feature is enabled, this signal is asserted based on the PPS mode selected. Otherwise, PTPPPS is asserted every time the seconds counter is incremented.
ETH_REFCLK	Input	**EMAC Reference Clock.** Externally supplied Ethernet clock.
ETH_RXDn	Input	**EMAC Receive Data n.** Receive data bus. n = 0, 1
ETH_TXDn	Output	**EMAC Transmit Data n.** Transmit data bus. n = 0, 1
ETH_TXEN	I/O	**EMAC Transmit Enable.** When asserted indicates that the data on TXDn is valid.
JTG_SWCLK	I/O	**Serial Wire Clock.** Clocks data into and out of the target during debug.
JTG_SWDIO	I/O	**Serial Wire Data IO.** Sends and receives serial data to and from the target during debug.
JTG_SWO	Output	**Serial Wire Out.** Provides trace data to the emulator.
JTG_TCK	Input	**JTAG Clock.** JTAG test access port clock.
JTG_TDI	Input	**JTAG Serial Data In.** JTAG test access port data input.
JTG_TDO	Output	**JTAG Serial Data Out.** JTAG test access port data output.
JTG_TMS	Input	**JTAG Mode Select.** JTAG test access port mode select.

Table 6. ADSP-CM40xF Detailed Signal Description (Continued)

Signal Name	Direction	Description
USB_ID	Input	**USB OTG ID.** Senses whether the controller is a host or device. This signal is pulled low when an A-type plug is sensed (signifying that the USB controller is the A device), but the input is high when a B-type plug is sensed (signifying that the USB controller is the B device).
USB_VBC	Output	**USB VBUS Control.** Controls an external voltage source to supply VBUS when in host mode. May be configured as open drain. Polarity is configurable as well.
USB_VBUS	I/O	**USB Bus Voltage.** Connects to bus voltage in host and device modes.
VREFn	I/O	**Voltage Reference for ADC.** When internal reference is selected for ADC, the VREF pin is used for connecting bypass caps. When external reference is selected, an external reference device should be connected to these pins to supply the external reference voltage. n=0,1.
VREG_BASE	Output	**Voltage Regulator Base Node.** Connected to Base of PNP transistor when using internal VDD_INT reference.

ADSP-CM402F/ADSP-CM403F 120-LEAD LQFP SIGNAL DESCRIPTIONS

The processor's pin definitions are shown in Table 7. The columns in this table provide the following information:

- Signal Name: The Signal Name column in the table includes the signal name for every pin and (where applicable) the GPIO multiplexed pin function for every pin.
- Description: The Description column in the table provides a verbose (descriptive) name for the signal.
- General-Purpose Port: The Port column in the table shows whether or not the signal is multiplexed with other signals on a general-purpose I/O port pin.
- Pin Name: The Pin Name column in the table identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).

Table 7. ADSP-CM402F/ADSP-CM403F 120-Lead LQFP Signal Descriptions

Signal Name	Description	Port	Pin Name
ADC0_VIN00	Channel 0 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN00
ADC0_VIN01	Channel 1 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN01
ADC0_VIN02	Channel 2 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN02
ADC0_VIN03	Channel 3 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN03
ADC0_VIN04	Channel 4 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN04
ADC0_VIN05	Channel 5 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN05
ADC0_VIN06	Channel 6 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN06
ADC0_VIN07	Channel 7 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN07
ADC0_VIN08	Channel 8 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN08
ADC0_VIN09	Channel 9 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN09
ADC0_VIN10	Channel 10 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN10
ADC0_VIN11	Channel 11 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN11
ADC1_VIN00	Channel 0 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN00
ADC1_VIN01	Channel 1 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN01
ADC1_VIN02	Channel 2 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN02
ADC1_VIN03	Channel 3 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN03
ADC1_VIN04	Channel 4 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN04
ADC1_VIN05	Channel 5 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN05
ADC1_VIN06	Channel 6 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN06
ADC1_VIN07	Channel 7 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN07
ADC1_VIN08	Channel 8 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN08
ADC1_VIN09	Channel 9 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN09
ADC1_VIN10	Channel 10 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN10
ADC1_VIN11	Channel 11 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN11
BYP_A0	On-chip Analog Power Regulation Bypass Filter Node for ADC0 (see recommended bypass - Figure 4 on Page 6)	Not Muxed	BYP_A0
BYP_A1	On-chip Analog Power Regulation Bypass Filter Node for ADC1 (see recommended bypass - Figure 4 on Page 6)	Not Muxed	BYP_A1
BYP_D0	On-chip Digital Power Regulation Bypass Filter Node for Analog Subsystem (see recommended bypass - Figure 4 on Page 6)	Not Muxed	BYP_D0
CAN0_RX	CAN0 Receive	B	PB_15
CAN0_TX	CAN0 Transmit	C	PC_00
CAN1_RX	CAN1 Receive	B	PB_10
CAN1_TX	CAN1 Transmit	B	PB_11
CNT0_DG	CNT0 Count Down and Gate	B	PB_02
CNT0_OUTA	CNT0 Output Divider A	B	PB_13

Table 7. ADSP-CM402F/ADSP-CM403F 120-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
TM0_ACLK1	TIMER0 Alternate Clock 1	B	PB_11
TM0_ACLK2	TIMER0 Alternate Clock 2	A	PA_11
TM0_ACLK3	TIMER0 Alternate Clock 3	A	PA_10
TM0_ACLK4	TIMER0 Alternate Clock 4	A	PA_09
TM0_ACLK5	TIMER0 Alternate Clock 5	A	PA_08
TM0_CLK	TIMER0 Clock	B	PB_06
TM0_TMR0	TIMER0 Timer 0	B	PB_07
TM0_TMR1	TIMER0 Timer 1	B	PB_08
TM0_TMR2	TIMER0 Timer 2	B	PB_09
TM0_TMR3	TIMER0 Timer 3	A	PA_15
TM0_TMR4	TIMER0 Timer 4	A	PA_12
TM0_TMR5	TIMER0 Timer 5	A	PA_13
TM0_TMR6	TIMER0 Timer 6	A	PA_14
TM0_TMR7	TIMER0 Timer 7	B	PB_05
TRACE_CLK	Embedded Trace Module Clock	B	PB_00
TRACE_D00	Embedded Trace Module Data 0	B	PB_01
TRACE_D01	Embedded Trace Module Data 1	B	PB_02
TRACE_D02	Embedded Trace Module Data 2	B	PB_03
TRACE_D03	Embedded Trace Module Data 3	C	PC_02
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	B	PB_05
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	B	PB_04
$\overline{\text{UART0\_RX}}$	UART0 Receive	C	PC_01
$\overline{\text{UART0\_TX}}$	UART0 Transmit	C	PC_02
$\overline{\text{UART1\_CTS}}$	UART1 Clear to Send	A	PA_11
$\overline{\text{UART1\_RTS}}$	UART1 Request to Send	C	PC_07
$\overline{\text{UART1\_RX}}$	UART1 Receive	B	PB_08
$\overline{\text{UART1\_RX}}$	UART1 Receive	B	PB_15
$\overline{\text{UART1\_TX}}$	UART1 Transmit	B	PB_09
$\overline{\text{UART1\_TX}}$	UART1 Transmit	C	PC_00
$\overline{\text{UART2\_RX}}$	UART2 Receive	B	PB_12
$\overline{\text{UART2\_TX}}$	UART2 Transmit	C	PC_07
VDD_ANA0	Analog Voltage Domain (see recommended bypass - Figure 4 on Page 6)	Not Muxed	VDD_ANA0
VDD_ANA1	Analog Voltage Domain (see recommended bypass - Figure 4 on Page 6)	Not Muxed	VDD_ANA1
VDD_EXT	External Voltage Domain	Not Muxed	VDD_EXT
VDD_INT	Internal Voltage Domain	Not Muxed	VDD_INT
VDD_VREG	VREG Supply Voltage	Not Muxed	VDD_VREG
VREF0	Voltage Reference for ADC0. Default configuration is Output (see recommended bypass - Figure 4 on Page 6)	Not Muxed	VREF0
VREF1	Voltage Reference for ADC1. Default configuration is Output (see recommended bypass - Figure 4 on Page 6)	Not Muxed	VREF1
VREG_BASE	Voltage Regulator Base Node	Not Muxed	VREG_BASE

ADSP-CM409F 212-BALL BGA SIGNAL DESCRIPTIONS

The processor's pin definitions are shown in Table 18. The columns in this table provide the following information:

- Signal Name: The Signal Name column in the table includes the signal name for every pin and (where applicable) the GPIO multiplexed pin function for every pin.
- Description: The Description column in the table provides a verbose (descriptive) name for the signal.
- General-Purpose Port: The Port column in the table shows whether or not the signal is multiplexed with other signals on a general-purpose I/O port pin.
- Pin Name: The Pin Name column in the table identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).

Table 18. ADSP-CM409F 212-Ball BGA Signal Descriptions

Signal Name	Description	Port	Pin Name
ADC0_VIN00	Channel 0 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN00
ADC0_VIN01	Channel 1 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN01
ADC0_VIN02	Channel 2 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN02
ADC0_VIN03	Channel 3 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN03
ADC0_VIN04	Channel 4 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN04
ADC0_VIN05	Channel 5 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN05
ADC0_VIN06	Channel 6 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN06
ADC0_VIN07	Channel 7 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN07
ADC0_VIN08	Channel 8 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN08
ADC0_VIN09	Channel 9 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN09
ADC0_VIN10	Channel 10 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN10
ADC0_VIN11	Channel 11 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN11
ADC1_VIN00	Channel 0 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN00
ADC1_VIN01	Channel 1 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN01
ADC1_VIN02	Channel 2 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN02
ADC1_VIN03	Channel 3 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN03
ADC1_VIN04	Channel 4 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN04
ADC1_VIN05	Channel 5 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN05
ADC1_VIN06	Channel 6 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN06
ADC1_VIN07	Channel 7 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN07
ADC1_VIN08	Channel 8 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN08
ADC1_VIN09	Channel 9 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN09
ADC1_VIN10	Channel 10 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN10
ADC1_VIN11	Channel 11 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN11
BYP_A0	On-chip Analog Power Regulation Bypass Filter Node for ADC0 (see recommended bypass -Figure 4 on Page 6)	Not Muxed	BYP_A0
BYP_A1	On-chip Analog Power Regulation Bypass Filter Node for ADC1 (see recommended bypass - Figure 4 on Page 6)	Not Muxed	BYP_A1
BYP_D0	On-chip Digital Power Regulation Bypass Filter Node for Analog Subsystem (see recommended bypass - Figure 4 on Page 6)	Not Muxed	BYP_D0
CAN0_RX	CAN0 Receive	B	PB_15
CAN0_TX	CAN0 Transmit	C	PC_00
CAN1_RX	CAN1 Receive	B	PB_10
CAN1_TX	CAN1 Transmit	B	PB_11
CNT0_DG	CNT0 Count Down and Gate	B	PB_02
CNT0_OUTA	CNT0 Output Divider A	B	PB_13

Table 18. ADSP-CM409F 212-Ball BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PD_00-PD_15	Port D Positions 0 – 15	D	PD_00 – PD_15
PE_00-PE_15	Port E Positions 0 – 15	E	PE_00 – PE_15
PF_00-PF_10	Port F Positions 0 – 15	F	PF_00 – PF_10
PWM0_AH	PWM0 Channel A High Side	A	PA_02
PWM0_AL	PWM0 Channel A Low Side	A	PA_03
PWM0_BH	PWM0 Channel B High Side	A	PA_04
PWM0_BL	PWM0 Channel B Low Side	A	PA_05
PWM0_CH	PWM0 Channel C High Side	A	PA_06
PWM0_CL	PWM0 Channel C Low Side	A	PA_07
PWM0_DH	PWM0 Channel D High Side	B	PB_00
PWM0_DL	PWM0 Channel D Low Side	B	PB_01
PWM0_SYNC	PWM0 Sync	A	PA_00
$\overline{\text{PWM0\_TRIP0}}$	PWM0 Trip Input 0	A	PA_01
PWM1_AH	PWM1 Channel A High Side	A	PA_12
PWM1_AL	PWM1 Channel A Low Side	A	PA_13
PWM1_BH	PWM1 Channel B High Side	A	PA_14
PWM1_BL	PWM1 Channel B Low Side	A	PA_15
PWM1_CH	PWM1 Channel C High Side	A	PA_08
PWM1_CL	PWM1 Channel C Low Side	A	PA_09
PWM1_DH	PWM1 Channel D High Side	B	PB_02
PWM1_DL	PWM1 Channel D Low Side	B	PB_03
PWM1_SYNC	PWM1 Sync	A	PA_10
$\overline{\text{PWM1\_TRIP0}}$	PWM1 Trip Input 0	A	PA_11
PWM2_AH	PWM2 Channel A High Side	B	PB_06
PWM2_AL	PWM2 Channel A Low Side	B	PB_07
PWM2_BH	PWM2 Channel B High Side	B	PB_08
PWM2_BL	PWM2 Channel B Low Side	B	PB_09
PWM2_CH	PWM2 Channel C High Side	C	PC_03
PWM2_CL	PWM2 Channel C Low Side	C	PC_04
PWM2_DH	PWM2 Channel D High Side	C	PC_05
PWM2_DL	PWM2 Channel D Low Side	C	PC_06
PWM2_SYNC	PWM2 Sync	B	PB_04
$\overline{\text{PWM2\_TRIP0}}$	PWM2 Trip Input 0	B	PB_05
REFCAP	Output of BandGap Generator Filter Node (see recommended bypass filter - Figure 4 on Page 6)	Not Muxed	REFCAP
SINC0_CLK0	SINC0 Clock 0	B	PB_10
SINC0_CLK1	SINC0 Clock 1	C	PC_07
SINC0_D0	SINC0 Data 0	B	PB_11
SINC0_D1	SINC0 Data 1	B	PB_12
SINC0_D2	SINC0 Data 2	B	PB_13
SINC0_D3	SINC0 Data 3	B	PB_14
SMC0_A01	SMC0 Address 1	B	PB_13
SMC0_A01	SMC0 Address 1	F	PF_05
SMC0_A02	SMC0 Address 2	B	PB_14
SMC0_A02	SMC0 Address 2	F	PF_06
SMC0_A03	SMC0 Address 3	B	PB_15

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PA_15	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 15 | PWM1 Channel B Low Side | TM0 Timer 3 | SMC0 Data 7 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_00	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 0 | PWM0 Channel D High Side | Embedded Trace Module Clock | SPORT0 Channel A Clock | SMC0 Data 8 | CNT0 Count Zero Marker Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_01	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 1 | PWM0 Channel D Low Side | Embedded Trace Module Data 0 | SPORT0 Channel A Frame Sync | SMC0 Data 9 | CNT0 Count Up and Direction Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_02	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 2 | PWM1 Channel D High Side | Embedded Trace Module Data 1 | SPORT0 Channel A Data 0 | SMC0 Data 10 | CNT0 Count Down and Gate Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_03	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 3 | PWM1 Channel D Low Side | Embedded Trace Module Data 2 | SPORT0 Channel A Data 1 | SMC0 Data 11 | CNT1 Count Zero Marker Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_04	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 4 | PWM2 Sync | UART0 Request to Send | SPORT0 Channel A Transmit Data Valid | SMC0 Data 12 | CNT1 Count Up and Direction Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_05	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 5 | PWM2 Trip Input 0 | UART0 Clear to Send | TM0 Timer 7 | SMC0 Data 13 | CNT1 Count Down and Gate Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_06	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 6 | PWM2 Channel A High Side | TM0 Common Clock | SPI1 Slave Select Output 2 | SMC0 Data 14 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_07	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 7 | PWM2 Channel A Low Side | TM0 Timer 0 | SPI1 Slave Select Output 3 | SMC0 Data 15 | Capture Timer0 Input 0 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PB_08	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 8 | PWM2 Channel B High Side | TM0 Timer 1 | UART1 Receive | SMC0 Asynchronous Ready | TM0 Timer2 Alternate Capture Input | Capture Timer0 Input 1 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_09	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 9 | PWM2 Channel B Low Side | TM0 Timer 2 | UART1 Transmit | SMC0 Read Enable | Capture Timer0 Input 2 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_10	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 10 | SINC0 Clock 0 | SPI0 Data 2 | CAN1 Receive | SMC0 Write Enable | TM0 Timer1 Alternate Capture Input Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_11	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 11 | SINC0 Data 0 | SPI0 Data 3 | CAN1 Transmit | SMC0 Memory Select 0 | TM0 Timer1 Alternate Clock Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_12	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 12 | SINC0 Data 1 | SPORT0 Channel B Transmit Data Valid | UART2 Receive | SMC0 Output Enable | TM0 Timer3 Alternate Capture Input Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_13	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 13 | SINC0 Data 2 | CNT0 Output Divider A | SPI0 Slave Select Output 2 | SMC0 Address 1 | SYS0 Deep Sleep Wakeup 3 | TM0 Timer0 Alternate Clock Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_14	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 14 | SINC0 Data 3 | CNT0 Output Divider B | SPI0 Slave Select Output 3 | SMC0 Address 2 | SYS0 Deep Sleep Wakeup 2 | SPI0 Slave Select Input Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_15	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 15 | CAN0 Receive | SPORT1 Channel A Transmit Data Valid | UART1 Receive | SMC0 Address 3 | TM0 Timer4 Alternate Capture Input Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PC_00	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PC Position 0 | CAN0 Transmit | SPORT1 Channel B Transmit Data Valid | UART1 Transmit | SMC0 Address 4 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.

SPECIFICATIONS

For information about product specifications, contact your Analog Devices representative.

OPERATING CONDITIONS

Parameter		Test Conditions/Comments	Min	Nominal	Max	Unit
V_{DD_INT}	Digital Internal Supply Voltage	$f_{CCLK} \le 240$ MHz	1.14	1.2	1.26	V
V_{DD_EXT}[1]	Digital External Supply Voltage		3.13	3.3	3.47	V
V_{DD_ANA}[1]	Analog Supply Voltage		3.13	3.3	3.47	V
V_{IH}[2]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	2.0			V
V_{IH_CLKIN}[3]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	2.2			V
V_{IHTWI}[4, 5]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	0.7 × $V_{VBUSTWI}$		$V_{VBUSTWI}$	V
V_{IL}[2]	Low Level Input Voltage	V_{DD_EXT} = 3.13 V			0.8	V
V_{ILTWI}[4, 5]	Low Level Input Voltage	V_{DD_EXT} = 3.13 V			0.3 × $V_{VBUSTWI}$	V
T_J	Junction Temperature	$T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C

[1] Must remain powered (even if the associated function is not used).
[2] Parameter value applies to all input and bidirectional signals except TWI signals and USB0 signals.
[3] Parameter applies to SYS_CLKIN signal.
[4] Parameter applies to TWI_SDA and TWI_SCL.
[5] TWI signals are pulled up to V_{BUSTWI}. See Table 26.

Table 26. TWI_VSEL Selections and V_{DD_EXT}/V_{BUSTWI}

TWI_DT Setting	V_{DD_EXT} Nominal	V_{BUSTWI} Min	V_{BUSTWI} Nom	V_{BUSTWI} Max	Unit
TWI000[1]	3.30	3.13	3.30	3.47	V
TWI100	3.30	4.75	5.00	5.25	V

[1] Designs must comply with the V_{DD_EXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

Clock Related Operating Conditions

Table 27 describes the core clock, system clock, and peripheral clock timing requirements. The data presented in the tables applies to all speed grades found in the Ordering Guide on Page 124 except where expressly noted. Figure 10 provides a graphical representation of the various clocks and their available multiplier or divider values.

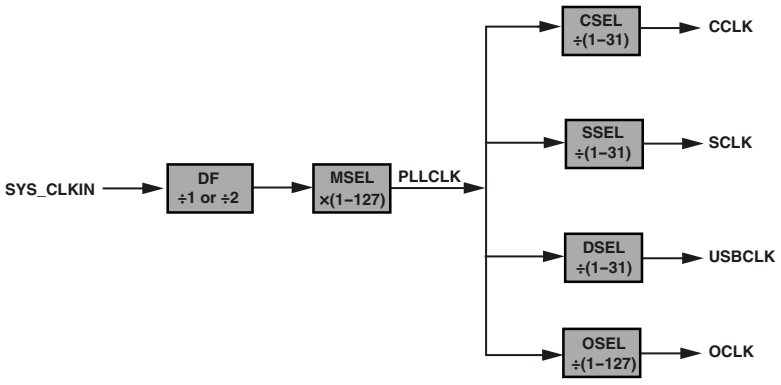

Figure 10. Clock Relationships and Divider Values

Asynchronous Write

Table 39 and Figure 29 show asynchronous memory write timing, related to the static memory controller (SMC).

Table 39. Asynchronous Memory Write (BxMODE = b#00)

Parameter		Min	Max	Unit
Timing Requirement				
$t_{DARDYAWE}$[1]	SMC0_ARDY Valid After $\overline{SMC0\_AWE}$ Low[2]		(WAT – 2.5) × t_{SCLK} – 17.5	ns
Switching Characteristics				
t_{ENDAT}	DATA Enable After $\overline{SMC0\_AMSx}$ Assertion	–3		ns
t_{DDAT}	DATA Disable After $\overline{SMC0\_AMSx}$ Deassertion		3	ns
t_{AMSAWE}	SMC0_Ax/$\overline{SMC0\_AMSx}$ Assertion Before $\overline{SMC0\_AWE}$ Low[3]	(PREST + WST + PREAT) × t_{SCLK} – 6.4		ns
t_{HAWE}	Output[4] Hold After $\overline{SMC0\_AWE}$ High[5]	WHT × t_{SCLK} – 2		ns
t_{WAWE}[6]	$\overline{SMC0\_AWE}$ Active Low Width[2]	WAT × t_{SCLK} – 2		ns
$t_{DAWEARDY}$[1]	$\overline{SMC0\_AWE}$ High Delay After SMC0_ARDY Assertion	2.5 × t_{SCLK}	3.5 × t_{SCLK} + 17.5	ns

[1] SMC_BxCTL.ARDYEN bit = 1.
[2] WAT value set using the SMC_BxTIM.WAT bits.
[3] PREST, WST, PREAT values set using the SMC_BxETIM.PREST bits, SMC_BxTIM.WST bits, SMC_BxETIM.PREAT bits, and the SMC_BxTIM.RAT bits.
[4] Output signals are DATA, SMC0_Ax, $\overline{SMC0\_AMSx}$, $\overline{SMC0\_ABEx}$.
[5] WHT value set using the SMC_BxTIM.WHT bits.
[6] SMC_BxCTL.ARDYEN bit = 0.

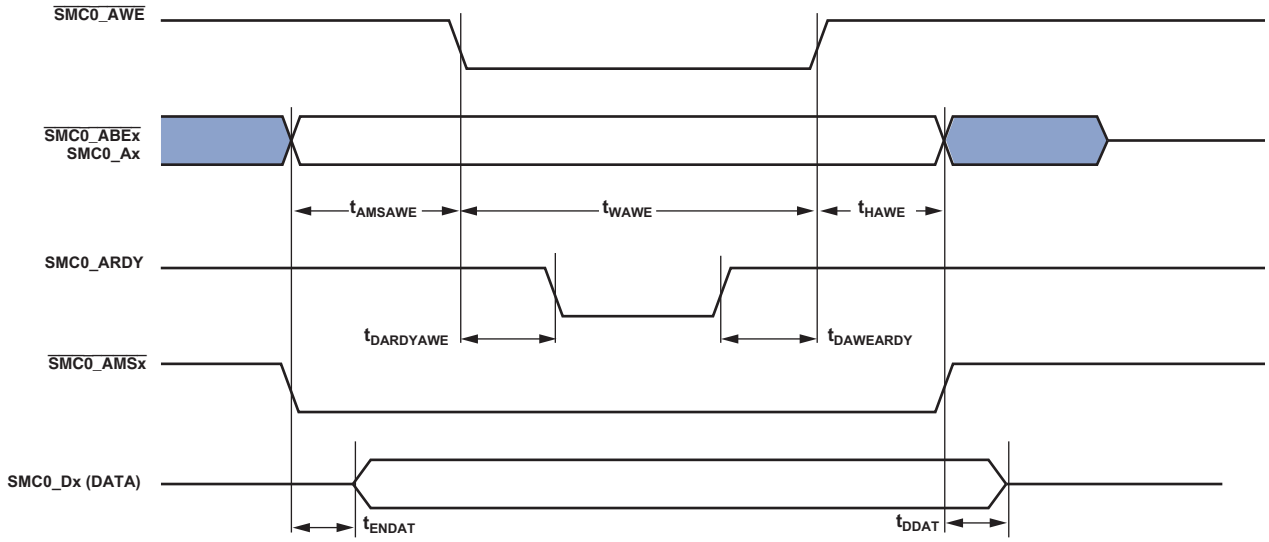

Figure 29. Asynchronous Write

Serial Peripheral Interface (SPI) Port—Memory Map Mode Timing

Table 53. SPI Port—Memory Map Mode Timing

Parameter		Min	Max	Unit
Switching Characteristic				
$t_{ZDSPIDM}$	SPI_CLK Edge to Data-Out High Impedance	–1	+8	ns

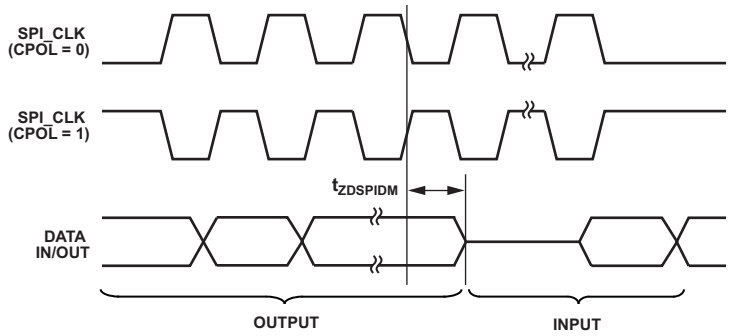

Figure 44. SPI_CLK Valid Edge to Data-Out High Impedance in Master Mode with CPHA = 0

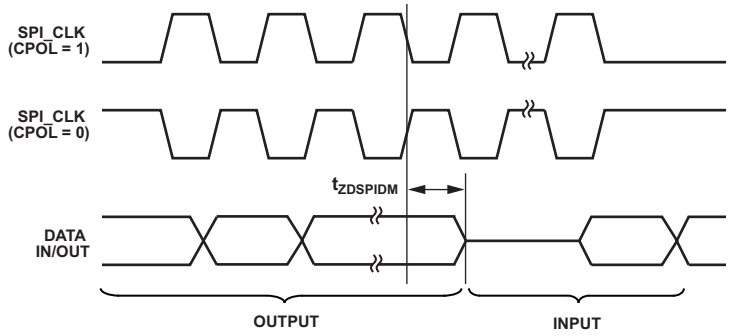

Figure 45. SPI_CLK Valid Edge to Data-Out High Impedance in Master Mode with CPHA = 1

Table 63. 10/100 Ethernet MAC Controller (EMAC) Timing: RMII Station Management

Parameter[1]		Min	Max	Unit
Timing Requirements				
t_{MDIOS}	ETHx_MDIO Input Valid to ETHx_MDC Rising Edge (Setup)	14		ns
t_{MDCIH}	ETHx_MDC Rising Edge to ETHx_MDIO Input Invalid (Hold)	0		ns
Switching Characteristics				
t_{MDCOV}	ETHx_MDC Falling Edge to ETHx_MDIO Output Valid		t_{SCLK} + 5	ns
t_{MDCOH}	ETHx_MDC Falling Edge to ETHx_MDIO Output Invalid (Hold)	t_{SCLK} – 2.5		ns

[1] ETHx_MDC/ETHx_MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. ETHx_MDC is an output clock whose minimum period is programmable as a multiple of the system clock SCLK. ETHx_MDIO is a bidirectional data line.

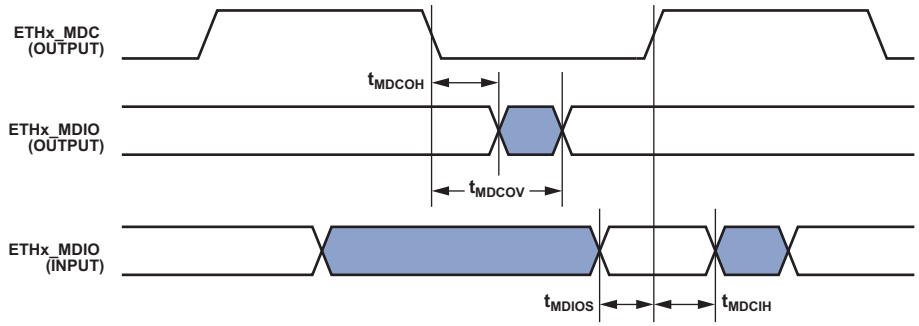

Figure 54. 10/100 Ethernet MAC Controller Timing: RMII Station Management

Debug Interface (JTAG Emulation Port) Timing

Table 67 and Figure 58 provide I/O timing, related to the debug interface (JTAG emulator port).

Table 67. JTAG Emulation Port Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	JTG_TCK Period	20		ns
t_{STAP}	JTG_TDI, JTG_TMS Setup Before JTG_TCK High	4		ns
t_{HTAP}	JTG_TDI, JTG_TMS Hold After JTG_TCK High	4		ns
t_{SSYS}	System Inputs Setup Before JTG_TCK High[1]	12		ns
t_{HSYS}	System Inputs Hold After JTG_TCK High[1]	5		ns
t_{TRSTW}	$\overline{\text{JTG\_TRST}}$ Pulse Width (Measured in JTG_TCK cycles)[2]	4		t_{TCK}
Switching Characteristics				
t_{DTDO}	JTG_TDO Delay from JTG_TCK Low		13.5	ns
t_{DSYS}	System Outputs Delay After JTG_TCK Low[3]		17	ns

[1] System inputs = PA_xx, PB_xx, PC_xx, PD_xx, PE_xx, PF_xx, SYS_BMODEx, $\overline{\text{SYS\_HWRST}}$, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_NMI}}$, TWI0_SCL, TWI0_SDA, USB_ID.
[2] 50 MHz maximum.
[3] System outputs = PA_xx, PB_xx, PC_xx, PD_xx, PE_xx, PF_xx, $\overline{\text{SMC0\_AMS0}}$, $\overline{\text{SMC0\_ARE}}$, $\overline{\text{SMC0\_AWE}}$, SYS_CLKOUT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_RESOUT}}$.

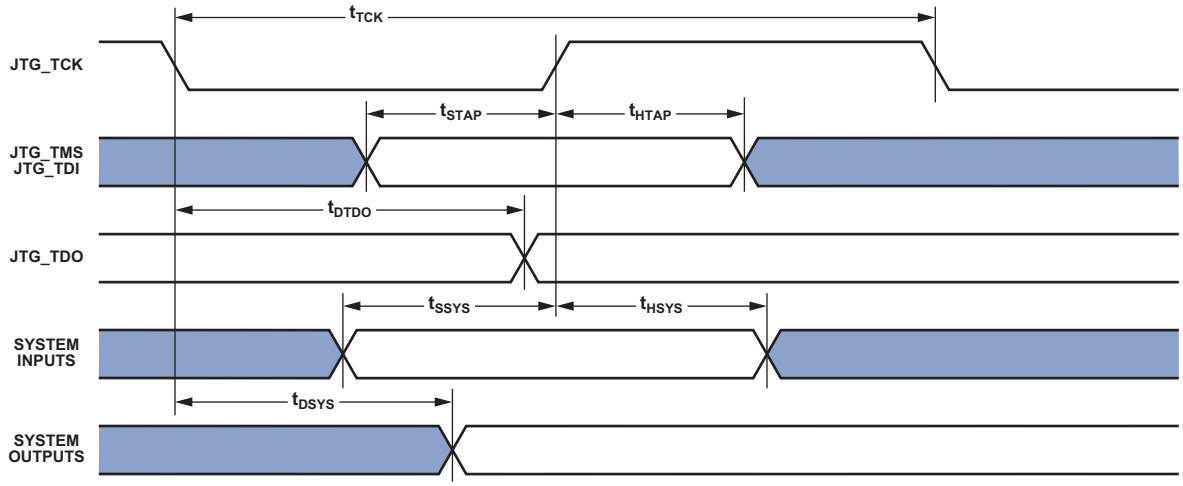

Figure 58. JTAG Emulation Port Timing

Table 72. ADSP-CM402F/ADSP-CM403F 120-Lead LQFP Lead Assignments (Alphabetical by Pin Name)

Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.
ADC0_VIN00	93	GND	121	PB_03	111	TWI0_SCL	28
ADC0_VIN01	92	GND_ANA0	79	PB_04	110	TWI0_SDA	29
ADC0_VIN02	91	GND_ANA1	71	PB_05	107	VDD_ANA0	80
ADC0_VIN03	89	GND_ANA2	90	PB_06	105	VDD_ANA1	70
ADC0_VIN04	88	GND_ANA3	61	PB_07	106	VDD_EXT	2
ADC0_VIN05	87	GND_VREF0	76	PB_08	103	VDD_EXT	9
ADC0_VIN06	86	GND_VREF1	74	PB_09	104	VDD_EXT	17
ADC0_VIN07	85	JTG_TCK/SWCLK	31	PB_10	102	VDD_EXT	22
ADC0_VIN08	84	JTG_TDI	30	PB_11	50	VDD_EXT	27
ADC0_VIN09	83	JTG_TDO/SWO	33	PB_12	51	VDD_EXT	36
ADC0_VIN10	82	JTG_TMS/SWDIO	34	PB_13	48	VDD_EXT	43
ADC0_VIN11	81	$\overline{\text{JTG\_TRST}}$	32	PB_14	46	VDD_EXT	49
ADC1_VIN00	57	PA_00	19	PB_15	47	VDD_EXT	53
ADC1_VIN01	58	PA_01	15	PC_00	45	VDD_EXT	95
ADC1_VIN02	59	PA_02	14	PC_01	42	VDD_EXT	97
ADC1_VIN03	60	PA_03	13	PC_02	41	VDD_EXT	100
ADC1_VIN04	62	PA_04	12	PC_03	40	VDD_EXT	101
ADC1_VIN05	63	PA_05	11	PC_04	39	VDD_EXT	109
ADC1_VIN06	64	PA_06	10	PC_05	38	VDD_EXT	116
ADC1_VIN07	65	PA_07	8	PC_06	37	VDD_INT	16
ADC1_VIN08	66	PA_08	7	PC_07	35	VDD_INT	44
ADC1_VIN09	67	PA_09	6	REFCAP	75	VDD_INT	54
ADC1_VIN10	68	PA_10	5	SYS_BMODE0	120	VDD_INT	96
ADC1_VIN11	69	PA_11	4	SYS_BMODE1	119	VDD_INT	108
BYP_A0	78	PA_12	3	SYS_CLKIN	24	VDD_VREG	26
BYP_A1	72	PA_13	1	SYS_CLKOUT	118	VREF0	77
BYP_D0	55	PA_14	117	$\overline{\text{SYS\_FAULT}}$	20	VREF1	73
DAC0_VOUT	94	PA_15	115	$\overline{\text{SYS\_HWRST}}$	21	VREG_BASE	25
DAC1_VOUT	56	PB_00	114	$\overline{\text{SYS\_NMI}}$	99		
GND	52	PB_01	113	$\overline{\text{SYS\_RESOUT}}$	18		
GND	98	PB_02	112	SYS_XTAL	23		

* Pin no. 121 is the GND supply (see Figure 66) for the processor; this pad **must** connect to GND.

Figure 65 shows the top view of the 120-lead LQFP package lead configuration and Figure 66 shows the bottom view of the 120-lead LQFP package lead configuration.

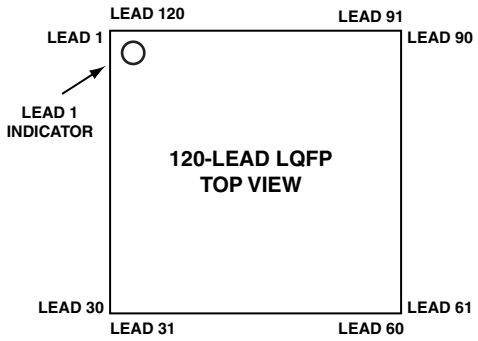

Figure 65. 120-Lead LQFP Lead Configuration (Top View)

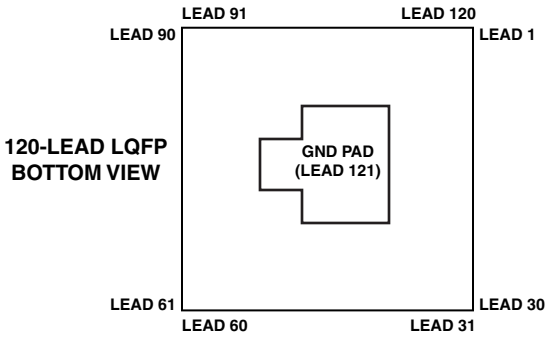

Figure 66. 120-Lead LQFP Lead Configuration (Bottom View)

Table 73. ADSP-CM407F/ADSP-CM408F 176-Lead LQFP Lead Assignments (Numerical by Lead Number) (Continued)

Lead No.	Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.	Pin Name
30	SYS_CLKIN	75	PE_13	120	ADC0_VIN03	165	VDD_EXT
31	VREG_BASE	76	PB_14	121	ADC0_VIN02	166	PD_01
32	VDD_VREG	77	PB_15	122	ADC0_VIN01	167	PD_02
33	VDD_EXT	78	PB_13	123	ADC0_VIN00	168	PB_01
34	USB0_DM	79	VDD_EXT	124	GND_ANA2	169	PD_00
35	USB0_DP	80	PB_11	125	VDD_EXT	170	PA_15
36	USB0_VBUS	81	PB_12	126	PE_03	171	PB_00
37	USB0_ID	82	PE_12	127	PE_02	172	VDD_EXT
38	PC_10	83	GND	128	VDD_INT	173	PA_14
39	PC_08	84	PE_11	129	VDD_EXT	174	SYS_CLKOUT
40	PC_09	85	PE_10	130	PE_01	175	SYS_BMODE1
41	VDD_EXT	86	VDD_EXT	131	GND	176	SYS_BMODE0
42	TWI0_SCL	87	PE_09	132	$\overline{\text{SYS\_NMI}}$	177	GND
43	TWI0_SDA	88	PE_08	133	PE_00		
44	JTG_TDI	89	PE_07	134	PD_15		
45	JTG_TCK/SWCLK	90	PE_06	135	PD_14		

* Pin no. 177 is the GND supply (see Figure 68) for the processor; this pad **must** connect to GND.

Table 74. ADSP-CM407F/ADSP-CM408F 176-Lead LQFP Lead Assignments (Alphabetical by Pin Name)

Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.
ADC0_VIN00	123	PA_12	3	PD_09	143	$\overline{\text{SYS\_RESOUT}}$	24
ADC0_VIN01	122	PA_13	1	PD_10	140	SYS_XTAL	29
ADC0_VIN02	121	PA_14	173	PD_11	141	TWI0_SCL	42
ADC0_VIN03	120	PA_15	170	PD_12	138	TWI0_SDA	43
ADC0_VIN04	119	PB_00	171	PD_13	139	USB0_DM	34
ADC0_VIN05	118	PB_01	168	PD_14	135	USB0_DP	35
ADC0_VIN06	117	PB_02	162	PD_15	134	USB0_ID	37
ADC0_VIN07	116	PB_03	159	PE_00	133	USB0_VBUS	36
ADC1_VIN00	97	PB_04	160	PE_01	130	VDD_ANA0	115
ADC1_VIN01	98	PB_05	156	PE_02	127	VDD_ANA1	105
ADC1_VIN02	99	PB_06	155	PE_03	126	VDD_EXT	2
ADC1_VIN03	100	PB_07	154	PE_04	92	VDD_EXT	8
ADC1_VIN04	101	PB_08	153	PE_05	91	VDD_EXT	15
ADC1_VIN05	102	PB_09	152	PE_06	90	VDD_EXT	23
ADC1_VIN06	103	PB_10	151	PE_07	89	VDD_EXT	28
ADC1_VIN07	104	PB_11	80	PE_08	88	VDD_EXT	33
BYP_A0	113	PB_12	81	PE_09	87	VDD_EXT	41
BYP_A1	107	PB_13	78	PE_10	85	VDD_EXT	50
BYP_D0	95	PB_14	76	PE_11	84	VDD_EXT	57
GND	83	PB_15	77	PE_12	82	VDD_EXT	64
GND	131	PC_00	66	PE_13	75	VDD_EXT	72
GND	177	PC_01	62	PE_14	74	VDD_EXT	79
GND_ANA0	114	PC_02	63	PE_15	73	VDD_EXT	86
GND_ANA1	106	PC_03	60	PF_00	71	VDD_EXT	93

* Pin no. 177 is the GND supply (see Figure 68) for the processor; this pad **must** connect to GND.

Table 76. ADSP-CM409F 212-Ball BGA Ball Assignments (Alphabetical by Ball Name) (Continued)

Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.
GND	B02	PA_07	G01	PD_13	C13	VDD_EXT	D08
GND	C03	PA_08	G03	PD_14	A14	VDD_EXT	D09
GND	C14	PA_09	F01	PD_15	B14	VDD_EXT	D10
GND	H07	PA_10	D01	PE_00	A15	VDD_EXT	D11
GND	H08	PA_11	D02	PE_01	B16	VDD_EXT	L03
GND	H09	PA_12	E03	PE_02	A16	VDD_EXT	R07
GND	J07	PA_13	D03	PE_03	A17	VDD_EXT	R09
GND	J08	PA_14	A02	PE_04	V17	VDD_EXT	T04
GND	J09	PA_15	B04	PE_05	V16	VDD_EXT	T05
GND	K07	PB_00	A03	PE_06	U16	VDD_EXT	T14
GND	K08	PB_01	B05	PE_07	V15	VDD_EXT	T15
GND	K09	PB_02	B07	PE_08	U15	VDD_INT	D07
GND	L07	PB_03	A07	PE_09	U14	VDD_INT	D12
GND	L08	PB_04	C08	PE_10	V14	VDD_INT	H03
GND	L09	PB_05	B08	PE_11	T13	VDD_INT	R08
GND	R11	PB_06	A08	PE_12	V13	VDD_INT	R10
GND	T03	PB_07	C09	PE_13	V11	VDD_VREG	J03
GND	U02	PB_08	B09	PE_14	U11	VREF0	H16
GND	V01	PB_09	A09	PE_15	T10	VREF1	L16
GND_ANA	A18	PB_10	C10	PF_00	U10	VREG_BASE	K03
GND_ANA	B17	PB_11	T12	PF_01	V10		
GND_ANA	C16	PB_12	U13	PF_02	T09		
GND_ANA	F16	PB_13	U12	PF_03	U09		
GND_ANA	H11	PB_14	V12	PF_04	V09		

Figure 69 shows an overview of signal placement on the 212-ball CSP_BGA package.

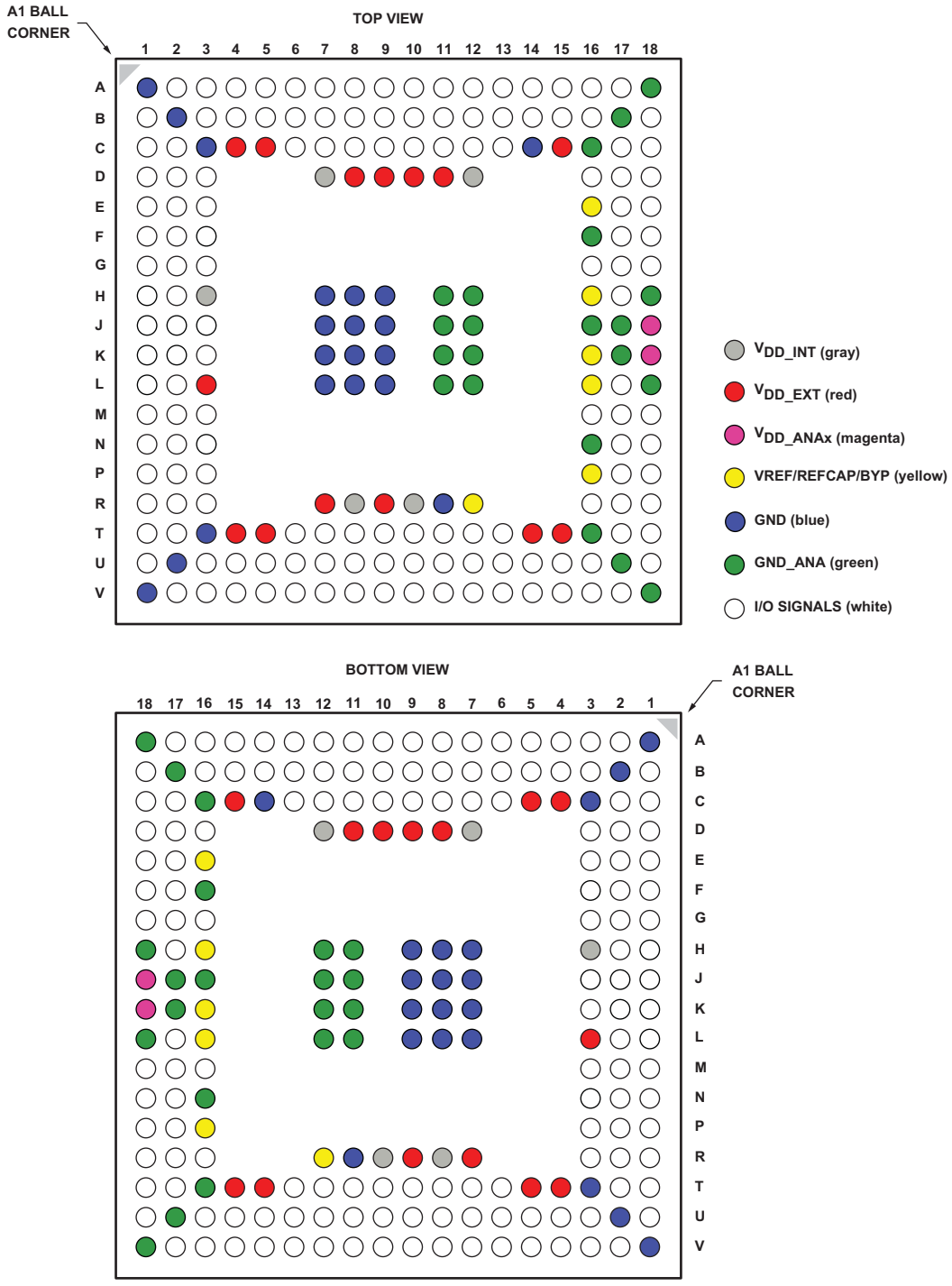

Figure 69. 212-Ball CSP_BGA Ball Configuration

ORDERING GUIDE

Model[1]	Max. Core Clock	ADC ENOB	Ethernet	Temperature Range[2]	Package Description	Package Option
ADSP-CM402CSWZ-EF	150 MHz	11+	N/A	–40°C to +105°C	120-Lead Low Profile Quad Flat Package, Exposed Pad	SW-120-3
ADSP-CM402CSWZ-FF	100 MHz	11+	N/A	–40°C to +105°C	120-Lead Low Profile Quad Flat Package, Exposed Pad	SW-120-3
ADSP-CM403CSWZ-CF	240 MHz	13+	N/A	–40°C to +105°C	120-Lead Low Profile Quad Flat Package, Exposed Pad	SW-120-3
ADSP-CM403CSWZ-EF	150 MHz	13+	N/A	–40°C to +105°C	120-Lead Low Profile Quad Flat Package, Exposed Pad	SW-120-3
ADSP-CM403CSWZ-FF	100 MHz	13+	N/A	–40°C to +105°C	120-Lead Low Profile Quad Flat Package, Exposed Pad	SW-120-3
ADSP-CM407CSWZ-AF	240 MHz	11+	1	–40°C to +105°C	176-Lead Low Profile Quad Flat Package, Exposed Pad	SW-176-3
ADSP-CM407CSWZ-BF	240 MHz	11+	N/A	–40°C to +105°C	176-Lead Low Profile Quad Flat Package, Exposed Pad	SW-176-3
ADSP-CM407CSWZ-DF	150 MHz	11+	N/A	–40°C to +105°C	176-Lead Low Profile Quad Flat Package, Exposed Pad	SW-176-3
ADSP-CM408CSWZ-AF	240 MHz	13+	1	–40°C to +105°C	176-Lead Low Profile Quad Flat Package, Exposed Pad	SW-176-3
ADSP-CM408CSWZ-BF	240 MHz	13+	N/A	–40°C to +105°C	176-Lead Low Profile Quad Flat Package, Exposed Pad	SW-176-3
ADSP-CM409CBCZ-AF	240 MHz	13+	1	–40°C to +105°C	212-Ball Chip Scale Package Ball Grid Array	BC-212-1

[1] Z = RoHS Compliant Part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. See Operating Conditions on Page 64 for the junction temperature (T_J) specification which is the only temperature specification.

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