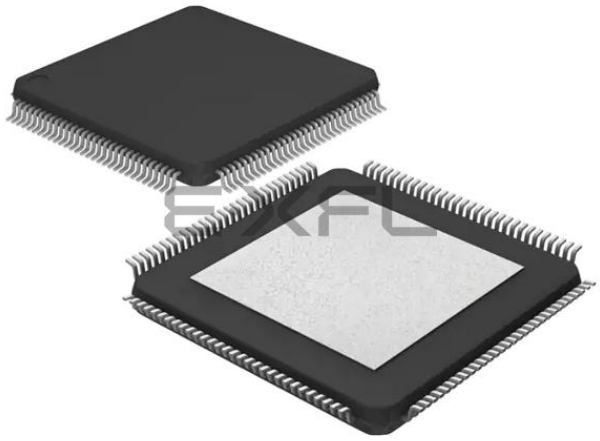

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, I²C, SPI, SPORT, UART/USART, USB
Clock Rate	240MHz
Non-Volatile Memory	FLASH (2MB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP-EP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-cm407cswz-bf

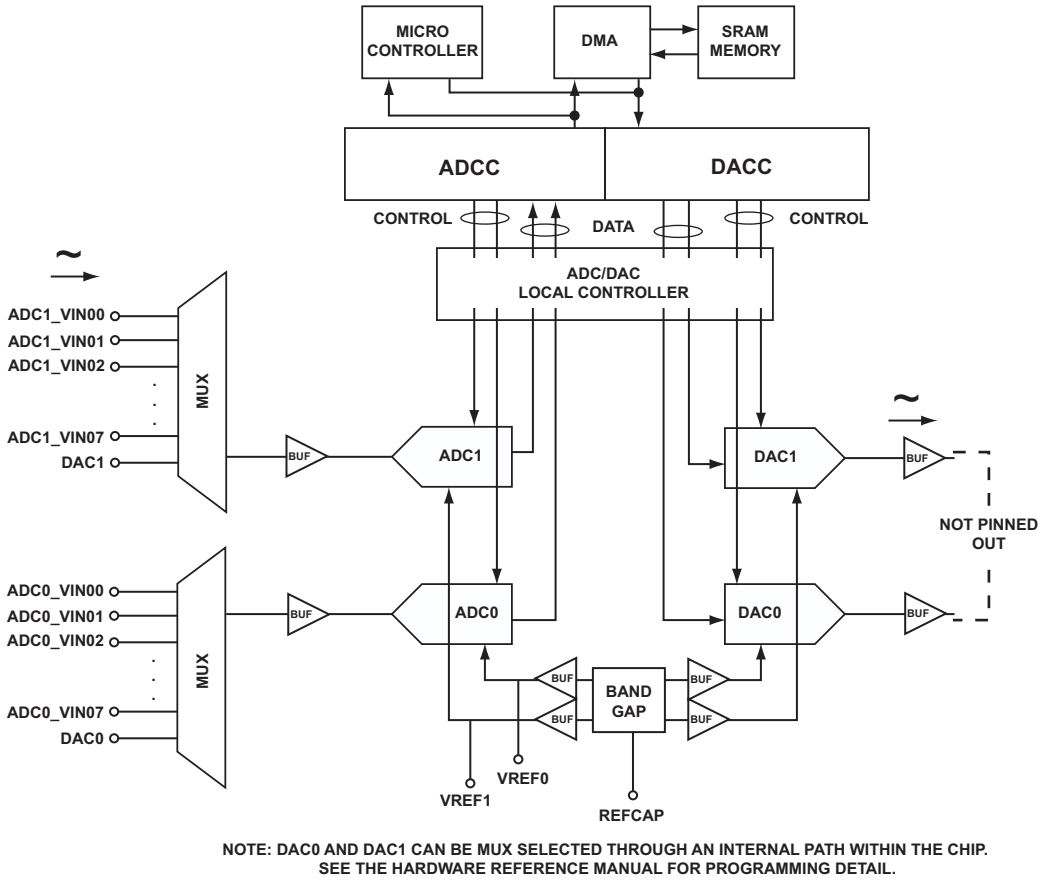

Figure 3. ADSP-CM407F/ADSP-CM408F Analog Subsystem Block Diagram

Considerations for Best Converter Performance

As with any high performance analog/digital circuit, to achieve best performance, good circuit design and board layout practices should be followed. The power supply and its noise bypass (decoupling), ground return paths and pin connections, and analog/digital routing channel paths and signal shielding, are all of first-order consideration. For application hints on design best practice, see Figure 4 and the *ADSP-CM40x Mixed-Signal Control Processor with ARM Cortex-M4 Hardware Reference*. For more information about the VREG circuit, see Figure 9.

ADC Module

The ADC module contains two 16-bit, high speed, low power successive approximation register (SAR) ADCs, allowing for dual simultaneous sampling with each ADC preceded by a 12-channel multiplexer. See ADC Specifications on Page 68 for detailed performance specifications. Input multiplexers enable conversion of up to a combined 26 analog input sources to the ADCs (12 analog inputs plus 1 DAC loopback input per ADC).

The voltage input range requirement for those analog inputs is from 0 V to 2.5 V. All analog inputs are of single-ended design. As with all single-ended inputs, signals from high impedance sources are the most difficult to measure, and depending on the electrical environment, may require an external buffer circuit for signal conditioning (see Figure 5). An on-chip pre-buffer between the multiplexer and ADC reduces the need for additional signal conditioning external to the processor. Additionally, each ADC has an on-chip 2.5 V reference that can be overdriven when an external voltage reference is preferred.

DAC Module

The DAC is a 12-bit, low power, string DAC design. The output of the DAC is buffered, and can drive an R/C load to either ground or VDD_ANA. See DAC Specifications on Page 70 for detailed performance specifications. It should be noted that on some models of the processor, the DAC outputs are not pinned out. However, these outputs are always available as one of the multiplexed inputs to the ADCs. This feature may be useful for functional self-check of the converters.

Note: On the ADSP-CM402F/CM403F/CM409F processors, the DAC output is available to the ADC as channel 12; whereas on the ADSP-CM407F/CM408F processors, the DAC output is available to the ADC as Channel 8.

PROCESSOR INFRASTRUCTURE

The following sections provide information on the primary infrastructure components of the ADSP-CM40xF processors.

DMA Controllers (DDEs)

The processor contains 17 independent and concurrently operating peripheral DMA channels plus two MDMA streams. DDE Channel 0 to Channel 16 are for peripherals and Channel 17 to Channel 20 are for MDMA.

System Event Controller (SEC)

The SEC manages the enabling and routing of system fault sources through its integrated fault management unit.

Trigger Routing Unit (TRU)

The TRU provides system-level sequence control without core intervention. The TRU maps trigger masters (generators of triggers) to trigger slaves (receivers of triggers). Slave endpoints can be configured to respond to triggers in various ways. Common applications enabled by the TRU include:

- Initiating the ADC sampling periodically in each PWM period or based on external events
- Automatically triggering the start of a DMA sequence after a sequence from another DMA channel completes
- Software triggering
- Synchronization of concurrent activities

Pin Interrupts (PINT)

Every port pin on the processor can request interrupts in either an edge-sensitive or a level-sensitive manner with programmable polarity. Interrupt functionality is decoupled from GPIO operation. Six system-level interrupt channels (PINT0 to PINT5) are reserved for this purpose. Each of these interrupt channels can manage up to 32 interrupt pins. The assignment from pin to interrupt is not performed on a pin-by-pin basis. Rather, groups of eight pins (half ports) can be flexibly assigned to interrupt channels.

Every pin interrupt channel features a special set of 32-bit memory-mapped registers that enable half-port assignment and interrupt management. This includes masking, identification, and clearing of requests. These registers also enable access to the respective pin states and use of the interrupt latches, regardless of whether the interrupt is masked or not. Most control registers feature multiple MMR address entries to write-one-to-set or write-one-to-clear them individually.

General-Purpose I/O (GPIO)

Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers:

- GPIO direction control register—Specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers —A write one to modify mechanism allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins.
- GPIO interrupt mask registers—Allow each individual GPIO pin to function as an interrupt to the processor. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers—Specify whether individual pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant.

Pin Multiplexing

The processor supports a flexible multiplexing scheme that multiplexes the GPIO pins with various peripherals. A maximum of five peripherals plus GPIO functionality is shared by each GPIO pin. All GPIO pins have a bypass path feature—that is, when the output enable and the input enable of a GPIO pin are both active, the data signal before the pad driver is looped back to the receive path for the same GPIO pin.

For more information, see:

- ADSP-CM402F/ADSP-CM403F GPIO Multiplexing for 120-Lead LQFP on Page 27.
- ADSP-CM407F/ADSP-CM408F GPIO Multiplexing for 176-Lead LQFP on Page 37.
- ADSP-CM409F GPIO Multiplexing for 212-Ball BGA on Page 48.

MEMORY ARCHITECTURE

The internal and external memory of the ADSP-CM40xF processor is shown in Figure 7 and described in the following sections.

ARM Cortex-M4 Memory Subsystem

The memory map of the ADSP-CM40xF family is based on the Cortex-M4 model from ARM. By retaining the standardized memory mapping, it becomes easier to port applications across M4 platforms. Only the physical implementation of memories inside the model differs from other vendors.

ADSP-CM40xF application development is typically based on memory blocks across CODE/SRAM and external memory regions. Sufficient internal memory is available via internal SRAM and internal flash. Additional external memory devices may be interfaced via the SMC asynchronous memory port, as well as through the SPI0 serial memory interface.

Code Region

Accesses in this region (0x0000_0000 to 0x1FFF_FFFF) are performed by the core on its ICODE and DCODE interfaces, and they target the memory and cache resources within the Cortex-M4F platform integration component.

- **Boot ROM.** A 32K byte boot ROM executed at system reset. This space supports read-only access by the M4F core only. Note that ROM memory contents cannot be modified by the user.

PROCESSOR RELIABILITY FEATURES

The processor provides the following features which can enhance or help achieve certain levels of system safety and reliability. While the level of safety is mainly dominated by system considerations, the following features are provided to enhance robustness.

Multi-Parity-Bit-Protected L1 Memories

In the processor's SRAM and cache L1 memory space, each word is protected by multiple parity bits to detect the single event upsets that occur in all RAMs.

Cortex MPU

The MPU divides the memory map into a number of regions, and allows the system programmer to define the location, size, access permissions, and memory attributes of each region. It supports independent attribute settings for each region, overlapping regions, and export of memory attributes to the system.

For more information, refer to the ARM Infocenter web page.

System Protection Unit (SPU)

All system resources and L2 memory banks can be controlled by either the processor core, memory-to-memory DMA, or the debug unit. A system protection unit (SPU) enables write accesses to specific resources that are locked to a given master. System protection is enabled in greater granularity for some modules through a global lock concept.

Watchpoint Protection

The primary purpose of watchpoints and hardware breakpoints is to serve emulator needs. When enabled, they signal an emulator event whenever user-defined system resources are accessed or a core executes from user-defined addresses. Watchdog events can be configured such that they signal the events to the core or to the SEC.

Software Watchdog

The on-chip watchdog timer can provide software-based supervision of the ADSP-CM40xF core.

Signal Watchdogs

The eight general-purpose timers feature two modes to monitor off-chip signals. The watchdog period mode monitors whether external signals toggle with a period within an expected range. The watchdog width mode monitors whether the pulse widths of external signals are in an expected range. Both modes help to detect incorrect undesired toggling (or lack thereof) of system-level signals.

Oscillator Watchdog

The oscillator watchdog monitors the external clock oscillator, and can detect the absence of clock as well as incorrect harmonic oscillation. The oscillator watchdog detection signal is routed to the fault management portion of the system event controller.

Low-Latency Sinc Filter Over-range Detection

The SINC filter units provide a low-latency secondary filter with programmable positive and negative limit detectors for each input channel. These may be used to monitor an isolation ADC bitstream for overrange or underrange conditions with a filter group delay as low as 0.7 µs on a 10 MHz bitstream. The secondary SINC filter events can be used to interrupt the core, to trigger other events directly in hardware using the trigger routing unit (TRU), or to signal the fault management unit of a system fault.

Up/Down Count Mismatch Detection

The GP counter can monitor external signal pairs, such as request/grant strobes. If the edge count mismatch exceeds the expected range, the up/down counter can flag this to the processor or to the system event controller (SEC).

Fault Management

The fault management unit is part of the system event controller (SEC). Most system events can be defined as faults. If defined as such, the SEC forwards the event to its fault management unit which may automatically reset the entire device for reboot, or simply toggle the $\overline{\text{SYS\_FAULT}}$ output pin to signal off-chip hardware. Optionally, the fault management unit can delay the action taken via a keyed sequence, to provide a final chance for the core to resolve the crisis and to prevent the fault action from being taken.

ADDITIONAL PROCESSOR PERIPHERALS

The processor contains a rich set of peripherals connected to the core via several concurrent high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see Figure 1, Block Diagram).

The processor contains high speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The following sections describe additional peripherals that were not described in the previous sections.

Timers

The processor includes several timers which are described in the following sections.

General-Purpose Timers (TIMER)

The general-purpose (GP) timer unit provides eight general-purpose programmable timers. Each timer has an external pin that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input on the TM0_ACLKx pins, an external signal on the TM0_CLK input pin, or to the internal SCLK.

registers with associated hardware. These four SWU match groups operate independently, but share common event (interrupt and trigger) outputs.

DEVELOPMENT TOOLS

The ADSP-CM40xF processor is supported with a set of highly sophisticated and easy-to-use development tools for embedded applications. For more information, see the Analog Devices website.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-CM40xF processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *ADSP-CM40x Mixed-Signal Control Processor with ARM Cortex-M4 Hardware Reference*
- *ADSP-CM402F/CM403F/CM407F/CM408F/CM409F Anomaly Sheet*

This data sheet describes the ARM Cortex-M4 core and memory architecture used on the ADSP-CM40xF processor, but does not provide detailed programming information for the ARM processor. For more information about programming the ARM processor, visit the ARM Infocenter web page.

The applicable documentation for programming the ARM Cortex-M4 processor include:

- *Cortex®-M4 Devices Generic User Guide*
- *CoreSight™ ETM™-M4 Technical Reference Manual*
- *Cortex®-M4 Technical Reference Manual*

RELATED SIGNAL CHAINS

A signal chain is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (http:\\www.analog.com\circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

SECURITY FEATURES DISCLAIMER

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Table 6. ADSP-CM40xF Detailed Signal Description (Continued)

Signal Name	Direction	Description
USB_ID	Input	**USB OTG ID.** Senses whether the controller is a host or device. This signal is pulled low when an A-type plug is sensed (signifying that the USB controller is the A device), but the input is high when a B-type plug is sensed (signifying that the USB controller is the B device).
USB_VBC	Output	**USB VBUS Control.** Controls an external voltage source to supply VBUS when in host mode. May be configured as open drain. Polarity is configurable as well.
USB_VBUS	I/O	**USB Bus Voltage.** Connects to bus voltage in host and device modes.
VREFn	I/O	**Voltage Reference for ADC.** When internal reference is selected for ADC, the VREF pin is used for connecting bypass caps. When external reference is selected, an external reference device should be connected to these pins to supply the external reference voltage. n=0,1.
VREG_BASE	Output	**Voltage Regulator Base Node.** Connected to Base of PNP transistor when using internal VDD_INT reference.

ADSP-CM402F/ADSP-CM403F 120-LEAD LQFP SIGNAL DESCRIPTIONS

The processor's pin definitions are shown in Table 7. The columns in this table provide the following information:

- Signal Name: The Signal Name column in the table includes the signal name for every pin and (where applicable) the GPIO multiplexed pin function for every pin.
- Description: The Description column in the table provides a verbose (descriptive) name for the signal.
- General-Purpose Port: The Port column in the table shows whether or not the signal is multiplexed with other signals on a general-purpose I/O port pin.
- Pin Name: The Pin Name column in the table identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).

Table 7. ADSP-CM402F/ADSP-CM403F 120-Lead LQFP Signal Descriptions

Signal Name	Description	Port	Pin Name
ADC0_VIN00	Channel 0 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN00
ADC0_VIN01	Channel 1 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN01
ADC0_VIN02	Channel 2 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN02
ADC0_VIN03	Channel 3 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN03
ADC0_VIN04	Channel 4 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN04
ADC0_VIN05	Channel 5 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN05
ADC0_VIN06	Channel 6 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN06
ADC0_VIN07	Channel 7 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN07
ADC0_VIN08	Channel 8 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN08
ADC0_VIN09	Channel 9 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN09
ADC0_VIN10	Channel 10 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN10
ADC0_VIN11	Channel 11 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN11
ADC1_VIN00	Channel 0 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN00
ADC1_VIN01	Channel 1 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN01
ADC1_VIN02	Channel 2 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN02
ADC1_VIN03	Channel 3 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN03
ADC1_VIN04	Channel 4 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN04
ADC1_VIN05	Channel 5 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN05
ADC1_VIN06	Channel 6 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN06
ADC1_VIN07	Channel 7 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN07
ADC1_VIN08	Channel 8 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN08
ADC1_VIN09	Channel 9 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN09
ADC1_VIN10	Channel 10 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN10
ADC1_VIN11	Channel 11 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN11
BYP_A0	On-chip Analog Power Regulation Bypass Filter Node for ADC0 (see recommended bypass - Figure 4 on Page 6)	Not Muxed	BYP_A0
BYP_A1	On-chip Analog Power Regulation Bypass Filter Node for ADC1 (see recommended bypass - Figure 4 on Page 6)	Not Muxed	BYP_A1
BYP_D0	On-chip Digital Power Regulation Bypass Filter Node for Analog Subsystem (see recommended bypass - Figure 4 on Page 6)	Not Muxed	BYP_D0
CAN0_RX	CAN0 Receive	B	PB_15
CAN0_TX	CAN0 Transmit	C	PC_00
CAN1_RX	CAN1 Receive	B	PB_10
CAN1_TX	CAN1 Transmit	B	PB_11
CNT0_DG	CNT0 Count Down and Gate	B	PB_02
CNT0_OUTA	CNT0 Output Divider A	B	PB_13

Table 7. ADSP-CM402F/ADSP-CM403F 120-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
TM0_ACLK1	TIMER0 Alternate Clock 1	B	PB_11
TM0_ACLK2	TIMER0 Alternate Clock 2	A	PA_11
TM0_ACLK3	TIMER0 Alternate Clock 3	A	PA_10
TM0_ACLK4	TIMER0 Alternate Clock 4	A	PA_09
TM0_ACLK5	TIMER0 Alternate Clock 5	A	PA_08
TM0_CLK	TIMER0 Clock	B	PB_06
TM0_TMR0	TIMER0 Timer 0	B	PB_07
TM0_TMR1	TIMER0 Timer 1	B	PB_08
TM0_TMR2	TIMER0 Timer 2	B	PB_09
TM0_TMR3	TIMER0 Timer 3	A	PA_15
TM0_TMR4	TIMER0 Timer 4	A	PA_12
TM0_TMR5	TIMER0 Timer 5	A	PA_13
TM0_TMR6	TIMER0 Timer 6	A	PA_14
TM0_TMR7	TIMER0 Timer 7	B	PB_05
TRACE_CLK	Embedded Trace Module Clock	B	PB_00
TRACE_D00	Embedded Trace Module Data 0	B	PB_01
TRACE_D01	Embedded Trace Module Data 1	B	PB_02
TRACE_D02	Embedded Trace Module Data 2	B	PB_03
TRACE_D03	Embedded Trace Module Data 3	C	PC_02
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	B	PB_05
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	B	PB_04
$\overline{\text{UART0\_RX}}$	UART0 Receive	C	PC_01
$\overline{\text{UART0\_TX}}$	UART0 Transmit	C	PC_02
$\overline{\text{UART1\_CTS}}$	UART1 Clear to Send	A	PA_11
$\overline{\text{UART1\_RTS}}$	UART1 Request to Send	C	PC_07
$\overline{\text{UART1\_RX}}$	UART1 Receive	B	PB_08
$\overline{\text{UART1\_RX}}$	UART1 Receive	B	PB_15
$\overline{\text{UART1\_TX}}$	UART1 Transmit	B	PB_09
$\overline{\text{UART1\_TX}}$	UART1 Transmit	C	PC_00
$\overline{\text{UART2\_RX}}$	UART2 Receive	B	PB_12
$\overline{\text{UART2\_TX}}$	UART2 Transmit	C	PC_07
VDD_ANA0	Analog Voltage Domain (see recommended bypass - Figure 4 on Page 6)	Not Muxed	VDD_ANA0
VDD_ANA1	Analog Voltage Domain (see recommended bypass - Figure 4 on Page 6)	Not Muxed	VDD_ANA1
VDD_EXT	External Voltage Domain	Not Muxed	VDD_EXT
VDD_INT	Internal Voltage Domain	Not Muxed	VDD_INT
VDD_VREG	VREG Supply Voltage	Not Muxed	VDD_VREG
VREF0	Voltage Reference for ADC0. Default configuration is Output (see recommended bypass - Figure 4 on Page 6)	Not Muxed	VREF0
VREF1	Voltage Reference for ADC1. Default configuration is Output (see recommended bypass - Figure 4 on Page 6)	Not Muxed	VREF1
VREG_BASE	Voltage Regulator Base Node	Not Muxed	VREG_BASE

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PD_08	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PD Position 8 | SMC0 Address 6 | TM0 Common Clock Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PD_09	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PD Position 9 | SMC0 Address 7 | TM0 Timer5 Alternate Capture Input Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PD_10	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PD Position 10 | SMC0 Address 8 | TM0 Timer4 Alternate Capture Input Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PD_11	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PD Position 11 | SMC0 Address 9 | TM0 Timer3 Alternate Capture Input Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PD_12	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PD Position 12 | SMC0 Address 10 | TM0 Timer2 Alternate Capture Input Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PD_13	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PD Position 13 | SMC0 Address 11 | TM0 Timer1 Alternate Capture Input Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PD_14	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PD Position 14 | SMC0 Address 12 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PD_15	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PD Position 15 | SMC0 Address 13 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PE_00	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 0 | SMC0 Address 14 | SPORT0 Channel A Clock Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PE_01	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 1 | SMC0 Address 15 | SPORT0 Channel A Frame Sync Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PE_02	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 2 | SMC0 Address 16 | SPORT0 Channel Data 0 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PE_03	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 3 | SMC0 Address 17 | SPORT0 Channel Data 1 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PE_04	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 4 | SMC0 Address 18 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PE_05	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 5 | SMC0 Address 19 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PE_06	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 6 | ETH0 PTP Clock Input | SMC0 Address 20 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PE_07	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 7 | ETH0 PTP Auxiliary Trigger Input | SMC0 Address 21 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PE_08	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 8 | ETH0 PTP Pulse-Per-Second Output | SMC0 Address 22 | CNT2 Count Zero Marker Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PE_09	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 9 | ETH0 Carrier Sense | SMC0 Address 23 | CNT2 Count Up and Direction Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PE_10	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 10 | ETH0 Management Channel Serial Data | SMC0 Memory Select 1 | CNT2 Count Down and Gate Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PE_11	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 11 | ETH0 Management Channel Clock | SMC0 Address 24 | CNT3 Count Zero Marker Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PE_12	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 12 | ETH0 Transmit Data 0 | CNT3 Count Up and Direction Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PE_13	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PE Position 13 | ETH0 Transmit Data 1 | CNT3 Count Down and Gate Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
USB0_ID	I/O	na	none	none	none	VDD_EXT	Desc: USB0 OTG ID Notes: If USB is not used, connect to ground.
USB0_VBUS	I/O	E	none	none	none	VDD_EXT	Desc: USB0 Bus Voltage Notes: If USB is not used, pull low.
VDD_ANA0	s	na	none	none	none	na	Desc: Analog Power Supply Voltage 3.13 V to 3.47 V (see recommended bypass - Figure 4 on Page 6) Notes: No notes.
VDD_ANA1	s	na	none	none	none	na	Desc: Analog Power Supply Voltage 3.13 V to 3.47 V (see recommended bypass - Figure 4 on Page 6) Notes: No notes.
VDD_EXT	s	na	none	none	none	na	Desc: External Voltage Domain Notes: No notes.
VDD_INT	s	na	none	none	none	na	Desc: Internal Voltage Domain Notes: No notes.
VDD_VREG	s	na	none	none	none	na	Desc: VREG Supply Voltage Notes: No notes.
VREF0	a	na	none	none	none	na	Desc: Voltage Reference for ADC0. Default configuration is Output (see recommended bypass - Figure 4 on Page 6) Notes: When using internal ADC reference, this pin should never be loaded with resistive or inductive load or connected to anything but the recommended capacitor. When using external ADC reference, connect to externally generated reference voltage supply
VREF1	a	na	none	none	none	na	Desc: Voltage Reference for ADC1. Default configuration is Output (see recommended bypass - Figure 4 on Page 6) Notes: When using internal ADC reference, this pin should never be loaded with resistive or inductive load or connected to anything but the recommended capacitor. When using external ADC reference, connect to externally generated reference voltage supply
VREG_BASE	a	na	none	none	none	na	Desc: Voltage Regulator Base Node Notes: When unused, connect to GND or pull low

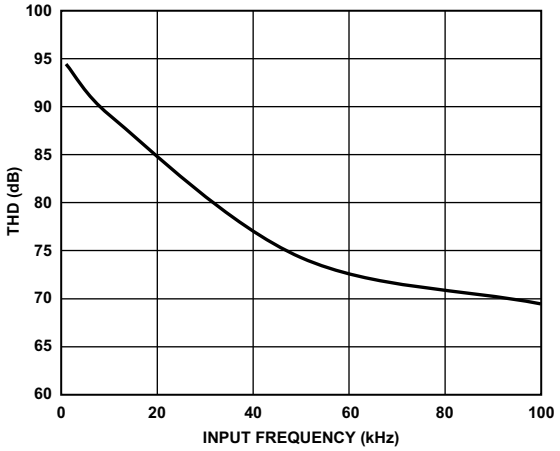

Figure 17. THD vs. Frequency, 0 V to 2.5 V Sine Wave Input

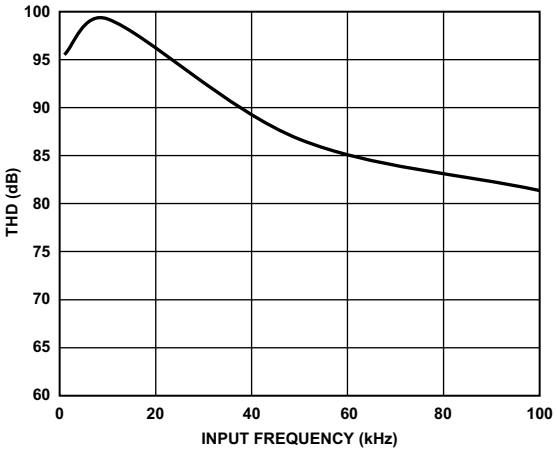

Figure 18. THD vs. Frequency, 0 V to 1.25 V Sine Wave Input

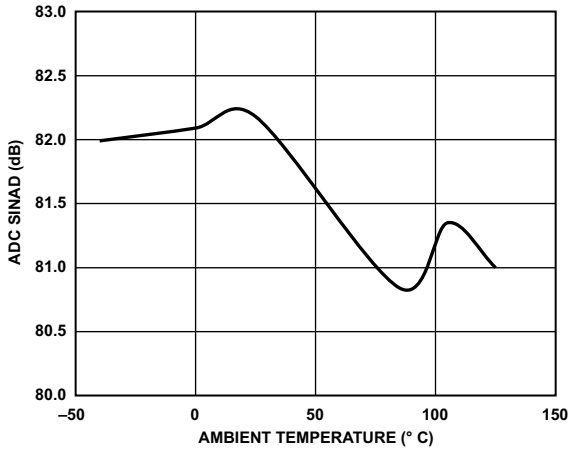

Figure 19. ADC SINAD vs. Temperature, 0 V to 2.5 V (1 kHz) Sine Wave Input

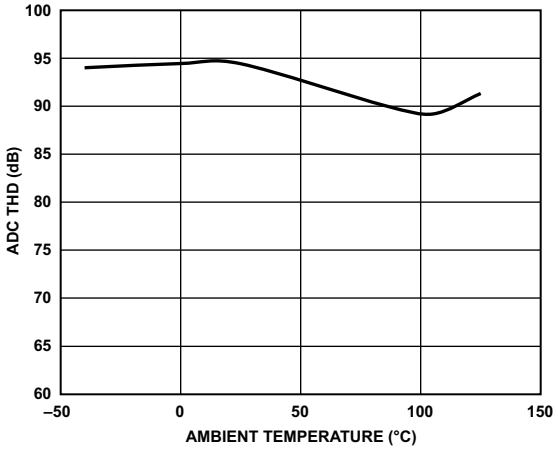

Figure 20. ADC THD vs. Temperature, 0 V to 2.5 V (1 kHz) Sine Wave Input

Asynchronous Flash Read

Table 37 and Figure 27 show asynchronous flash memory read timing, related to the static memory controller (SMC).

Table 37. Asynchronous Flash Read

Parameter		Min	Max	Unit
Switching Characteristics				
t_{AMSADV}	SMC0_Ax (Address)/$\overline{\text{SMC0\_AMSx}}$ Assertion Before $\overline{\text{SMC0\_AOE}}$ Low[1]	PREST × t_{SCLK} – 2		ns
t_{WADV}	$\overline{\text{SMC0\_AOE}}$ Active Low Width[2]	RST × t_{SCLK} – 3		ns
$t_{DADVARE}$	$\overline{\text{SMC0\_ARE}}$ Low Delay From $\overline{\text{SMC0\_AOE}}$ High[3]	PREAT × t_{SCLK} – 3		ns
t_{HARE}	Output[4] Hold After $\overline{\text{SMC0\_ARE}}$ High[5]	RHT × t_{SCLK} – 2		ns
t_{WARE}[6]	$\overline{\text{SMC0\_ARE}}$ Active Low Width[7]	RAT × t_{SCLK} – 2		ns

[1] PREST value set using the SMC_BxETIM.PREST bits.
[2] RST value set using the SMC_BxTIM.RST bits.
[3] PREAT value set using the SMC_BxETIM.PREAT bits.
[4] Output signals are SMC0_Ax, $\overline{\text{SMC0\_AMS}}$.
[5] RHT value set using the SMC_BxTIM.RHT bits.
[6] SMC0_BxCTL.ARDYEN bit = 0.
[7] RAT value set using the SMC_BxTIM.RAT bits.

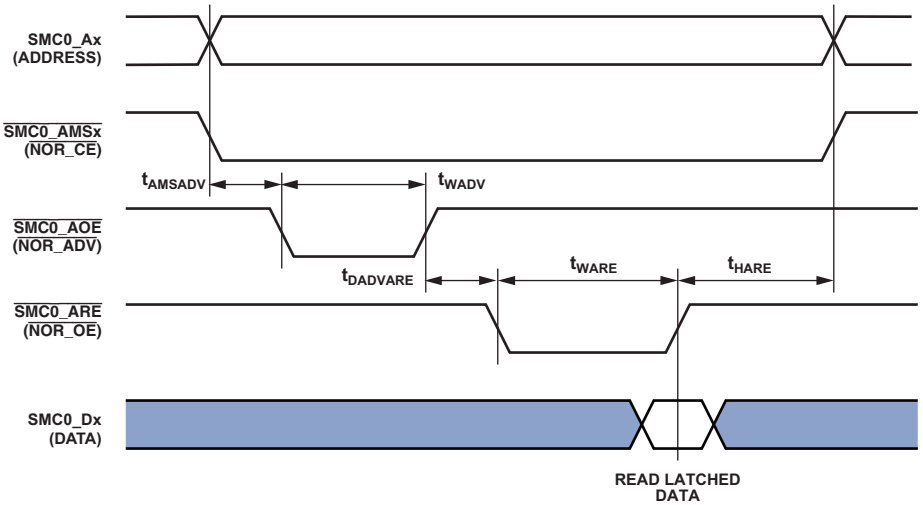

Figure 27. Asynchronous Flash Read

Asynchronous Flash Write

Table 40 and Figure 30 show asynchronous flash memory write timing, related to the static memory controller (SMC).

Table 40. Asynchronous Flash Write

Parameter		Min	Max	Unit
Switching Characteristics				
t_{AMSADV}	SMC0_Ax/$\overline{\text{SMC0\_AMSx}}$ Assertion Before $\overline{\text{SMC0\_AOE}}$ Low[1]		PREST × t_{SCLK} – 2	ns
$t_{DADVAWE}$	$\overline{\text{SMC0\_AWE}}$ Low Delay From $\overline{\text{SMC0\_AOE}}$ High[2]		PREAT × t_{SCLK} – 6.2	ns
t_{WADV}	$\overline{\text{SMC0\_AOE}}$ Active Low Width[3]		WST × t_{SCLK} – 3	ns
t_{HAWE}	Output[4] Hold After $\overline{\text{SMC0\_AWE}}$ High[5]		WHT × t_{SCLK} – 2	ns
t_{WAWE}[6]	$\overline{\text{SMC0\_AWE}}$ Active Low Width[7]		WAT × t_{SCLK} – 2	ns

[1] PREST value set using the SMC_BxETIM.PREST bits.
[2] PREAT value set using the SMC_BxETIM.PREAT bits.
[3] WST value set using the SMC_BxTIM.WST bits.
[4] Output signals are DATA, SMC0_Ax, $\overline{\text{SMC0\_AMSx}}$.
[5] WHT value set using the SMC_BxTIM.WHT bits.
[6] SMC_BxCTL.ARDYEN bit = 0.
[7] WAT value set using the SMC_BxTIM.WAT bits.

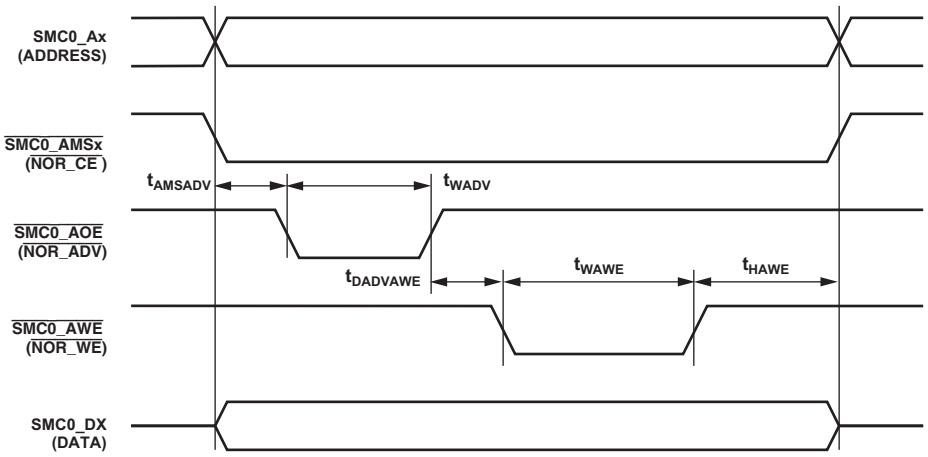

Figure 30. Asynchronous Flash Write

All Accesses

Table 41 describes timing that applies to all memory accesses, related to the static memory controller (SMC).

Table 41. All Accesses

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TURN}	$\overline{\text{SMC0\_AMSx}}$ Inactive Width	(IT + TT) × t_{SCLK} – 2		ns

Table 43. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}	Frame Sync Setup Before SPT_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[1]	12		ns
t_{HFSI}	Frame Sync Hold After SPT_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[1]	–0.5		ns
t_{SDRI}	Receive Data Setup Before SPT_CLK[1]	3.4		ns
t_{HDRI}	Receive Data Hold After SPT_CLK[1]	1.5		ns
Switching Characteristics				
t_{DFSI}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]		3.5	ns
t_{HOFSI}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]	–1		ns
t_{DDTI}	Transmit Data Delay After SPT_CLK[2]		3.5	ns
t_{HDTI}	Transmit Data Hold After SPT_CLK[2]	–1.25		ns
t_{SCLKIW}	SPT_CLK Width[3]	$0.5 \times t_{SPTCLKPROG} - 1$		ns
t_{SPTCLK}	SPT_CLK Period[3]	$t_{SPTCLKPROG} - 1$		ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.
[3] See Table 27 Clock Related Operating Conditions for details on the minimum period that may be programmed for $f_{SPTCLKPROG}$.

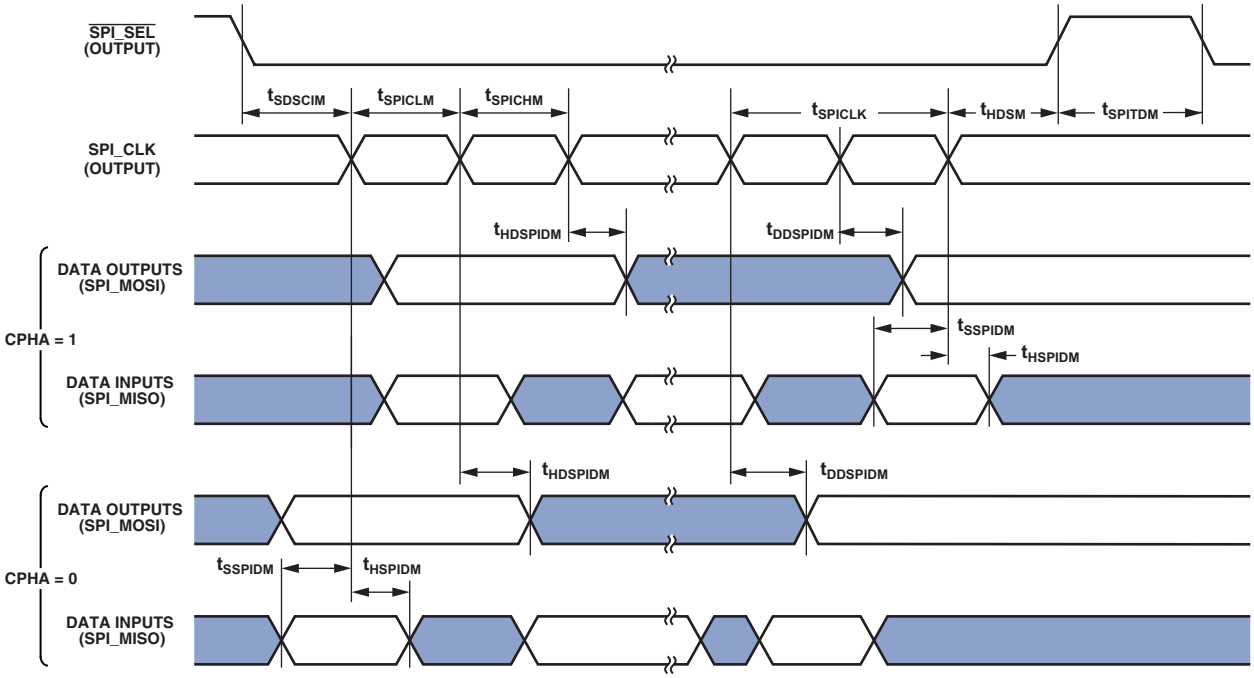

Figure 35. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port—SPI_RDY Master Timing

SPI_RDY is used to provide flow control. The CPOL and CPHA bits are set in SPI_CTL, while LEADX, LAGX, and STOP are in SPI_DLY.

Table 52. SPI Port—SPI_RDY Master Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SRDYSCKM0}$	Minimum Setup Time for SPI_RDY De-assertion in Master Mode Before Last Valid SPI_CLK Edge of Valid Data Transfer to Block Subsequent Transfer with CPHA = 0	$(2 + 2 \times BAUD^{1}) \times t_{SCLK} + 10$		ns
$t_{SRDYSCKM1}$	Minimum Setup Time for SPI_RDY De-assertion in Master Mode Before Last Valid SPI_CLK Edge of Valid Data Transfer to Block Subsequent Transfer with CPHA = 1	$(2 + 2 \times BAUD^{1}) \times t_{SCLK} + 10$		ns
Switching Characteristics				
$t_{SRDYSCKM}$	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA/CPOL = 0 and BAUD = 0 (STOP, LEAD, LAG = 0)	$4.5 \times t_{SCLK}$	$5.5 \times t_{SCLK} + 10$	ns
	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA/CPOL = 1 and BAUD = 0 (STOP, LEAD, LAG = 0)	$4 \times t_{SCLK}$	$5 \times t_{SCLK} + 10$	ns
	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA/CPOL = 0 and BAUD ≥ 1 (STOP, LEAD, LAG = 0)	$(1 + 1.5 \times BAUD^{1}) \times t_{SCLK}$	$(2 + 2.5 \times BAUD^{1}) \times t_{SCLK} + 10$	ns
	Time Between Assertion of SPI_RDY by Slave and First Edge of SPI_CLK for New SPI Transfer with CPHA/CPOL = 1 and BAUD ≥ 1 (STOP, LEAD, LAG = 0)	$(1 + 1 \times BAUD^{1}) \times t_{SCLK}$	$(2 + 2 \times BAUD^{1}) \times t_{SCLK} + 10$	ns

[1] BAUD value set using the SPI_CLK.BAUD bits. BAUD value = SPI_CLK.BAUD bits + 1.

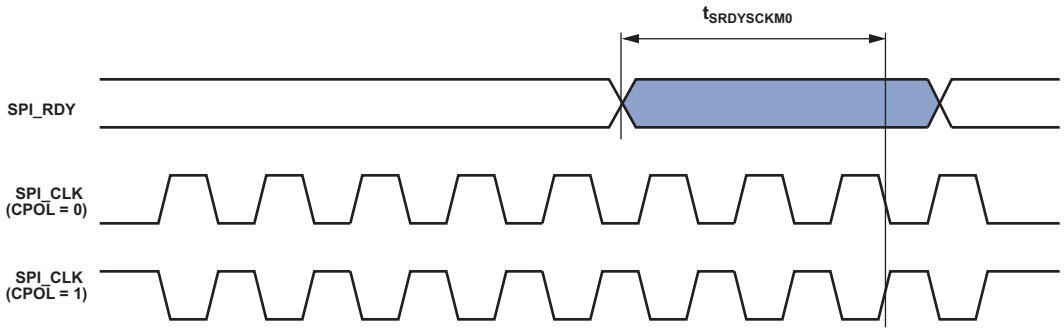

Figure 41. SPI_RDY Setup Before SPI_CLK with CPHA = 0

Figure 65 shows the top view of the 120-lead LQFP package lead configuration and Figure 66 shows the bottom view of the 120-lead LQFP package lead configuration.

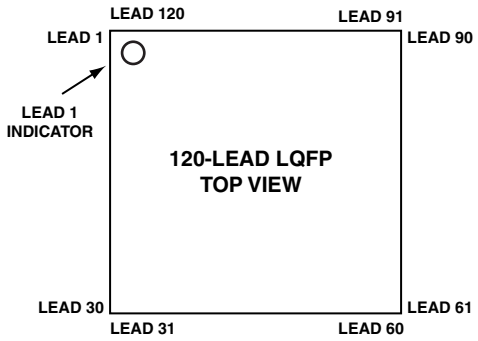

Figure 65. 120-Lead LQFP Lead Configuration (Top View)

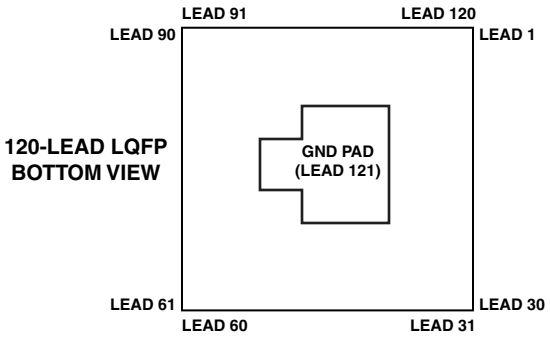

Figure 66. 120-Lead LQFP Lead Configuration (Bottom View)

Figure 67 shows the top view of the 176-lead LQFP lead configuration and Figure 68 shows the bottom view of the 176-lead LQFP lead configuration.

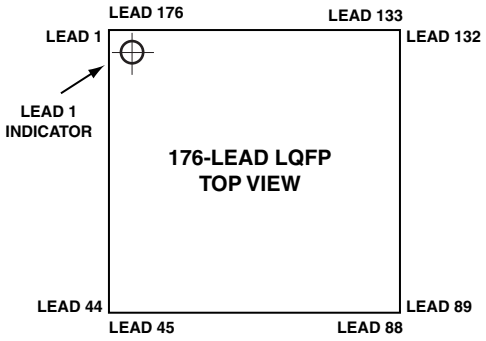

Figure 67. 176-Lead LQFP Lead Configuration (Top View)

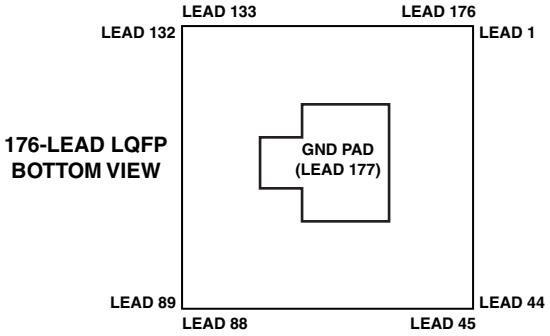

Figure 68. 176-Lead LQFP Lead Configuration (Bottom View)

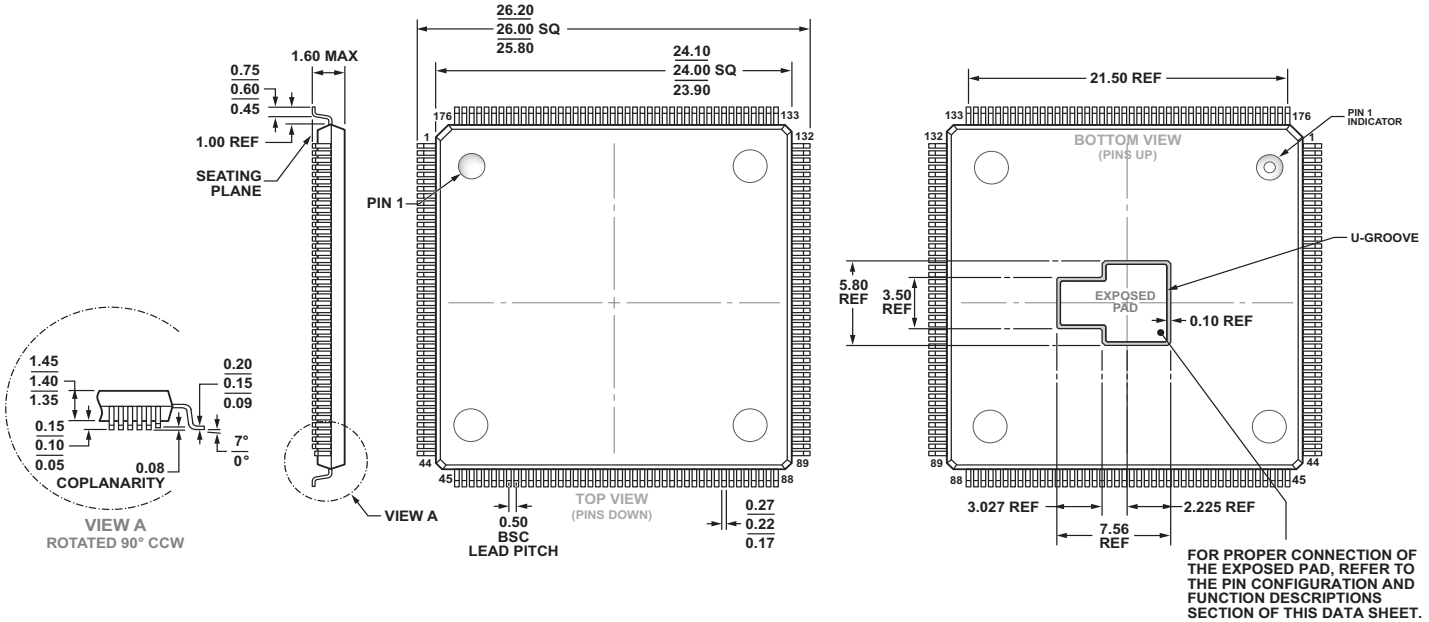

Figure 71. 176-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP][1]
(SW-176-3)
Dimensions shown in millimeters

[1] For information relating to the SW-176-3 package's exposed pad, see the table endnote in ADSP-CM407F/ADSP-CM408F 176-Lead LQFP Lead Assignments on Page 113.

ORDERING GUIDE

Model[1]	Max. Core Clock	ADC ENOB	Ethernet	Temperature Range[2]	Package Description	Package Option
ADSP-CM402CSWZ-EF	150 MHz	11+	N/A	–40°C to +105°C	120-Lead Low Profile Quad Flat Package, Exposed Pad	SW-120-3
ADSP-CM402CSWZ-FF	100 MHz	11+	N/A	–40°C to +105°C	120-Lead Low Profile Quad Flat Package, Exposed Pad	SW-120-3
ADSP-CM403CSWZ-CF	240 MHz	13+	N/A	–40°C to +105°C	120-Lead Low Profile Quad Flat Package, Exposed Pad	SW-120-3
ADSP-CM403CSWZ-EF	150 MHz	13+	N/A	–40°C to +105°C	120-Lead Low Profile Quad Flat Package, Exposed Pad	SW-120-3
ADSP-CM403CSWZ-FF	100 MHz	13+	N/A	–40°C to +105°C	120-Lead Low Profile Quad Flat Package, Exposed Pad	SW-120-3
ADSP-CM407CSWZ-AF	240 MHz	11+	1	–40°C to +105°C	176-Lead Low Profile Quad Flat Package, Exposed Pad	SW-176-3
ADSP-CM407CSWZ-BF	240 MHz	11+	N/A	–40°C to +105°C	176-Lead Low Profile Quad Flat Package, Exposed Pad	SW-176-3
ADSP-CM407CSWZ-DF	150 MHz	11+	N/A	–40°C to +105°C	176-Lead Low Profile Quad Flat Package, Exposed Pad	SW-176-3
ADSP-CM408CSWZ-AF	240 MHz	13+	1	–40°C to +105°C	176-Lead Low Profile Quad Flat Package, Exposed Pad	SW-176-3
ADSP-CM408CSWZ-BF	240 MHz	13+	N/A	–40°C to +105°C	176-Lead Low Profile Quad Flat Package, Exposed Pad	SW-176-3
ADSP-CM409CBCZ-AF	240 MHz	13+	1	–40°C to +105°C	212-Ball Chip Scale Package Ball Grid Array	BC-212-1

[1] Z = RoHS Compliant Part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. See Operating Conditions on Page 64 for the junction temperature (T_J) specification which is the only temperature specification.

D11805-0-11/15(A)