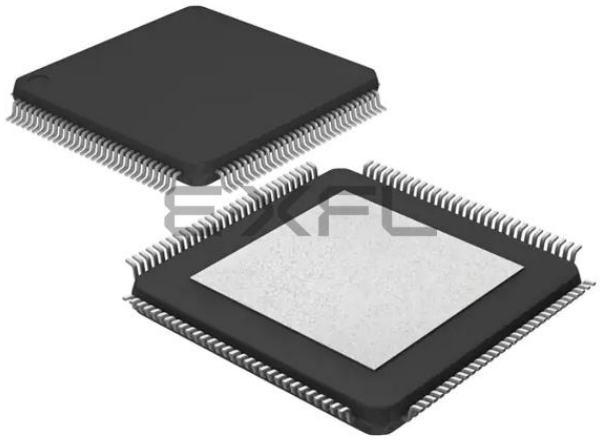

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Discontinued at Digi-Key
Type	Floating Point
Interface	CAN, Ethernet, I²C, SPI, SPORT, UART/USART, USB
Clock Rate	240MHz
Non-Volatile Memory	FLASH (2MB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP-EP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-cm408cswz-af

GENERAL DESCRIPTION

The ADSP-CM40xF family of mixed-signal control processors is based on the ARM® Cortex-M4™ processor core with floating-point unit operating at frequencies up to 240 MHz and integrating up to 384 kB of SRAM memory, 2 MB of flash memory, accelerators and peripherals optimized for motor control and photo-voltaic (PV) inverter control and an analog module consisting of two 16-bit SAR ADCs and two 12-bit DACs. The ADSP-CM40xF family operates from a single voltage supply (VDD_EXT/VDD_ANA), generating its own internal voltage supplies using internal voltage regulators and an external pass transistor.

This family of mixed-signal control processors offers low static power consumption and is produced with a low power and low voltage design methodology, delivering world class processor and ADC performance with lower power consumption.

By integrating a rich set of industry-leading system peripherals and memory (shown in Table 1), the ADSP-CM40xF mixed-signal control processors are the platform of choice for next-generation applications that require RISC programmability, advanced communications and leading-edge signal processing in one integrated package. These applications span a wide array of markets including power/motor control, embedded industrial, instrumentation, medical and consumer.

Each ADSP-CM40xF family member contains the following modules.

- 8 GP timers with PWM output
- 3-phase PWM units with up to 4 output pairs per unit
- 2 CAN modules
- 1 two-wire interface (TWI) module
- 3 UARTs
- 1 ADC controller (ADCC) to control on-chip ADCs
- 1 DAC controller (DACC) to control on-chip DACs
- 4 Sinus Cardinalis (SINC) filter pairs
- 1 harmonic analysis engine (HAE)
- 2 SPI (1 connected to internal SPI flash memory)
- 3 half-SPORTs
- 1 watchdog timer unit
- 3 capture timer units
- 1 cyclic redundancy check (CRC)

Table 1 provides the additional product features shown by model.

Table 1. ADSP-CM4 0xF Family Product Features

Generic	**ADSP-CM402F**		**ADSP-CM403F**			**ADSP-CM407F**			**ADSP-CM408F**		**ADSP-CM409F**
Package	120-Lead LQFP					176-Lead LQFP					212-Ball BGA
GPIOs	40					91					
SMC	16-Bit Asynchronous/5 Address					16-Bit Asynchronous/24 Address					
ADC ENOB (No Averaging)	11+		13+			11+			13+		
ADC Inputs	24					16					24
DAC Outputs	2					N/A					2
SPORTs	3 Half-SPORTs					4 Half-SPORTs					
Ethernet	N/A					1	N/A	N/A	1	N/A	1
USB	N/A					1	1	N/A	1	1	1
External SPI	1					2					
HAE	1										
CAN	2										
UART	3										
Feature Set Code	E	F	C	E	F	A	B	D	A	B	A
L1 SRAM (kB)	128	128	384	128	128	384	384	128	384	384	384
Flash (kB)	512	256	2048	512	256	2048	2048	1024	2048	2048	2048
Core Clock (MHz)	150	100	240	150	100	240	240	150	240	240	240
Model	ADSP-CM402CSWZ-EF	ADSP-CM402CSWZ-FF	ADSP-CM403CSWZ-CF	ADSP-CM403CSWZ-EF	ADSP-CM403CSWZ-FF	ADSP-CM407CSWZ-AF	ADSP-CM407CSWZ-BF	ADSP-CM407CSWZ-DF	ADSP-CM408CSWZ-AF	ADSP-CM408CSWZ-BF	ADSP-CM409CBCZ-AF

ANALOG FRONT END

The mixed-signal controllers contain two ADCs and two DACs. Control of these data converters is simplified by a powerful on-chip analog-to-digital conversion controller (ADCC) and a digital-to-analog conversion controller (DACC). The ADCC and DACC are integrated seamlessly into the software programming model, and they efficiently manage the configuration and real-time operation of the ADCs and DACs.

For technical details, see ADC/DAC Specifications on Page 68.

The ADCC provides the mechanism to precisely control execution of timing and analog sampling events on the ADCs. The ADCC supports two-channel (one each—ADC0, ADC1) simultaneous sampling of ADC inputs and can deliver 16 channels of ADC data to memory in 3 µs. Conversion data from the ADCs may be either routed via DMA to memory, or to a destination register via the processor. The ADCC can be configured so that the two ADCs sample and convert both analog inputs simultaneously or at different times and may be operated in asynchronous or synchronous modes. The best performance can be achieved in synchronous mode.

Likewise, the DACC interfaces to two DACs and has purpose of managing those DACs. Conversion data to the DACs may be either routed from memory through DMA, or from a source register via the processor.

Functional operation and programming for the ADCC and DACC are described in detail in the *ADSP-CM40x Mixed-Signal Control Processor with ARM Cortex-M4 Hardware Reference*.

ADC and DAC features and performance specifications differ by processor model. Simplified block diagrams of the ADCC/DACC and the ADC/DAC are shown in Figure 2 and Figure 3.

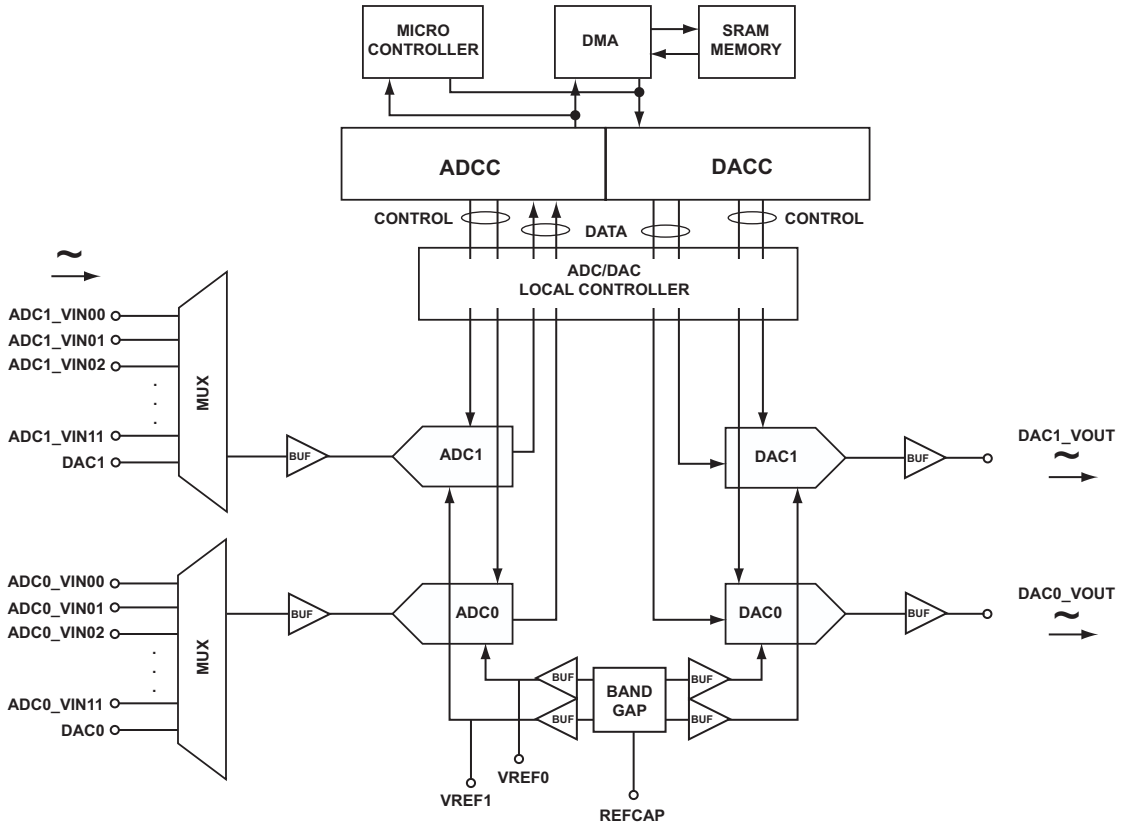


Figure 2. ADSP-CM402F/ADSP-CM403F/ADSP-CM409F Analog Front End Block Diagram

ADSP-CM402F/ADSP-CM403F 120-LEAD LQFP SIGNAL DESCRIPTIONS

The processor's pin definitions are shown in Table 7. The columns in this table provide the following information:

- Signal Name: The Signal Name column in the table includes the signal name for every pin and (where applicable) the GPIO multiplexed pin function for every pin.
- Description: The Description column in the table provides a verbose (descriptive) name for the signal.
- General-Purpose Port: The Port column in the table shows whether or not the signal is multiplexed with other signals on a general-purpose I/O port pin.
- Pin Name: The Pin Name column in the table identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).

Table 7. ADSP-CM402F/ADSP-CM403F 120-Lead LQFP Signal Descriptions

Signal Name	Description	Port	Pin Name
ADC0_VIN00	Channel 0 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN00
ADC0_VIN01	Channel 1 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN01
ADC0_VIN02	Channel 2 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN02
ADC0_VIN03	Channel 3 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN03
ADC0_VIN04	Channel 4 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN04
ADC0_VIN05	Channel 5 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN05
ADC0_VIN06	Channel 6 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN06
ADC0_VIN07	Channel 7 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN07
ADC0_VIN08	Channel 8 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN08
ADC0_VIN09	Channel 9 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN09
ADC0_VIN10	Channel 10 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN10
ADC0_VIN11	Channel 11 Single-Ended Analog Input for ADC0	Not Muxed	ADC0_VIN11
ADC1_VIN00	Channel 0 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN00
ADC1_VIN01	Channel 1 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN01
ADC1_VIN02	Channel 2 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN02
ADC1_VIN03	Channel 3 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN03
ADC1_VIN04	Channel 4 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN04
ADC1_VIN05	Channel 5 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN05
ADC1_VIN06	Channel 6 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN06
ADC1_VIN07	Channel 7 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN07
ADC1_VIN08	Channel 8 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN08
ADC1_VIN09	Channel 9 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN09
ADC1_VIN10	Channel 10 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN10
ADC1_VIN11	Channel 11 Single-Ended Analog Input for ADC1	Not Muxed	ADC1_VIN11
BYP_A0	On-chip Analog Power Regulation Bypass Filter Node for ADC0 (see recommended bypass - Figure 4 on Page 6)	Not Muxed	BYP_A0
BYP_A1	On-chip Analog Power Regulation Bypass Filter Node for ADC1 (see recommended bypass - Figure 4 on Page 6)	Not Muxed	BYP_A1
BYP_D0	On-chip Digital Power Regulation Bypass Filter Node for Analog Subsystem (see recommended bypass - Figure 4 on Page 6)	Not Muxed	BYP_D0
CAN0_RX	CAN0 Receive	B	PB_15
CAN0_TX	CAN0 Transmit	C	PC_00
CAN1_RX	CAN1 Receive	B	PB_10
CAN1_TX	CAN1 Transmit	B	PB_11
CNT0_DG	CNT0 Count Down and Gate	B	PB_02
CNT0_OUTA	CNT0 Output Divider A	B	PB_13

Table 11. ADSP-CM407F/ADSP-CM408F 176-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
CNT1_UD	CNT1 Count Up and Direction	B	PB_04
CNT1_ZM	CNT1 Count Zero Marker	B	PB_03
CNT2_DG	CNT2 Count Down and Gate	E	PE_10
CNT2_UD	CNT2 Count Up and Direction	E	PE_09
CNT2_ZM	CNT2 Count Zero Marker	E	PE_08
CNT3_DG	CNT3 Count Down and Gate	E	PE_13
CNT3_UD	CNT3 Count Up and Direction	E	PE_12
CNT3_ZM	CNT3 Count Zero Marker	E	PE_11
CPTMR0_IN0	CPTMR0 Capture Timer0 Input 0	B	PB_07
CPTMR0_IN1	CPTMR0 Capture Timer0 Input 1	B	PB_08
CPTMR0_IN2	CPTMR0 Capture Timer0 Input 2	B	PB_09
ETH0_CRS	EMAC0 Carrier Sense/RMII Receive Data Valid	E	PE_09
ETH0_MDC	EMAC0 Management Channel Clock	E	PE_11
ETH0_MDIO	EMAC0 Management Channel Serial Data	E	PE_10
ETH0_PTPAUXIN	EMAC0 PTP Auxiliary Trigger Input	E	PE_07
ETH0_PTPCLKIN	EMAC0 PTP Clock Input	E	PE_06
ETH0_PTPPPS	EMAC0 PTP Pulse-Per-Second Output	E	PE_08
ETH0_REFCLK	EMAC0 Reference Clock	E	PE_15
ETH0_RXD0	EMAC0 Receive Data 0	F	PF_00
ETH0_RXD1	EMAC0 Receive Data 1	F	PF_01
ETH0_TXD0	EMAC0 Transmit Data 0	E	PE_12
ETH0_TXD1	EMAC0 Transmit Data 1	E	PE_13
ETH0_TXEN	EMAC0 Transmit Enable	E	PE_14
GND	Digital Ground	Not Muxed	GND
GND_ANA0	Analog Ground return for VDD_ANA0 (see recommended bypass - Figure 4 on Page 6)	Not Muxed	GND_ANA0
GND_ANA1	Analog Ground return for VDD_ANA1 (see recommended bypass - Figure 4 on Page 6)	Not Muxed	GND_ANA1
GND_ANA2	Analog Ground (see recommended bypass - Figure 4 on Page 6)	Not Muxed	GND_ANA2
GND_ANA3	Analog Ground (see recommended bypass - Figure 4 on Page 6)	Not Muxed	GND_ANA3
GND_VREF0	Ground return for VREF0 (see recommended bypass filter - Figure 4 on Page 6)	Not Muxed	GND_VREF0
GND_VREF1	Ground return for VREF1 (see recommended bypass filter - Figure 4 on Page 6)	Not Muxed	GND_VREF1
JTG_TCK/SWCLK	JTAG Clock/Serial Wire Clock	Not Muxed	JTG_TCK/SWCLK
JTG_TDI	JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO/SWO	JTAG Serial Data Out/Serial Wire Trace Output	Not Muxed	JTG_TDO/SWO
JTG_TMS/SWDIO	JTAG Mode Select/Serial Wire Debug Data I/O	Not Muxed	JTG_TMS/SWDIO
$\overline{\text{JTG\_TRST}}$	JTAG Reset	Not Muxed	$\overline{\text{JTG\_TRST}}$
PA_00-PA_15	Port A Positions 0 – 15	A	PA_00 – PA_15
PB_00-PB_15	Port B Positions 0 – 15	B	PB_00 – PB_15
PC_00-PC_15	Port C Positions 0 – 15	C	PC_00 – PC_15
PD_00-PD_15	Port D Positions 0 – 15	D	PD_00 – PD_15
PE_00-PE_15	Port E Positions 0 – 15	E	PE_00 – PE_15
PF_00-PF_10	Port F Positions 0 – 10	F	PF_00 – PF_10
PWM0_AH	PWM0 Channel A High Side	A	PA_02
PWM0_AL	PWM0 Channel A Low Side	A	PA_03

ADSP-CM407F/ADSP-CM408F GPIO MULTIPLEXING FOR 176-LEAD LQFP

Table 12 through Table 17 identify the pin functions that are multiplexed on the general-purpose I/O pins of the 176-lead LQFP package.

Table 12. Signal Multiplexing for Port A (176-Lead LQFP)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PA_00	PWM0_SYNC		SPT1_ACLK		
PA_01	PWM0_TRIP0		SPT1_AFS		
PA_02	PWM0_AH		SPT1_AD0		
PA_03	PWM0_AL		SPT1_AD1		
PA_04	PWM0_BH		SPT1_BCLK		
PA_05	PWM0_BL		SPT1_BFS		
PA_06	PWM0_CH		SPT1_BD0		
PA_07	PWM0_CL	SMC0_AMS2	SPT1_BD1		
PA_08	PWM1_CH		SMC0_D00		TM0_ACLK5
PA_09	PWM1_CL		SMC0_D01		TM0_ACLK4
PA_10	PWM1_SYNC		SMC0_D02		TM0_ACLK3
PA_11	PWM1_TRIP0	UART1_CTS	SMC0_D03		TM0_ACLK2
PA_12	PWM1_AH	TM0_TMR4	SMC0_D04		
PA_13	PWM1_AL	TM0_TMR5	SMC0_D05		
PA_14	PWM1_BH	TM0_TMR6	SMC0_D06		
PA_15	PWM1_BL	TM0_TMR3	SMC0_D07		

Table 13. Signal Multiplexing for Port B (176-Lead LQFP)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PB_00	PWM0_DH	TRACE_CLK	SPT0_ACLK	SMC0_D08	CNT0_ZM
PB_01	PWM0_DL	TRACE_D00	SPT0_AFS	SMC0_D09	CNT0_UD
PB_02	PWM1_DH	TRACE_D01	SPT0_AD0	SMC0_D10	CNT0_DG
PB_03	PWM1_DL	TRACE_D02	SPT0_AD1	SMC0_D11	CNT1_ZM
PB_04	PWM2_SYNC	UART0_RTS	SPT0_ATDV	SMC0_D12	CNT1_UD
PB_05	PWM2_TRIP0	UART0_CTS	TM0_TMR7	SMC0_D13	CNT1_DG
PB_06	PWM2_AH	TM0_CLK	SPI1_SEL2	SMC0_D14	
PB_07	PWM2_AL	TM0_TMR0	SPI1_SEL3	SMC0_D15	CPTMR0_IN0
PB_08	PWM2_BH	TM0_TMR1	UART1_RX	SMC0_ARDY	TM0_ACI2/ CPTMR0_IN1
PB_09	PWM2_BL	TM0_TMR2	UART1_TX	SMC0_ARE	CPTMR0_IN2
PB_10	SINC0_CLK0	SPI0_D2	CAN1_RX	SMC0_AWE	TM0_ACI1
PB_11	SINC0_D0	SPI0_D3	CAN1_TX	SMC0_AMS0	TM0_ACLK1
PB_12	SINC0_D1	SPT0_BTDV	UART2_RX	SMC0_AOE	TM0_ACI3
PB_13	SINC0_D2	CNT0_OUTA	SPI0_SEL2	SMC0_A01	TM0_ACLK0/ SYS_DSWAKE3
PB_14	SINC0_D3	CNT0_OUTB	SPI0_SEL3	SMC0_A02	SPI0_SS/ SYS_DSWAKE2
PB_15	CAN0_RX	SPT1_ATDV	UART1_RX	SMC0_A03	TM0_ACI4

Table 14. Signal Multiplexing for Port C (176-Lead LQFP)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	CAN0_TX	SPT1_BTDV	UART1_TX	SMC0_A04	
PC_01	UART0_RX			SMC0_A05	TM0_ACI5
PC_02	UART0_TX	TRACE_D03	SPI0_RDY		
PC_03	SPI0_CLK	PWM2_CH			
PC_04	SPI0_MISO	PWM2_CL			
PC_05	SPI0_MOSI	PWM2_DH			
PC_06	SPI0_SEL1	PWM2_DL			SYS_DSWAKE0
PC_07	SINC0_CLK1	UART2_TX	UART1_RTS		SYS_DSWAKE1
PC_08		SPT0_BCLK	SMC0_D00		
PC_09		SPT0_BFS	SMC0_D01		
PC_10		SPT0_BD0	SMC0_D02		
PC_11	SMC0_AMS3	SPT0_BD1	SMC0_D03		
PC_12		SPI1_CLK	SMC0_D04		
PC_13		SPI1_MISO	SMC0_D05		
PC_14		SPI1_MOSI	SMC0_D06		
PC_15		SPI1_SEL1	SMC0_D07		SPI1_SS

Table 15. Signal Multiplexing for Port D (176-Lead LQFP)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PD_00			SMC0_D08	TM0_TMR0	
PD_01			SMC0_D09	TM0_TMR1	
PD_02			SMC0_D10	TM0_TMR2	
PD_03			SMC0_D11	TM0_TMR3	
PD_04			SMC0_D12	TM0_TMR4	
PD_05			SMC0_D13	TM0_TMR5	
PD_06			SMC0_D14	TM0_TMR6	
PD_07			SMC0_D15	TM0_TMR7	
PD_08			SMC0_A06	TM0_CLK	
PD_09			SMC0_A07	TM0_ACI5	
PD_10			SMC0_A08	TM0_ACI4	
PD_11			SMC0_A09	TM0_ACI3	
PD_12			SMC0_A10	TM0_ACI2	
PD_13			SMC0_A11	TM0_ACI1	
PD_14			SMC0_A12		
PD_15			SMC0_A13		

Table 18. ADSP-CM409F 212-Ball BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_A03	SMC0 Address 3	F	PF_07
SMC0_A04	SMC0 Address 4	C	PC_00
SMC0_A04	SMC0 Address 4	F	PF_08
SMC0_A05	SMC0 Address 5	C	PC_01
SMC0_A05	SMC0 Address 5	F	PF_09
SMC0_A06	SMC0 Address 6	D	PD_08
SMC0_A07	SMC0 Address 7	D	PD_09
SMC0_A08	SMC0 Address 8	D	PD_10
SMC0_A09	SMC0 Address 9	D	PD_11
SMC0_A10	SMC0 Address 10	D	PD_12
SMC0_A11	SMC0 Address 11	D	PD_13
SMC0_A12	SMC0 Address 12	D	PD_14
SMC0_A13	SMC0 Address 13	D	PD_15
SMC0_A14	SMC0 Address 14	E	PE_00
SMC0_A15	SMC0 Address 15	E	PE_01
SMC0_A16	SMC0 Address 16	E	PE_02
SMC0_A17	SMC0 Address 17	E	PE_03
SMC0_A18	SMC0 Address 18	E	PE_04
SMC0_A19	SMC0 Address 19	E	PE_05
SMC0_A20	SMC0 Address 20	E	PE_06
SMC0_A21	SMC0 Address 21	E	PE_07
SMC0_A22	SMC0 Address 22	E	PE_08
SMC0_A23	SMC0 Address 23	E	PE_09
SMC0_A24	SMC0 Address 24	E	PE_11
$\overline{\text{SMC0\_ABE0}}$	SMC0 Byte Enable 0	F	PF_10
$\overline{\text{SMC0\_ABE1}}$	SMC0 Byte Enable 1	F	PF_02
$\overline{\text{SMC0\_AMS0}}$	SMC0 Memory Select 0	B	PB_11
$\overline{\text{SMC0\_AMS0}}$	SMC0 Memory Select 0	Not Muxed	$\overline{\text{SMC0\_AMS0}}$
$\overline{\text{SMC0\_AMS1}}$	SMC0 Memory Select 1	E	PE_10
$\overline{\text{SMC0\_AMS2}}$	SMC0 Memory Select 2	A	PA_07
$\overline{\text{SMC0\_AMS3}}$	SMC0 Memory Select 3	C	PC_11
$\overline{\text{SMC0\_AOE}}$	SMC0 Output Enable	B	PB_12
$\overline{\text{SMC0\_AOE}}$	SMC0 Output Enable	F	PF_03
SMC0_ARDY	SMC0 Asynchronous Ready	B	PB_08
SMC0_ARDY	SMC0 Asynchronous Ready	F	PF_04
$\overline{\text{SMC0\_ARE}}$	SMC0 Read Enable	B	PB_09
$\overline{\text{SMC0\_ARE}}$	SMC0 Read Enable	Not Muxed	$\overline{\text{SMC0\_ARE}}$
$\overline{\text{SMC0\_AWE}}$	SMC0 Write Enable	B	PB_10
$\overline{\text{SMC0\_AWE}}$	SMC0 Write Enable	Not Muxed	$\overline{\text{SMC0\_AWE}}$
SMC0_D00	SMC0 Data 0	A	PA_08
SMC0_D00	SMC0 Data 0	C	PC_08
SMC0_D01	SMC0 Data 1	A	PA_09
SMC0_D01	SMC0 Data 1	C	PC_09
SMC0_D02	SMC0 Data 2	A	PA_10
SMC0_D02	SMC0 Data 2	C	PC_10
SMC0_D03	SMC0 Data 3	A	PA_11

Table 18. ADSP-CM409F 212-Ball BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
VDD_ANA0	Analog Voltage Domain (see recommended bypass - Figure 4 on Page 6)	Not Muxed	VDD_ANA0
VDD_ANA1	Analog Voltage Domain (see recommended bypass - Figure 4 on Page 6)	Not Muxed	VDD_ANA1
VDD_EXT	External Voltage Domain	Not Muxed	VDD_EXT
VDD_INT	Internal Voltage Domain	Not Muxed	VDD_INT
VDD_VREG	VREG Supply Voltage	Not Muxed	VDD_VREG
VREF0	Voltage Reference for ADC0. Default configuration is Output (see recommended bypass - Figure 4 on Page 6)	Not Muxed	VREF0
VREF1	Voltage Reference for ADC1. Default configuration is Output (see recommended bypass - Figure 4 on Page 6)	Not Muxed	VREF1
VREG_BASE	Voltage Regulator Base Node	Not Muxed	VREG_BASE

ADSP-CM409F GPIO MULTIPLEXING FOR 212-BALL BGA

Table 19 through Table 24 identify the pin functions that are multiplexed on the general-purpose I/O pins of the 212-ball BGA package.

Table 19. Signal Multiplexing for Port A (212-Ball BGA)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PA_00	PWM0_SYNC		SPT1_ACLK		
PA_01	PWM0_TRIP0		SPT1_AFS		
PA_02	PWM0_AH		SPT1_AD0		
PA_03	PWM0_AL		SPT1_AD1		
PA_04	PWM0_BH		SPT1_BCLK		
PA_05	PWM0_BL		SPT1_BFS		
PA_06	PWM0_CH		SPT1_BD0		
PA_07	PWM0_CL	SMC0_AMS2	SPT1_BD1		
PA_08	PWM1_CH		SMC0_D00		TM0_ACLK5
PA_09	PWM1_CL		SMC0_D01		TM0_ACLK4
PA_10	PWM1_SYNC		SMC0_D02		TM0_ACLK3
PA_11	PWM1_TRIP0	UART1_CTS	SMC0_D03		TM0_ACLK2
PA_12	PWM1_AH	TM0_TMR4	SMC0_D04		
PA_13	PWM1_AL	TM0_TMR5	SMC0_D05		
PA_14	PWM1_BH	TM0_TMR6	SMC0_D06		
PA_15	PWM1_BL	TM0_TMR3	SMC0_D07		

Table 20. Signal Multiplexing for Port B (212-Ball BGA)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PB_00	PWM0_DH	TRACE_CLK	SPT0_ACLK	SMC0_D08	CNT0_ZM
PB_01	PWM0_DL	TRACE_D00	SPT0_AFS	SMC0_D09	CNT0_UD
PB_02	PWM1_DH	TRACE_D01	SPT0_AD0	SMC0_D10	CNT0_DG
PB_03	PWM1_DL	TRACE_D02	SPT0_AD1	SMC0_D11	CNT1_ZM
PB_04	PWM2_SYNC	UART0_RTS	SPT0_ATDV	SMC0_D12	CNT1_UD
PB_05	PWM2_TRIP0	UART0_CTS	TM0_TMR7	SMC0_D13	CNT1_DG
PB_06	PWM2_AH	TM0_CLK	SPI1_SEL2	SMC0_D14	
PB_07	PWM2_AL	TM0_TMR0	SPI1_SEL3	SMC0_D15	CPTMR0_IN0
PB_08	PWM2_BH	TM0_TMR1	UART1_RX	SMC0_ARDY	TM0_ACI2/ CPTMR0_IN1
PB_09	PWM2_BL	TM0_TMR2	UART1_TX	SMC0_ARE	CPTMR0_IN2
PB_10	SINC0_CLK0	SPI0_D2	CAN1_RX	SMC0_AWE	TM0_ACI1
PB_11	SINC0_D0	SPI0_D3	CAN1_TX	SMC0_AMS0	TM0_ACLK1
PB_12	SINC0_D1	SPT0_BTDV	UART2_RX	SMC0_AOE	TM0_ACI3
PB_13	SINC0_D2	CNT0_OUTA	SPI0_SEL2	SMC0_A01	TM0_ACLK0/ SYS_DSWAKE3
PB_14	SINC0_D3	CNT0_OUTB	SPI0_SEL3	SMC0_A02	SPI0_SS/ SYS_DSWAKE2
PB_15	CAN0_RX	SPT1_ATDV	UART1_RX	SMC0_A03	TM0_ACI4

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
GND_ANA1	g	na	none	none	none	VDD_ANA	Desc: Analog Ground return for VDD_ANA1 (see recommended bypass - Figure 4 on Page 6) Notes: No notes.
GND_ANA2	g	na	none	none	none	VDD_ANA	Desc: Analog Ground (see recommended bypass - Figure 4 on Page 6) Notes: No notes.
GND_ANA3	g	na	none	none	none	VDD_ANA	Desc: Analog Ground (see recommended bypass - Figure 4 on Page 6) Notes: No notes.
GND_VREF0	g	na	none	none	none	VDD_ANA	Desc: Ground return for VREF0 (see recommended bypass filter - Figure 4 on Page 6) Notes: No notes.
GND_VREF1	g	na	none	none	none	VDD_ANA	Desc: Ground return for VREF1 (see recommended bypass filter - Figure 4 on Page 6) Notes: No notes.
JTG_TCK/SWCLK	I/O	na	pd	pd	none	VDD_EXT	Desc: JTAG Clock/Serial Wire Clock Notes: No notes.
JTG_TDI	I/O	na	pu	pu	none	VDD_EXT	Desc: JTAG Serial Data In Notes: No notes.
JTG_TDO/SWO	I/O	A	none	none	none	VDD_EXT	Desc: JTAG Serial Data Out/Serial Wire Trace Output Notes: No notes.
JTG_TMS/SWDIO	I/O	A	pu	pu	none	VDD_EXT	Desc: JTAG Mode Select/Serial Wire Debug Data I/O Notes: No notes.
$\overline{\text{JTG\_TRST}}$	I/O	A	pu	pu	none	VDD_EXT	Desc: JTAG Reset Notes: Requires pull-up if using TRACE functionality; otherwise pull-down should be connected.
PA_00	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 0 | PWM0 Sync | SPORT1 Channel A Clock Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_01	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 1 | PWM0 Trip Input 0 | SPORT1 Channel A Frame Sync Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_02	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 2 | PWM0 Channel A High Side | SPORT1 Channel A Data 0 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_03	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 3 | PWM0 Channel A Low Side | SPORT1 Channel A Data 1 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_04	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 4 | PWM0 Channel B High Side | SPORT1 Channel B Clock Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PA_05	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 5 | PWM0 Channel B Low Side | SPORT1 Channel B Frame Sync Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_06	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 6 | PWM0 Channel C High Side | SPORT1 Channel B Data 0 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_07	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 7 | PWM0 Channel C Low Side | SMC0 Memory Select 2 | SPORT1 Channel B Data 1 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_08	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 8 | PWM1 Channel C High Side | SMC0 Data 0 | TM0 Timer5 Alternate Clock Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_09	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 9 | PWM1 Channel C Low Side | SMC0 Data 1 | TM0 Timer4 Alternate Clock Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_10	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 10 | PWM1 Sync | SMC0 Data 2 | TM0 Timer3 Alternate Clock Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_11	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 11 | PWM1 Trip Input 0 | UART1 Clear to Send | SMC0 Data 3 | TM0 Timer2 Alternate Clock Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_12	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 12 | PWM1 Channel A High Side | TM0 Timer 4 | SMC0 Data 4 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_13	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 13 | PWM1 Channel A Low Side | TM0 Timer 5 | SMC0 Data 5 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PA_14	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 14 | PWM1 Channel B High Side | TM0 Timer 6 | SMC0 Data 6 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PC_01	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PC Position 1 | UART0 Receive | SMC0 Address 5 | TM0 Timer5 Alternate Capture Input Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PC_02	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PC Position 2 | UART0 Transmit | Embedded Trace Module Data 3 | SPI0 Ready Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PC_03	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PC Position 3 | SPI0 Clock | PWM2 Channel C High Side Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PC_04	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PC Position 4 | SPI0 Master In, Slave Out | PWM2 Channel C Low Side Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PC_05	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PC Position 5 | SPI0 Master Out, Slave In | PWM2 Channel D High Side Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PC_06	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PC Position 6 | SPI0 Slave Select Output 1 | PWM2 Channel D Low Side | SYS0 Deep Sleep Wakeup 0 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PC_07	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PC Position 7 | SINC0 Clock 1 | UART2 Transmit | UART1 Request to Send | SYS0 Deep Sleep Wakeup 1 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PC_08	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PC Position 8 | SPORT0 Channel B Clock | SMC0 Data 0 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PC_09	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PC Position 9 | SPORT0 Channel B Frame Sync | SMC0 Data 1 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PC_10	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PC Position 10 | SPORT0 Channel B Data 0 | SMC0 Data 2 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PC_11	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PC Position 11 | SMC0 Memory Select 3 | SPT0 Channel B Data 1 | SMC0 Data 3 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
USB0_ID	I/O	na	none	none	none	VDD_EXT	Desc: USB0 OTG ID Notes: If USB is not used, connect to ground.
USB0_VBUS	I/O	E	none	none	none	VDD_EXT	Desc: USB0 Bus Voltage Notes: If USB is not used, pull low.
VDD_ANA0	s	na	none	none	none	na	Desc: Analog Power Supply Voltage 3.13 V to 3.47 V (see recommended bypass - Figure 4 on Page 6) Notes: No notes.
VDD_ANA1	s	na	none	none	none	na	Desc: Analog Power Supply Voltage 3.13 V to 3.47 V (see recommended bypass - Figure 4 on Page 6) Notes: No notes.
VDD_EXT	s	na	none	none	none	na	Desc: External Voltage Domain Notes: No notes.
VDD_INT	s	na	none	none	none	na	Desc: Internal Voltage Domain Notes: No notes.
VDD_VREG	s	na	none	none	none	na	Desc: VREG Supply Voltage Notes: No notes.
VREF0	a	na	none	none	none	na	Desc: Voltage Reference for ADC0. Default configuration is Output (see recommended bypass - Figure 4 on Page 6) Notes: When using internal ADC reference, this pin should never be loaded with resistive or inductive load or connected to anything but the recommended capacitor. When using external ADC reference, connect to externally generated reference voltage supply
VREF1	a	na	none	none	none	na	Desc: Voltage Reference for ADC1. Default configuration is Output (see recommended bypass - Figure 4 on Page 6) Notes: When using internal ADC reference, this pin should never be loaded with resistive or inductive load or connected to anything but the recommended capacitor. When using external ADC reference, connect to externally generated reference voltage supply
VREG_BASE	a	na	none	none	none	na	Desc: Voltage Regulator Base Node Notes: When unused, connect to GND or pull low

DAC Typical Performance Characteristics

V_{DD_ANA} = 3.3 V, V_{REF} = 2.5 V, T_J = 25°C, unless otherwise noted.

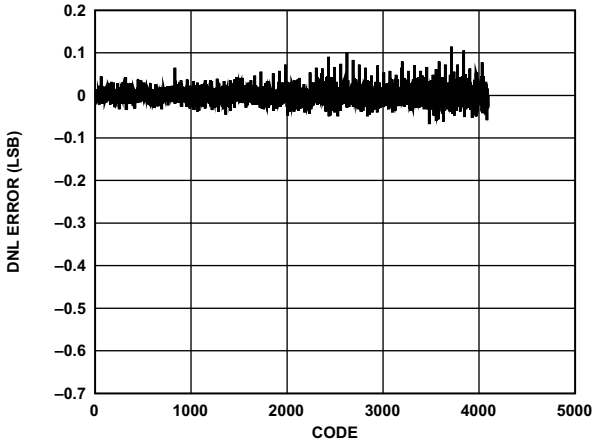


Figure 21. DAC DNL Error vs. Code

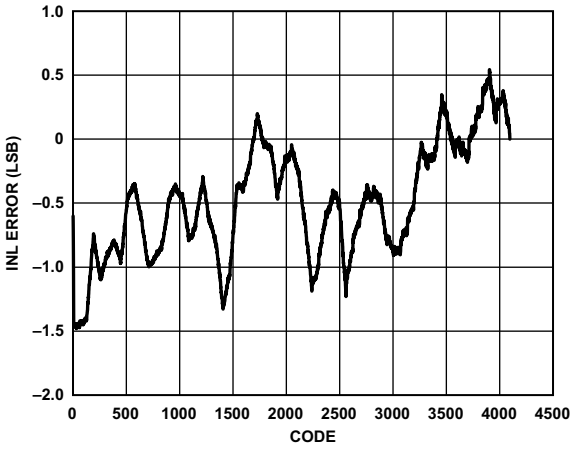


Figure 22. DAC INL Error vs. Code

Asynchronous Flash Write

Table 40 and Figure 30 show asynchronous flash memory write timing, related to the static memory controller (SMC).

Table 40. Asynchronous Flash Write

Parameter		Min	Max	Unit
Switching Characteristics				
t_{AMSADV}	SMC0_Ax/$\overline{\text{SMC0\_AMSx}}$ Assertion Before $\overline{\text{SMC0\_AOE}}$ Low[1]		PREST × t_{SCLK} – 2	ns
$t_{DADVAWE}$	$\overline{\text{SMC0\_AWE}}$ Low Delay From $\overline{\text{SMC0\_AOE}}$ High[2]		PREAT × t_{SCLK} – 6.2	ns
t_{WADV}	$\overline{\text{SMC0\_AOE}}$ Active Low Width[3]		WST × t_{SCLK} – 3	ns
t_{HAWE}	Output[4] Hold After $\overline{\text{SMC0\_AWE}}$ High[5]		WHT × t_{SCLK} – 2	ns
t_{WAWE}[6]	$\overline{\text{SMC0\_AWE}}$ Active Low Width[7]		WAT × t_{SCLK} – 2	ns

[1] PREST value set using the SMC_BxETIM.PREST bits.
[2] PREAT value set using the SMC_BxETIM.PREAT bits.
[3] WST value set using the SMC_BxTIM.WST bits.
[4] Output signals are DATA, SMC0_Ax, $\overline{\text{SMC0\_AMSx}}$.
[5] WHT value set using the SMC_BxTIM.WHT bits.
[6] SMC_BxCTL.ARDYEN bit = 0.
[7] WAT value set using the SMC_BxTIM.WAT bits.

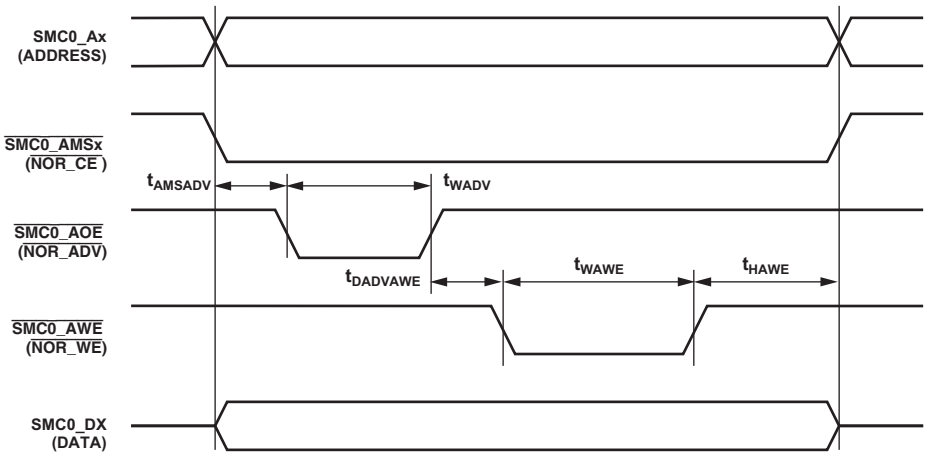


Figure 30. Asynchronous Flash Write

All Accesses

Table 41 describes timing that applies to all memory accesses, related to the static memory controller (SMC).

Table 41. All Accesses

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TURN}	$\overline{\text{SMC0\_AMSx}}$ Inactive Width	(IT + TT) × t_{SCLK} – 2		ns

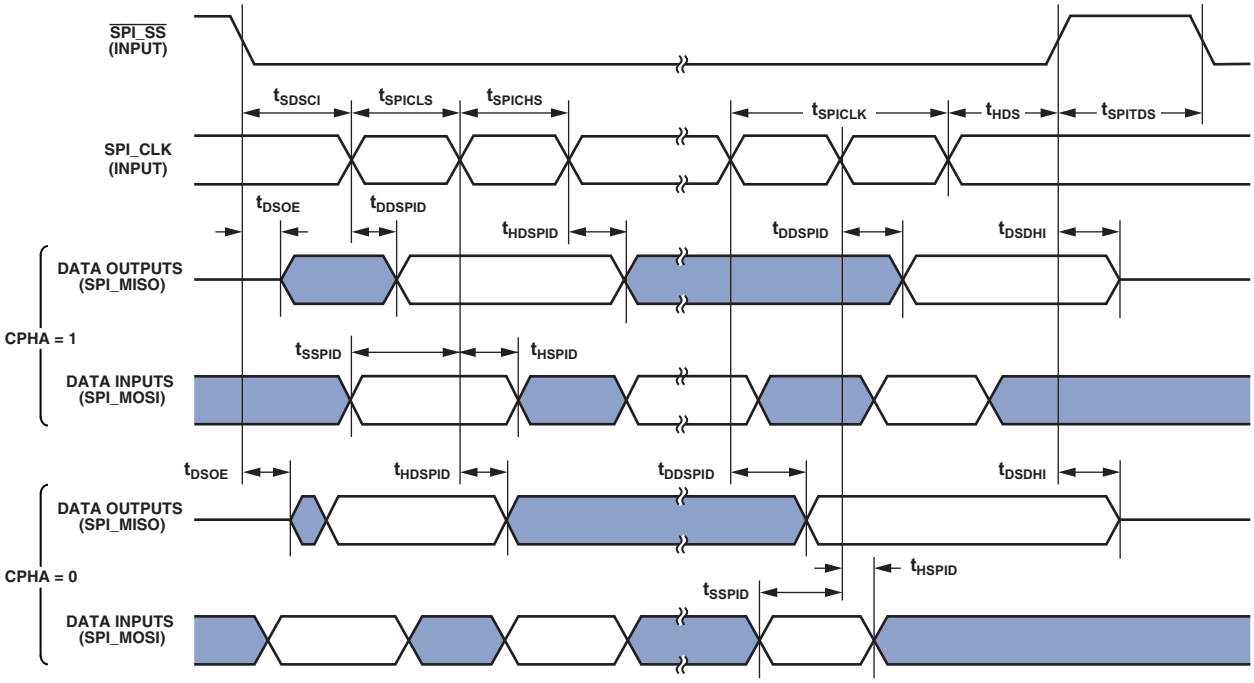
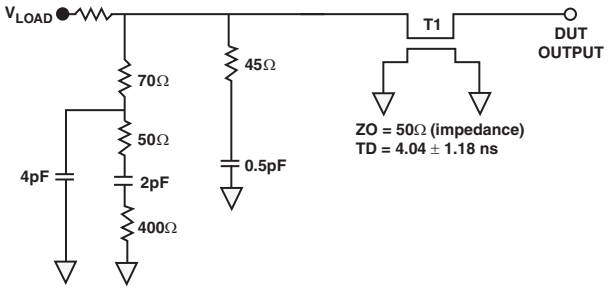


Figure 36. Serial Peripheral Interface (SPI) Port—Slave Timing



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD), IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 63. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

The graph of Figure 64 shows how output rise and fall times vary with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.

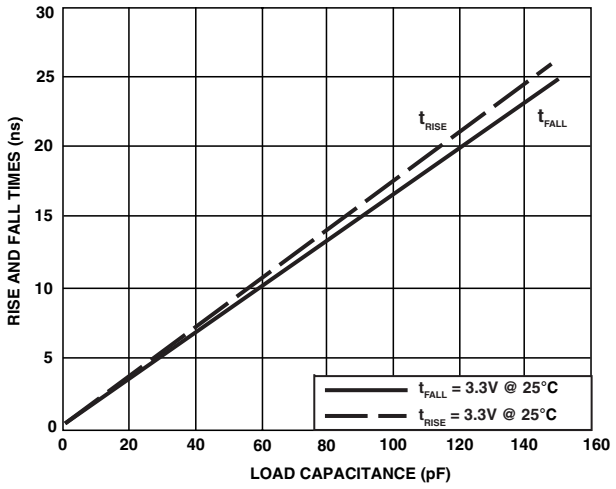


Figure 64. Driver Type A Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application printed circuit board, use the following equation:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C).

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 68, Table 69, and Table 70.

P_D = Power dissipation (see Total Power Dissipation (PD) on Page 67 for the method to calculate P_D).

Table 68. Thermal Characteristics (120-Lead LQFP)

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	21.5	°C/W
θ_{JA}	1 linear m/s air flow	19.2	°C/W
θ_{JA}	2 linear m/s air flow	18.4	°C/W
θ_{JC}		9.29	°C/W
Ψ_{JT}	0 linear m/s air flow	0.25	°C/W
Ψ_{JT}	1 linear m/s air flow	0.40	°C/W
Ψ_{JT}	2 linear m/s air flow	0.56	°C/W

Table 69. Thermal Characteristics (176-Lead LQFP)

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	21.5	°C/W
θ_{JA}	1 linear m/s air flow	19.3	°C/W
θ_{JA}	2 linear m/s air flow	18.5	°C/W
θ_{JC}		9.24	°C/W
Ψ_{JT}	0 linear m/s air flow	0.25	°C/W
Ψ_{JT}	1 linear m/s air flow	0.37	°C/W
Ψ_{JT}	2 linear m/s air flow	0.48	°C/W

Table 70. Thermal Characteristics (212-Ball BGA)

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	30.0	°C/W
θ_{JA}	1 linear m/s air flow	27.5	°C/W
θ_{JA}	2 linear m/s air flow	26.5	°C/W
θ_{JC}		9.2	°C/W
Ψ_{JT}	0 linear m/s air flow	0.15	°C/W
Ψ_{JT}	1 linear m/s air flow	0.24	°C/W
Ψ_{JT}	2 linear m/s air flow	0.27	°C/W

Table 75. ADSP-CM409F 212-Ball BGA Ball Assignments (Numerical by Ball Number) (Continued)

Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name
C07	PD_05	J02	PA_02	R08	VDD_INT	V11	PE_13
C08	PB_04	J03	VDD_VREG	R09	VDD_EXT	V12	PB_14
C09	PB_07	J07	GND	R10	VDD_INT	V13	PE_12
C10	PB_10	J08	GND	R11	GND	V14	PE_10
C11	PD_06	J09	GND	R12	BYP_D0	V15	PE_07
C12	PD_09	J11	GND_ANA	R16	DAC1_VOUT	V16	PE_05
C13	PD_13	J12	GND_ANA	R17	ADC1_VIN02	V17	PE_04
C14	GND	J16	GND_ANA	R18	ADC1_VIN04	V18	GND_ANA
C15	VDD_EXT	J17	GND_ANA	T01	JTG_TDI		
C16	GND_ANA	J18	VDD_ANA0	T02	JTG_TCK/SWCLK		
C17	ADC0_VIN01	K01	PA_01	T03	GND		
C18	ADC0_VIN02	K02	$\overline{\text{SYS\_HWRST}}$	T04	VDD_EXT		

Table 76. ADSP-CM409F 212-Ball BGA Ball Assignments (Alphabetical by Ball Name)

Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.
ADC0_VIN00	B18	GND_ANA	H12	PB_15	T11	PF_05	T07
ADC0_VIN01	C17	GND_ANA	H18	PC_00	V08	PF_06	T06
ADC0_VIN02	C18	GND_ANA	J11	PC_01	T08	PF_07	V07
ADC0_VIN03	D17	GND_ANA	J12	PC_02	U08	PF_08	V06
ADC0_VIN04	D18	GND_ANA	J16	PC_03	U07	PF_09	U06
ADC0_VIN05	E17	GND_ANA	J17	PC_04	V05	PF_10	U05
ADC0_VIN06	E18	GND_ANA	K11	PC_05	U04	REFCAP	K16
ADC0_VIN07	F17	GND_ANA	K12	PC_06	V04	$\overline{\text{SMC0\_AMS0}}$	A10
ADC0_VIN08	F18	GND_ANA	K17	PC_07	V03	$\overline{\text{SMC0\_ARE}}$	B10
ADC0_VIN09	G18	GND_ANA	L11	PC_08	P03	$\overline{\text{SMC0\_AWE}}$	A11
ADC0_VIN10	G17	GND_ANA	L12	PC_09	R03	SYS_BMODE0	C02
ADC0_VIN11	H17	GND_ANA	L18	PC_10	N03	SYS_BMODE1	B01
ADC1_VIN00	U18	GND_ANA	N16	PC_11	F03	SYS_CLKIN	M02
ADC1_VIN01	T17	GND_ANA	T16	PC_12	F02	SYS_CLKOUT	B03
ADC1_VIN02	R17	GND_ANA	U17	PC_13	E02	$\overline{\text{SYS\_FAULT}}$	L01
ADC1_VIN03	T18	GND_ANA	V18	PC_14	E01	$\overline{\text{SYS\_HWRST}}$	K02
ADC1_VIN04	R18	GND_VREF0	G16	PC_15	C01	$\overline{\text{SYS\_NMI}}$	B15
ADC1_VIN05	P17	GND_VREF1	M16	PD_00	A04	$\overline{\text{SYS\_RESOUT}}$	L02
ADC1_VIN06	P18	JTG_TCK/SWCLK	T02	PD_01	C06	SYS_XTAL	M01
ADC1_VIN07	N17	JTG_TDI	T01	PD_02	A05	TWI0_SCL	R02
ADC1_VIN08	N18	JTG_TDO/SWO	U03	PD_03	A06	TWI0_SDA	R01
ADC1_VIN09	M18	JTG_TMS/SWDIO	V02	PD_04	B06	USB0_DM	N01
ADC1_VIN10	M17	$\overline{\text{JTG\_TRST}}$	U01	PD_05	C07	USB0_DP	P01
ADC1_VIN11	L17	PA_00	M03	PD_06	C11	USB0_ID	P02
BYP_A0	E16	PA_01	K01	PD_07	B11	USB0_VBUS	N02
BYP_A1	P16	PA_02	J02	PD_08	A12	VDD_ANA0	J18
BYP_D0	R12	PA_03	J01	PD_09	C12	VDD_ANA1	K18
DAC0_VOUT	D16	PA_04	H02	PD_10	A13	VDD_EXT	C04
DAC1_VOUT	R16	PA_05	H01	PD_11	B12	VDD_EXT	C05
GND	A01	PA_06	G02	PD_12	B13	VDD_EXT	C15

Figure 69 shows an overview of signal placement on the 212-ball CSP_BGA package.

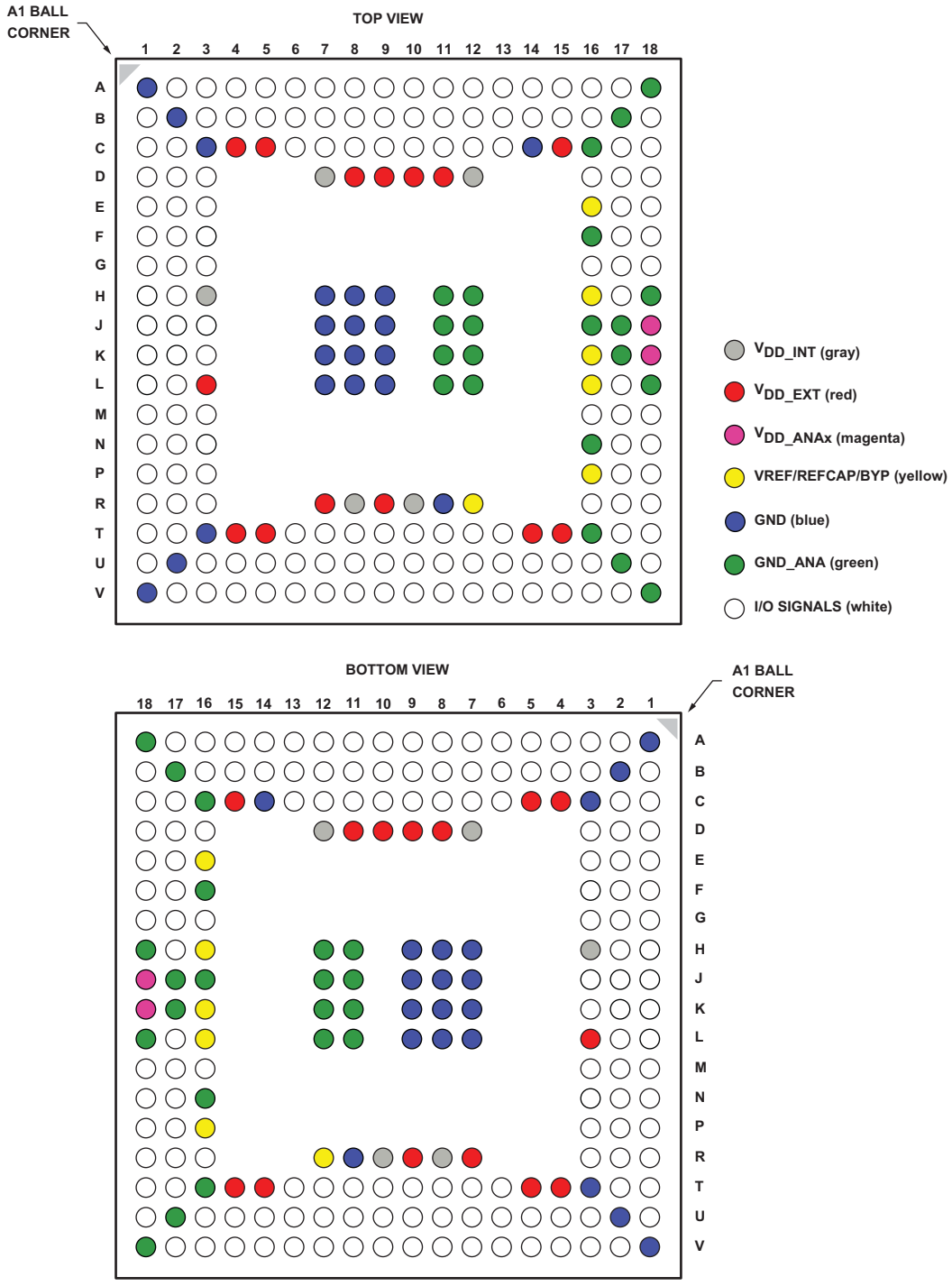


Figure 69. 212-Ball CSP_BGA Ball Configuration

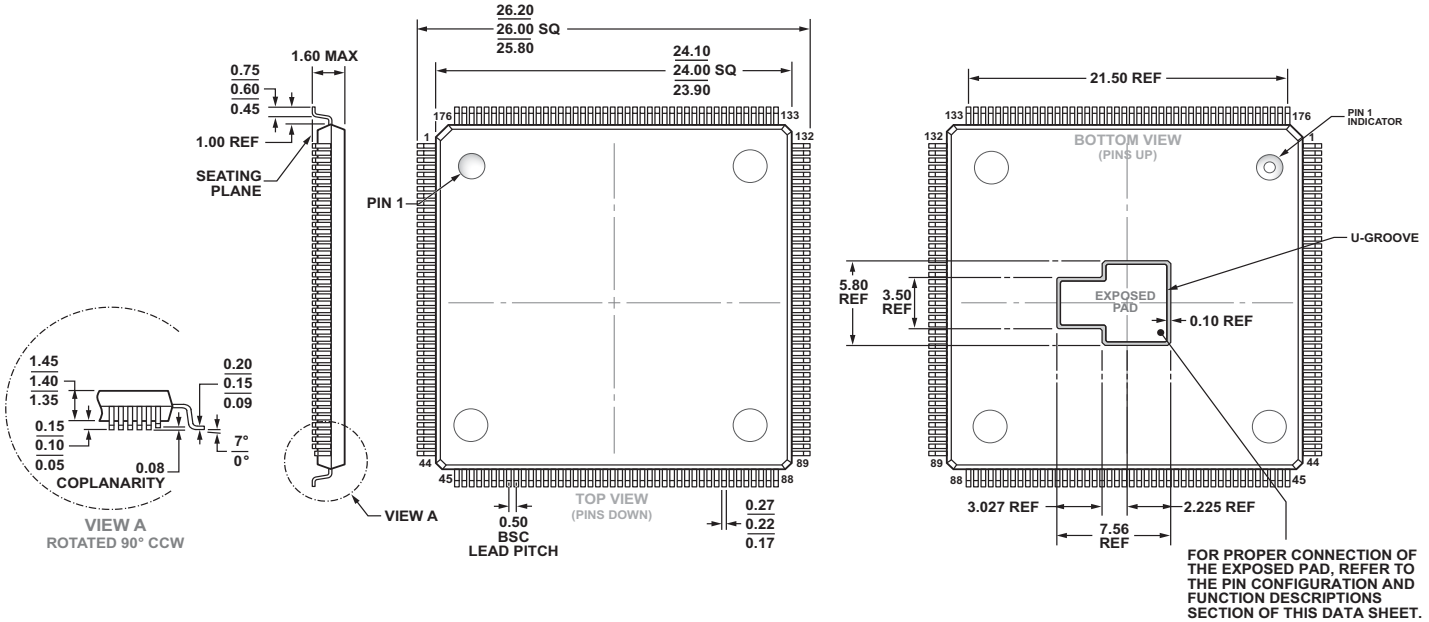


Figure 71. 176-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP][1]
(SW-176-3)
Dimensions shown in millimeters

[1] For information relating to the SW-176-3 package's exposed pad, see the table endnote in ADSP-CM407F/ADSP-CM408F 176-Lead LQFP Lead Assignments on Page 113.