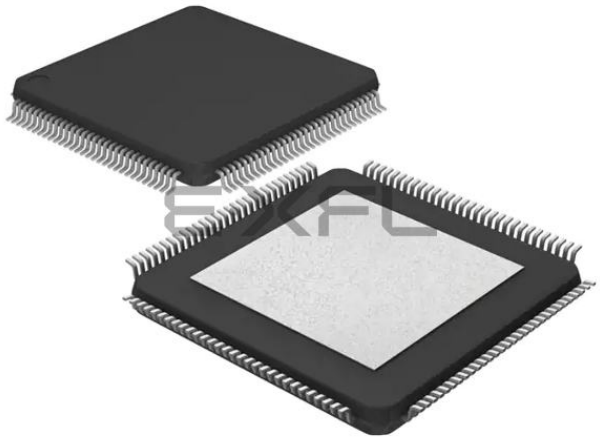

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, I²C, SPI, SPORT, UART/USART, USB
Clock Rate	240MHz
Non-Volatile Memory	FLASH (2MB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP-EP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-cm408cswz-bf

ANALOG FRONT END

The mixed-signal controllers contain two ADCs and two DACs. Control of these data converters is simplified by a powerful on-chip analog-to-digital conversion controller (ADCC) and a digital-to-analog conversion controller (DACC). The ADCC and DACC are integrated seamlessly into the software programming model, and they efficiently manage the configuration and real-time operation of the ADCs and DACs.

For technical details, see ADC/DAC Specifications on Page 68.

The ADCC provides the mechanism to precisely control execution of timing and analog sampling events on the ADCs. The ADCC supports two-channel (one each—ADC0, ADC1) simultaneous sampling of ADC inputs and can deliver 16 channels of ADC data to memory in 3 µs. Conversion data from the ADCs may be either routed via DMA to memory, or to a destination register via the processor. The ADCC can be configured so that the two ADCs sample and convert both analog inputs simultaneously or at different times and may be operated in asynchronous or synchronous modes. The best performance can be achieved in synchronous mode.

Likewise, the DACC interfaces to two DACs and has purpose of managing those DACs. Conversion data to the DACs may be either routed from memory through DMA, or from a source register via the processor.

Functional operation and programming for the ADCC and DACC are described in detail in the *ADSP-CM40x Mixed-Signal Control Processor with ARM Cortex-M4 Hardware Reference*.

ADC and DAC features and performance specifications differ by processor model. Simplified block diagrams of the ADCC/DACC and the ADC/DAC are shown in Figure 2 and Figure 3.

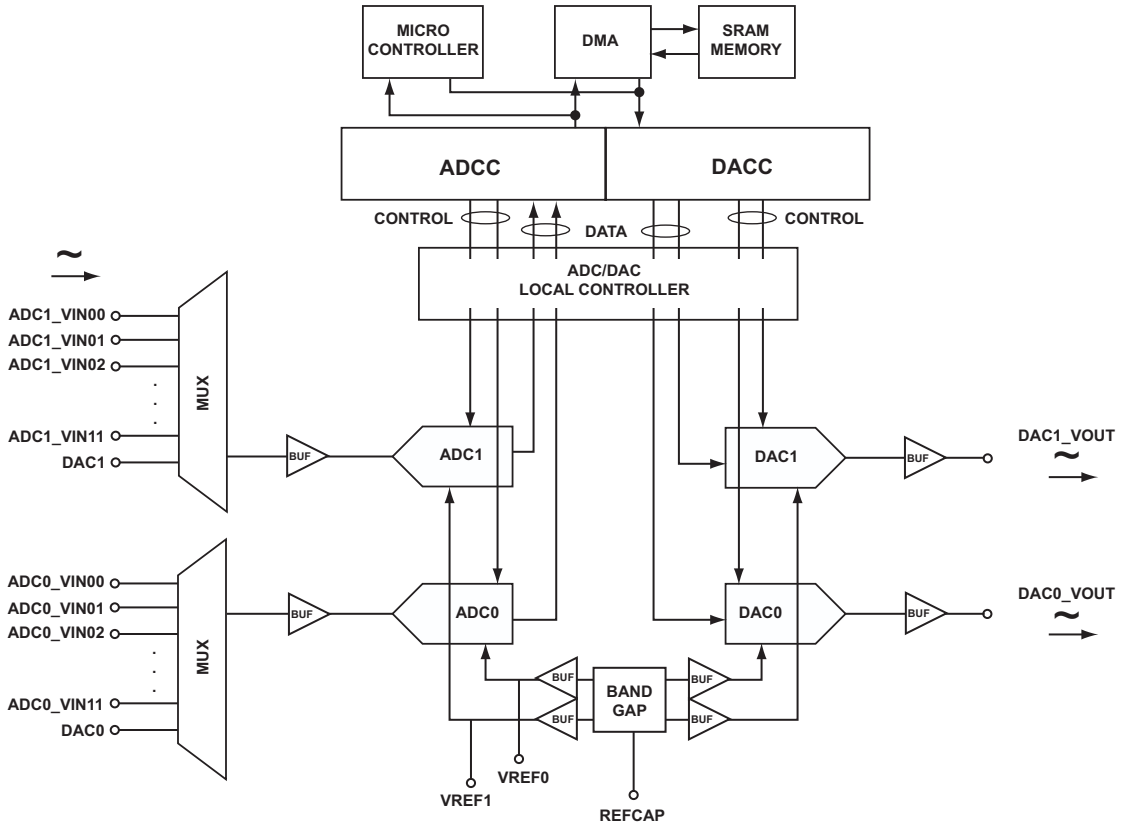


Figure 2. ADSP-CM402F/ADSP-CM403F/ADSP-CM409F Analog Front End Block Diagram

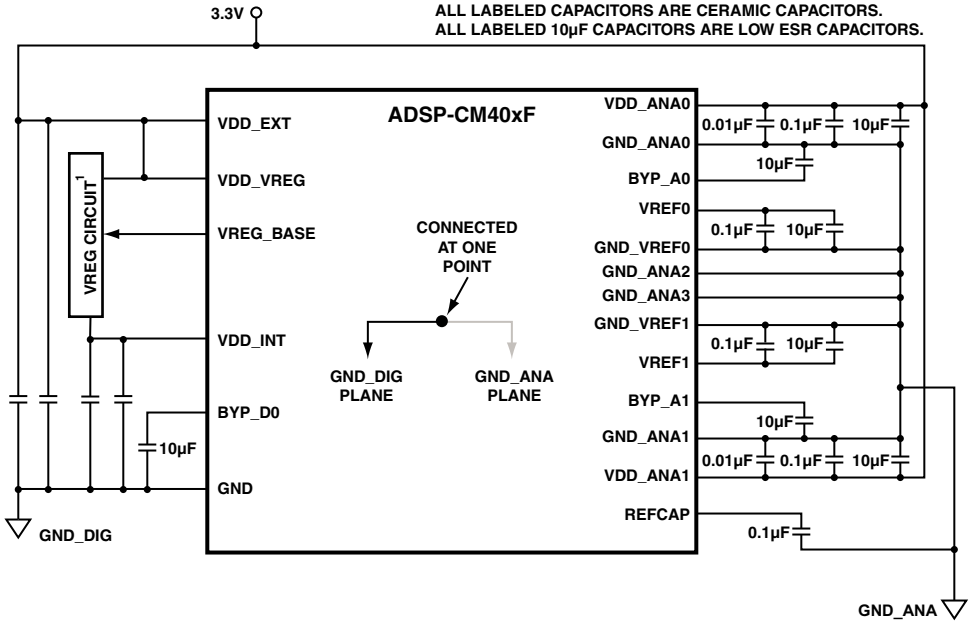


Figure 4. Typical Power Supply Configuration

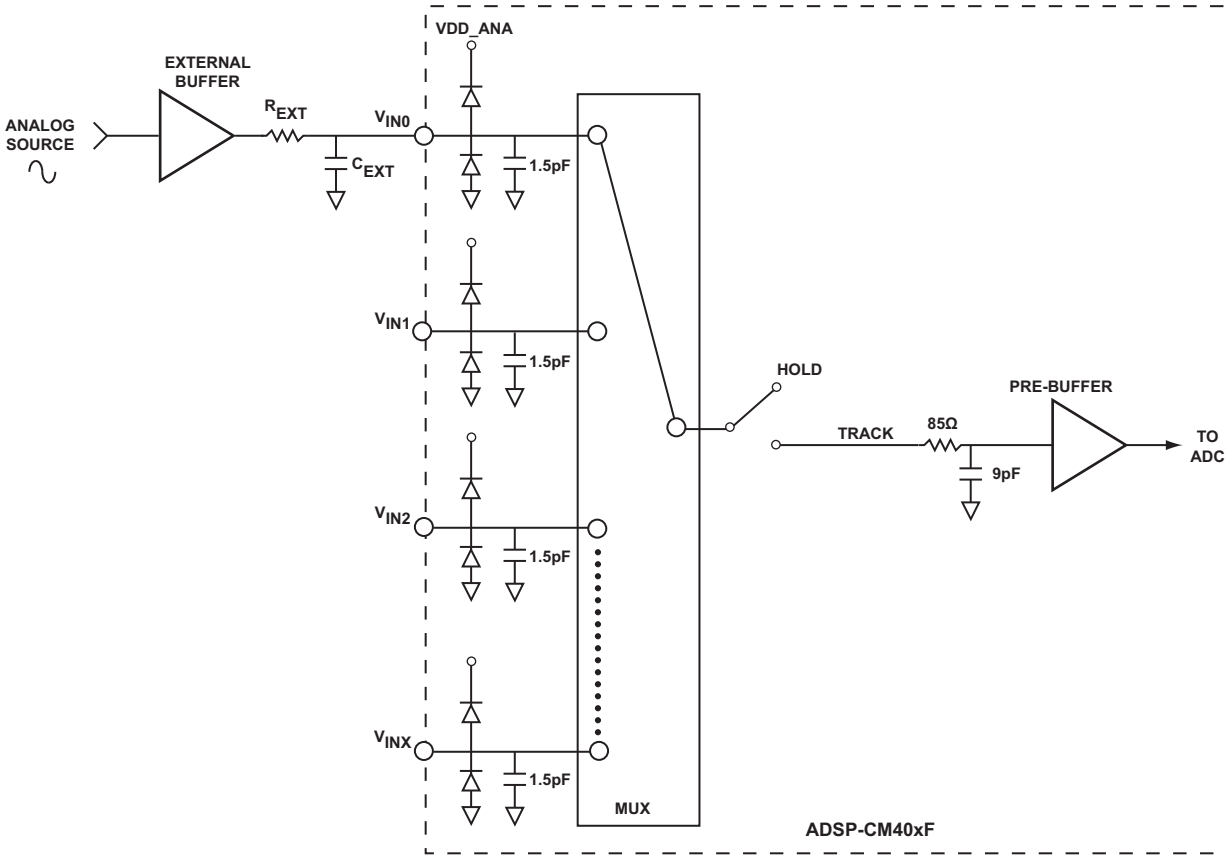


Figure 5. Equivalent Single-Ended Input (Simplified)

ARM CORTEX-M4 CORE

The ARM Cortex-M4, core shown in Figure 6, is a 32-bit reduced instruction set computer (RISC). It uses 32-bit buses for instruction and data. The length of the data can be 8 bits, 16 bits, or 32 bits. The length of the instruction word is 16 or 32 bits. The controller has the following features.

Cortex-M4 Architecture

- Thumb-2 ISA technology
- DSP and SIMD extensions
- Single cycle MAC (Up to 32 × 32 + 64 → 64)
- Hardware divide instructions
- Single-precision FPU
- NVIC interrupt controller (129 interrupts and 16 priorities)
- Memory protection unit (MPU)
- Full CoreSight™ debug, trace, breakpoints, watchpoints, and cross-triggers

Microarchitecture

- 3-stage pipeline with branch speculation
- Low-latency interrupt processing with tail chaining

Configurable For Ultra Low Power

- Deep sleep mode, dynamic power management
- Programmable clock generator unit

EmbeddedICE

EmbeddedICE™ provides integrated on-chip support for the core. The EmbeddedICE module contains the breakpoint and watchpoint registers that allow code to be halted for debugging purposes. These registers are controlled through the JTAG test port.

When a breakpoint or watchpoint is encountered, the processor halts and enters debug state. Once in a debug state, the processor registers can be inspected as well as the Flash/EE, SRAM, and memory-mapped registers.

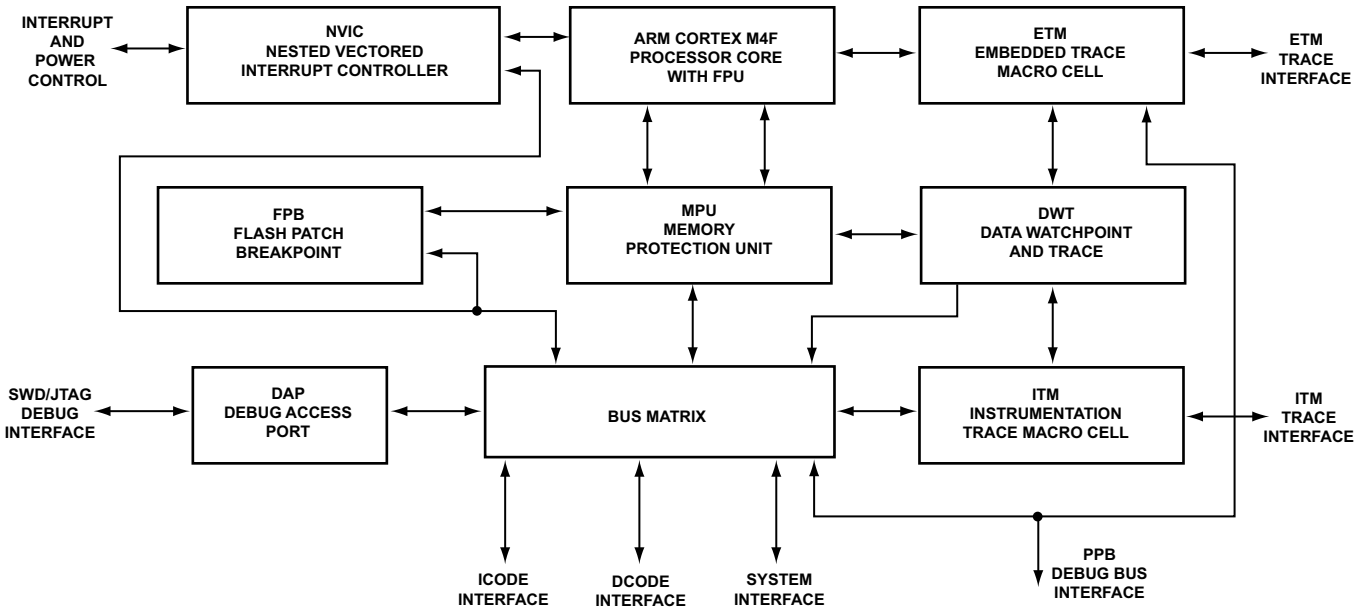


Figure 6. Cortex-M4 Block Diagram

The timer unit can be used in conjunction with the UARTs and the CAN controller to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timer can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to external signals. Timer events can also trigger other peripherals via the TRU (for instance, to signal a fault).

Watchdog Timer (WDT)

The core includes a 32-bit timer, which may be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state, via generation of a general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error. Optionally, the fault management unit (FMU) can directly initiate the processor reset upon the watchdog expiry event.

Capture Timer (CPTMR)

The processor includes three instants of capture timers (CPTMR) to capture total on time. Each capture timer captures total on time of the input signal between two leading edges of the input trigger signal. Capture timer inputs to all the timers come from external pins and the input trigger signal comes from trigger routing unit (TRU).

The core of the timer is a 32-bit counter which is reset at leading edge of the trigger and counts when the input signal level is active. The total on time of the input signal is captured from the counter at the leading edge of the trigger pulse. Capture timer can generate data interrupts to the processor core at leading edges of trigger pulses and status interrupts to indicate counter overflow condition.

3-Phase Pulse Width Modulator Unit (PWM)

The pulse width modulator (PWM) unit provides duty cycle and phase control capabilities to a resolution of one system clock cycle (SCLK). The heightened precision PWM (HPPWM) module provides increased performance to the PWM unit by increasing its resolution by several bits, resulting in enhanced precision levels. Additional features include:

- 16-bit center-based PWM generation unit
- Programmable PWM pulse width
- Single/double update modes
- Programmable dead time and switching frequency
- Twos-complement implementation which permits smooth transition to full on and full off states
- Dedicated asynchronous PWM trip signal

The eight PWM output signals (per PWM unit) consist of four high-side drive signals and four low-side drive signals. The polarity of a generated PWM signal can be set with software, so that either active high or active low PWM patterns can be produced.

Each PWM block integrates a flexible and programmable 3-phase PWM waveform generator that can be programmed to generate the required switching patterns to drive a 3-phase voltage source inverter for ac induction motor (ACIM) or permanent magnet synchronous motor (PMSM) control. In addition, the PWM block contains special functions that considerably simplify the generation of the required PWM switching patterns for control of the electronically commutated motor (ECM) or permanent magnet synchronous motor (PMSM) control. Software can enable a special mode for switched reluctance motors (SRM).

Each PWM unit features a dedicated asynchronous trip pin which (when brought low) instantaneously places all PWM outputs in the off state.

Serial Ports (SPORTs)

The synchronous serial ports provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices, Inc., audio codecs, ADCs, and DACs. The serial ports are made up of two data lines per direction, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels.For full-duplex operation, two half SPORTs can work in conjunction with clock and frame sync signals shared internally through the SPMUX block. In some operation modes, SPORT supports gated clock.

Serial ports operate in six modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode
- Right-justified mode

General-Purpose Counters

The 32-bit counter can operate in general-purpose up/down count modes and can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumbwheels. Count direction is either controlled by a level-sensitive input pin or by two edge detectors.

A third counter input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumb wheels. All three pins have a programmable debouncing circuit.

registers with associated hardware. These four SWU match groups operate independently, but share common event (interrupt and trigger) outputs.

DEVELOPMENT TOOLS

The ADSP-CM40xF processor is supported with a set of highly sophisticated and easy-to-use development tools for embedded applications. For more information, see the Analog Devices website.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-CM40xF processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *ADSP-CM40x Mixed-Signal Control Processor with ARM Cortex-M4 Hardware Reference*
- *ADSP-CM402F/CM403F/CM407F/CM408F/CM409F Anomaly Sheet*

This data sheet describes the ARM Cortex-M4 core and memory architecture used on the ADSP-CM40xF processor, but does not provide detailed programming information for the ARM processor. For more information about programming the ARM processor, visit the ARM Infocenter web page.

The applicable documentation for programming the ARM Cortex-M4 processor include:

- *Cortex®-M4 Devices Generic User Guide*
- *CoreSight™ ETM™-M4 Technical Reference Manual*
- *Cortex®-M4 Technical Reference Manual*

RELATED SIGNAL CHAINS

A signal chain is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (http:\\www.analog.com\circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

SECURITY FEATURES DISCLAIMER

To our knowledge, the Security Features, when used in accordance with the data sheet and hardware reference manual specifications, provide a secure method of implementing code and data safeguards. However, Analog Devices does not guarantee that this technology provides absolute security. ACCORDINGLY, ANALOG DEVICES HEREBY DISCLAIMS ANY AND ALL EXPRESS AND IMPLIED WARRANTIES THAT THE SECURITY FEATURES CANNOT BE BREACHED, COMPROMISED, OR OTHERWISE CIRCUMVENTED AND IN NO EVENT SHALL ANALOG DEVICES BE LIABLE FOR ANY LOSS, DAMAGE, DESTRUCTION, OR RELEASE OF DATA, INFORMATION, PHYSICAL PROPERTY, OR INTELLECTUAL PROPERTY.

Table 6. ADSP-CM40xF Detailed Signal Description (Continued)

Signal Name	Direction	Description
SPT_AFS	I/O	**SPORT A Channel Frame Sync.** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_ATDV	Output	**SPORT A Channel Transmit Data Valid.** This signal is optional and only active when SPORT is configured in multi-channel transmit mode. It is asserted during enabled slots.
SPT_BCLK	I/O	**SPORT B Channel Clock.** Data and frame sync are driven/sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_BD0	I/O	**SPORT B Channel Data 0.** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_BD1	I/O	**SPORT B Channel Data 1.** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SPT_BFS	I/O	**SPORT B Channel Frame Sync.** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_BTDV	Output	**SPORT B Channel Transmit Data Valid.** This signal is optional and only active when SPORT is configured in multi-channel transmit mode. It is asserted during enabled slots.
SYS_BMODEn	Input	**Boot Mode Control n.** Selects the boot mode of the processor. n = 0, 1
SYS_CLKIN	Input	**Processor Clock/Crystal Input.** Connect to an external clock source or crystal.
SYS_CLKOUT	Output	**Processor Clock Output.** Outputs internal clocks. Clocks may be divided down. See the CGU chapter in the processor hardware reference for more details.
SYS_DSWAKEn	Input	**System Deep Sleep Wakeup inputs.** n = 0 to 3
$\overline{\text{SYS\_FAULT}}$	Output	**System Fault.** Indicates system fault.
$\overline{\text{SYS\_HWRST}}$	Input	**Processor Hardware Reset Control.** Resets the device when asserted.
$\overline{\text{SYS\_NMI}}$	Input	**Non-maskable Interrupt.** See the processor hardware and programming references for more details.
$\overline{\text{SYS\_RESOUT}}$	Output	**Processor Reset Output.** Indicates that the device is in the reset state.
SYS_XTAL	Output	**System Crystal Output.** Drives an external crystal. Must be left unconnected if an external clock is driving CLKIN.
TM_ACIn	Input	**GP Timer Alternate Capture Input n.** Provides an additional input for GP Timers in WIDCAP, WATCHDOG, and PININT modes. n = 0 to 5
TM_ACLKn	Input	**GP Timer Alternate Clock n.** Provides an additional time base for use by an individual timer. n = 0 to 5
TM_CLK	Input	**GP Timer Clock.** Provides an additional global time base for use by all the GP timers.
TM_TMRn	I/O	**GP Timer Timer n.** The main input/output signal for each timer. n = 0 to 7. In PWM OUT mode, output is driven on this pin. In Width capture mode, it acts as input and Timer measures width and/or period of incoming signal on this pin. In EXTCLK mode, Timer counts number of incoming signal edges on this pin.
TRACE_CLK	Output	**Embedded Trace Module Clock.** Reference clock for the Trace Unit.
TRACE_Dn	Output	**Embedded Trace Module Data n.** Output data for clocked modes and changes on both edges of TRACE_CLK. n = 0 to 3
TWI_SCL	I/O	**TWI Serial Clock.** Clock output when master, clock input when slave. Compatible with I^2C bus standard.
TWI_SDA	I/O	**TWI Serial Data.** Receives or transmits data. Compatible with I^2C bus standard.
$\overline{\text{UART\_CTS}}$	Input	**UART Clear to Send.** Input Hardware Flow control signal. Transmitter initiates the transfer only when this signal is active.
$\overline{\text{UART\_RTS}}$	Output	**UART Request to Send.** Output Hardware Flow control signal. Receiver activates this signal when it is ready to receive new transfers.
$\overline{\text{UART\_RX}}$	Input	**UART Receive.** Receive input. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
$\overline{\text{UART\_TX}}$	Output	**UART Transmit.** Transmit output. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
USB_DM	I/O	**USB Data –.** Bidirectional differential data line.
USB_DP	I/O	**USB Data +**. Bidirectional differential data line.

Table 7. ADSP-CM402F/ADSP-CM403F 120-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PWM1_DL	PWM1 Channel D Low Side	B	PB_03
PWM1_SYNC	PWM1 Sync	A	PA_10
$\overline{\text{PWM1\_TRIP0}}$	PWM1 Trip Input 0	A	PA_11
PWM2_AH	PWM2 Channel A High Side	B	PB_06
PWM2_AL	PWM2 Channel A Low Side	B	PB_07
PWM2_BH	PWM2 Channel B High Side	B	PB_08
PWM2_BL	PWM2 Channel B Low Side	B	PB_09
PWM2_CH	PWM2 Channel C High Side	C	PC_03
PWM2_CL	PWM2 Channel C Low Side	C	PC_04
PWM2_DH	PWM2 Channel D High Side	C	PC_05
PWM2_DL	PWM2 Channel D Low Side	C	PC_06
PWM2_SYNC	PWM2 Sync	B	PB_04
$\overline{\text{PWM2\_TRIP0}}$	PWM2 Trip Input 0	B	PB_05
REFCAP	Output of BandGap Generator Filter Node (see recommended bypass filter - Figure 4 on Page 6)	Not Muxed	REFCAP
SINC0_CLK0	SINC0 Clock 0	B	PB_10
SINC0_CLK1	SINC0 Clock 1	C	PC_07
SINC0_D0	SINC0 Data 0	B	PB_11
SINC0_D1	SINC0 Data 1	B	PB_12
SINC0_D2	SINC0 Data 2	B	PB_13
SINC0_D3	SINC0 Data 3	B	PB_14
SMC0_A01	SMC0 Address 1	B	PB_13
SMC0_A02	SMC0 Address 2	B	PB_14
SMC0_A03	SMC0 Address 3	B	PB_15
SMC0_A04	SMC0 Address 4	C	PC_00
SMC0_A05	SMC0 Address 5	C	PC_01
$\overline{\text{SMC0\_AMS0}}$	SMC0 Memory Select 0	B	PB_11
$\overline{\text{SMC0\_AMS2}}$	SMC0 Memory Select 2	A	PA_07
$\overline{\text{SMC0\_AOE}}$	SMC0 Output Enable	B	PB_12
SMC0_ARDY	SMC0 Asynchronous Ready	B	PB_08
$\overline{\text{SMC0\_ARE}}$	SMC0 Read Enable	B	PB_09
$\overline{\text{SMC0\_AWE}}$	SMC0 Write Enable	B	PB_10
SMC0_D00	SMC0 Data 0	A	PA_08
SMC0_D01	SMC0 Data 1	A	PA_09
SMC0_D02	SMC0 Data 2	A	PA_10
SMC0_D03	SMC0 Data 3	A	PA_11
SMC0_D04	SMC0 Data 4	A	PA_12
SMC0_D05	SMC0 Data 5	A	PA_13
SMC0_D06	SMC0 Data 6	A	PA_14
SMC0_D07	SMC0 Data 7	A	PA_15
SMC0_D08	SMC0 Data 8	B	PB_00
SMC0_D09	SMC0 Data 9	B	PB_01
SMC0_D10	SMC0 Data 10	B	PB_02
SMC0_D11	SMC0 Data 11	B	PB_03
SMC0_D12	SMC0 Data 12	B	PB_04
SMC0_D13	SMC0 Data 13	B	PB_05

Table 10. Signal Multiplexing for Port C (120-Lead LQFP)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	CAN0_TX	SPT1_BTDV	UART1_TX	SMC0_A04	
PC_01	UART0_RX			SMC0_A05	TM0_ACI5
PC_02	UART0_TX	TRACE_D03	SPI0_RDY		
PC_03	SPI0_CLK	PWM2_CH			
PC_04	SPI0_MISO	PWM2_CL			
PC_05	SPI0_MOSI	PWM2_DH			
PC_06	SPI0_SEL1	PWM2_DL			SYS_DSWAKE0
PC_07	SINC0_CLK1	UART2_TX	UART1_RTS		SYS_DSWAKE1

Table 14. Signal Multiplexing for Port C (176-Lead LQFP)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	CAN0_TX	SPT1_BTDV	UART1_TX	SMC0_A04	
PC_01	UART0_RX			SMC0_A05	TM0_ACI5
PC_02	UART0_TX	TRACE_D03	SPI0_RDY		
PC_03	SPI0_CLK	PWM2_CH			
PC_04	SPI0_MISO	PWM2_CL			
PC_05	SPI0_MOSI	PWM2_DH			
PC_06	SPI0_SEL1	PWM2_DL			SYS_DSWAKE0
PC_07	SINC0_CLK1	UART2_TX	UART1_RTS		SYS_DSWAKE1
PC_08		SPT0_BCLK	SMC0_D00		
PC_09		SPT0_BFS	SMC0_D01		
PC_10		SPT0_BD0	SMC0_D02		
PC_11	SMC0_AMS3	SPT0_BD1	SMC0_D03		
PC_12		SPI1_CLK	SMC0_D04		
PC_13		SPI1_MISO	SMC0_D05		
PC_14		SPI1_MOSI	SMC0_D06		
PC_15		SPI1_SEL1	SMC0_D07		SPI1_SS

Table 15. Signal Multiplexing for Port D (176-Lead LQFP)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PD_00			SMC0_D08	TM0_TMR0	
PD_01			SMC0_D09	TM0_TMR1	
PD_02			SMC0_D10	TM0_TMR2	
PD_03			SMC0_D11	TM0_TMR3	
PD_04			SMC0_D12	TM0_TMR4	
PD_05			SMC0_D13	TM0_TMR5	
PD_06			SMC0_D14	TM0_TMR6	
PD_07			SMC0_D15	TM0_TMR7	
PD_08			SMC0_A06	TM0_CLK	
PD_09			SMC0_A07	TM0_ACI5	
PD_10			SMC0_A08	TM0_ACI4	
PD_11			SMC0_A09	TM0_ACI3	
PD_12			SMC0_A10	TM0_ACI2	
PD_13			SMC0_A11	TM0_ACI1	
PD_14			SMC0_A12		
PD_15			SMC0_A13		

Table 18. ADSP-CM409F 212-Ball BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
TM0_ACLK3	TIMER0 Alternate Clock 3	A	PA_10
TM0_ACLK4	TIMER0 Alternate Clock 4	A	PA_09
TM0_ACLK5	TIMER0 Alternate Clock 5	A	PA_08
TM0_CLK	TIMER0 Clock	B	PB_06
TM0_CLK	TIMER0 Clock	D	PD_08
TM0_TMR0	TIMER0 Timer 0	B	PB_07
TM0_TMR0	TIMER0 Timer 0	D	PD_00
TM0_TMR1	TIMER0 Timer 1	B	PB_08
TM0_TMR1	TIMER0 Timer 1	D	PD_01
TM0_TMR2	TIMER0 Timer 2	B	PB_09
TM0_TMR2	TIMER0 Timer 2	D	PD_02
TM0_TMR3	TIMER0 Timer 3	A	PA_15
TM0_TMR3	TIMER0 Timer 3	D	PD_03
TM0_TMR4	TIMER0 Timer 4	A	PA_12
TM0_TMR4	TIMER0 Timer 4	D	PD_04
TM0_TMR5	TIMER0 Timer 5	A	PA_13
TM0_TMR5	TIMER0 Timer 5	D	PD_05
TM0_TMR6	TIMER0 Timer 6	A	PA_14
TM0_TMR6	TIMER0 Timer 6	D	PD_06
TM0_TMR7	TIMER0 Timer 7	B	PB_05
TM0_TMR7	TIMER0 Timer 7	D	PD_07
TRACE_CLK	Embedded Trace Module Clock	B	PB_00
TRACE_D00	Embedded Trace Module Data 0	B	PB_01
TRACE_D01	Embedded Trace Module Data 1	B	PB_02
TRACE_D02	Embedded Trace Module Data 2	B	PB_03
TRACE_D03	Embedded Trace Module Data 3	C	PC_02
TRACE_D03	Embedded Trace Module Data 3	F	PF_02
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	B	PB_05
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	B	PB_04
$\overline{\text{UART0\_RX}}$	UART0 Receive	C	PC_01
$\overline{\text{UART0\_TX}}$	UART0 Transmit	C	PC_02
$\overline{\text{UART1\_CTS}}$	UART1 Clear to Send	A	PA_11
$\overline{\text{UART1\_RTS}}$	UART1 Request to Send	C	PC_07
$\overline{\text{UART1\_RX}}$	UART1 Receive	B	PB_08
$\overline{\text{UART1\_RX}}$	UART1 Receive	B	PB_15
$\overline{\text{UART1\_TX}}$	UART1 Transmit	B	PB_09
$\overline{\text{UART1\_TX}}$	UART1 Transmit	C	PC_00
$\overline{\text{UART2\_RX}}$	UART2 Receive	B	PB_12
$\overline{\text{UART2\_TX}}$	UART2 Transmit	C	PC_07
USB0_DM	USB0 Data –	Not Muxed	USB0_DM
USB0_DP	USB0 Data +	Not Muxed	USB0_DP
USB0_ID	USB0 OTG ID	Not Muxed	USB0_ID
USB0_VBC	USB0 VBUS Control	F	PF_02
USB0_VBUS	USB0 Bus Voltage	Not Muxed	USB0_VBUS

Table 21. Signal Multiplexing for Port C (212-Ball BGA)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	CAN0_TX	SPT1_BTDV	UART1_TX	SMC0_A04	
PC_01	UART0_RX			SMC0_A05	TM0_ACI5
PC_02	UART0_TX	TRACE_D03	SPI0_RDY		
PC_03	SPI0_CLK	PWM2_CH			
PC_04	SPI0_MISO	PWM2_CL			
PC_05	SPI0_MOSI	PWM2_DH			
PC_06	SPI0_SEL1	PWM2_DL			SYS_DSWAKE0
PC_07	SINC0_CLK1	UART2_TX	UART1_RTS		SYS_DSWAKE1
PC_08		SPT0_BCLK	SMC0_D00		
PC_09		SPT0_BFS	SMC0_D01		
PC_10		SPT0_BD0	SMC0_D02		
PC_11	SMC0_AMS3	SPT0_BD1	SMC0_D03		
PC_12		SPI1_CLK	SMC0_D04		
PC_13		SPI1_MISO	SMC0_D05		
PC_14		SPI1_MOSI	SMC0_D06		
PC_15		SPI1_SEL1	SMC0_D07		SPI1_SS

Table 22. Signal Multiplexing for Port D (212-Ball BGA)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PD_00			SMC0_D08	TM0_TMR0	
PD_01			SMC0_D09	TM0_TMR1	
PD_02			SMC0_D10	TM0_TMR2	
PD_03			SMC0_D11	TM0_TMR3	
PD_04			SMC0_D12	TM0_TMR4	
PD_05			SMC0_D13	TM0_TMR5	
PD_06			SMC0_D14	TM0_TMR6	
PD_07			SMC0_D15	TM0_TMR7	
PD_08			SMC0_A06	TM0_CLK	
PD_09			SMC0_A07	TM0_ACI5	
PD_10			SMC0_A08	TM0_ACI4	
PD_11			SMC0_A09	TM0_ACI3	
PD_12			SMC0_A10	TM0_ACI2	
PD_13			SMC0_A11	TM0_ACI1	
PD_14			SMC0_A12		
PD_15			SMC0_A13		

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PA_15	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 15 | PWM1 Channel B Low Side | TM0 Timer 3 | SMC0 Data 7 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_00	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 0 | PWM0 Channel D High Side | Embedded Trace Module Clock | SPORT0 Channel A Clock | SMC0 Data 8 | CNT0 Count Zero Marker Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_01	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 1 | PWM0 Channel D Low Side | Embedded Trace Module Data 0 | SPORT0 Channel A Frame Sync | SMC0 Data 9 | CNT0 Count Up and Direction Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_02	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 2 | PWM1 Channel D High Side | Embedded Trace Module Data 1 | SPORT0 Channel A Data 0 | SMC0 Data 10 | CNT0 Count Down and Gate Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_03	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 3 | PWM1 Channel D Low Side | Embedded Trace Module Data 2 | SPORT0 Channel A Data 1 | SMC0 Data 11 | CNT1 Count Zero Marker Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_04	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 4 | PWM2 Sync | UART0 Request to Send | SPORT0 Channel A Transmit Data Valid | SMC0 Data 12 | CNT1 Count Up and Direction Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_05	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 5 | PWM2 Trip Input 0 | UART0 Clear to Send | TM0 Timer 7 | SMC0 Data 13 | CNT1 Count Down and Gate Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_06	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 6 | PWM2 Channel A High Side | TM0 Common Clock | SPI1 Slave Select Output 2 | SMC0 Data 14 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_07	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 7 | PWM2 Channel A Low Side | TM0 Timer 0 | SPI1 Slave Select Output 3 | SMC0 Data 15 | Capture Timer0 Input 0 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

Clock and Reset Timing

Table 34 and Figure 24 describe clock and reset operations related to the clock generation unit (CGU) and reset control unit (RCU). Per the CCLK, SCLK, USBCLK, and OCLK timing specifications in Table 27 Clock Related Operating Conditions, combinations of SYS_CLKIN and clock multipliers must not select clock rates in excess of the processor's maximum instruction rate.

Table 34. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
f_{CKIN}	SYS_CLKIN Frequency (Using a Crystal)[1, 2, 3]	20	50	MHz
f_{CKIN}	SYS_CLKIN Frequency (Using a Crystal Oscillator)[1, 2, 3]	20	60	MHz
t_{CKINL}	SYS_CLKIN Low Pulse[1]	6.67		ns
t_{CKINH}	SYS_CLKIN High Pulse[1]	6.67		ns
t_{WRST}	$\overline{\text{SYS\_HWRST}}$ Asserted Pulse Width Low[4]	11 × t_{CKIN}		ns

[1] Applies to PLL bypass mode and PLL nonbypass mode.
[2] The t_{CKIN} period (see Figure 24) equals $1/f_{CKIN}$.
[3] If the CGU_CTL.DF bit is set, the minimum f_{CKIN} specification is 40 MHz.
[4] Applies after power-up sequence is complete. See Table 35 and Figure 25 for power-up reset timing.

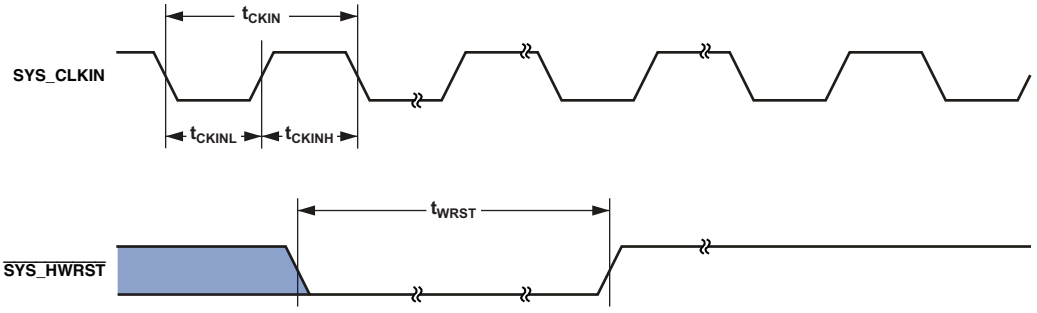


Figure 24. Clock and Reset Timing

Asynchronous Flash Read

Table 37 and Figure 27 show asynchronous flash memory read timing, related to the static memory controller (SMC).

Table 37. Asynchronous Flash Read

Parameter		Min	Max	Unit
Switching Characteristics				
t_{AMSADV}	SMC0_Ax (Address)/$\overline{\text{SMC0\_AMSx}}$ Assertion Before $\overline{\text{SMC0\_AOE}}$ Low[1]	PREST × t_{SCLK} – 2		ns
t_{WADV}	$\overline{\text{SMC0\_AOE}}$ Active Low Width[2]	RST × t_{SCLK} – 3		ns
$t_{DADVARE}$	$\overline{\text{SMC0\_ARE}}$ Low Delay From $\overline{\text{SMC0\_AOE}}$ High[3]	PREAT × t_{SCLK} – 3		ns
t_{HARE}	Output[4] Hold After $\overline{\text{SMC0\_ARE}}$ High[5]	RHT × t_{SCLK} – 2		ns
t_{WARE}[6]	$\overline{\text{SMC0\_ARE}}$ Active Low Width[7]	RAT × t_{SCLK} – 2		ns

[1] PREST value set using the SMC_BxETIM.PREST bits.
[2] RST value set using the SMC_BxTIM.RST bits.
[3] PREAT value set using the SMC_BxETIM.PREAT bits.
[4] Output signals are SMC0_Ax, $\overline{\text{SMC0\_AMS}}$.
[5] RHT value set using the SMC_BxTIM.RHT bits.
[6] SMC0_BxCTL.ARDYEN bit = 0.
[7] RAT value set using the SMC_BxTIM.RAT bits.

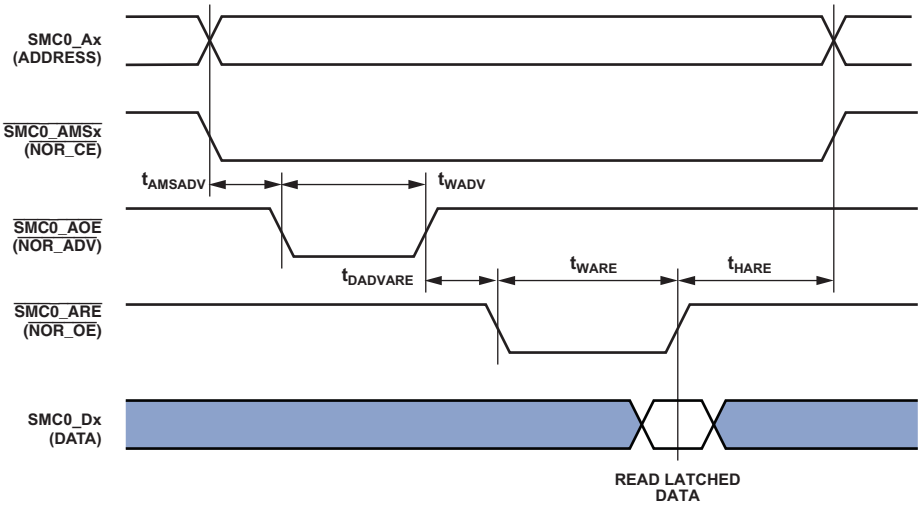


Figure 27. Asynchronous Flash Read

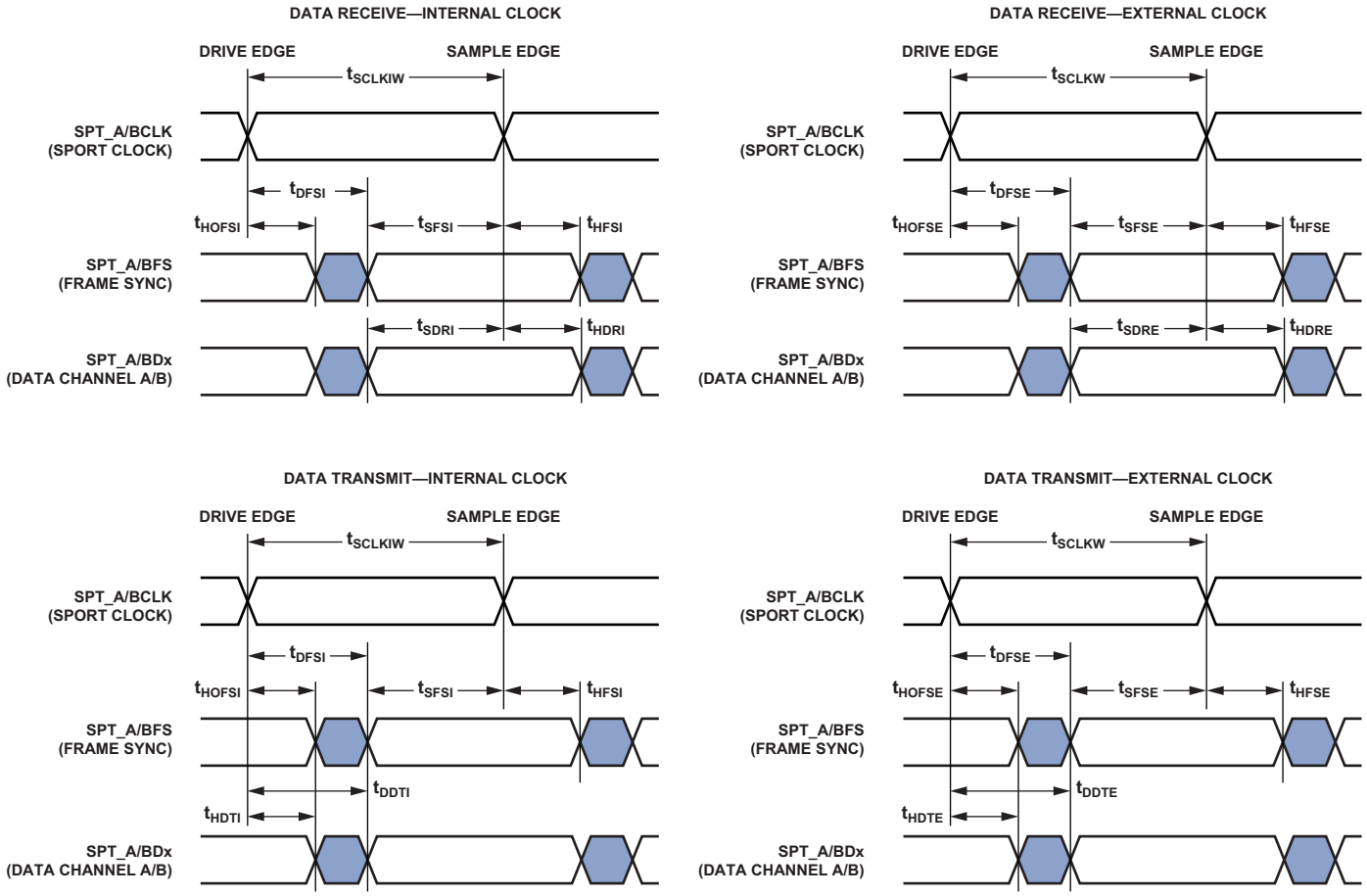


Figure 31. Serial Ports

Table 44. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External Transmit SPT_CLK[1]	1		ns
t_{DDTTE}	Data Disable from External Transmit SPT_CLK[1]		14	ns
t_{DDTIN}	Data Enable from Internal Transmit SPT_CLK[1]	–1		ns
t_{DDTTI}	Data Disable from Internal Transmit SPT_CLK[1]		2.8	ns

[1] Referenced to drive edge.

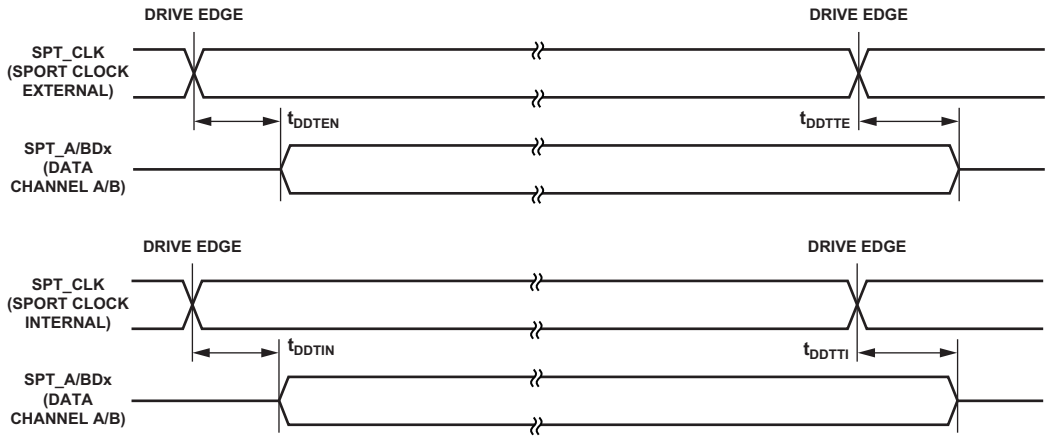


Figure 32. Serial Ports—Enable and Three-State

The SPT_TDV output signal becomes active in SPORT multichannel mode. During transmit slots (enabled with active channel selection registers) the SPT_TDV is asserted for communication with external devices.

Table 45. Serial Ports—Transmit Data Valid (TDV)

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DRDVEN}	Data-Valid Enable Delay from Drive Edge of External Clock[1]	2		ns
t_{DFDVEN}	Data-Valid Disable Delay from Drive Edge of External Clock[1]		14	ns
t_{DRDVIN}	Data-Valid Enable Delay from Drive Edge of Internal Clock[1]	–1		ns
t_{DFDVIN}	Data-Valid Disable Delay from Drive Edge of Internal Clock[1]		3.5	ns

[1] Referenced to drive edge.

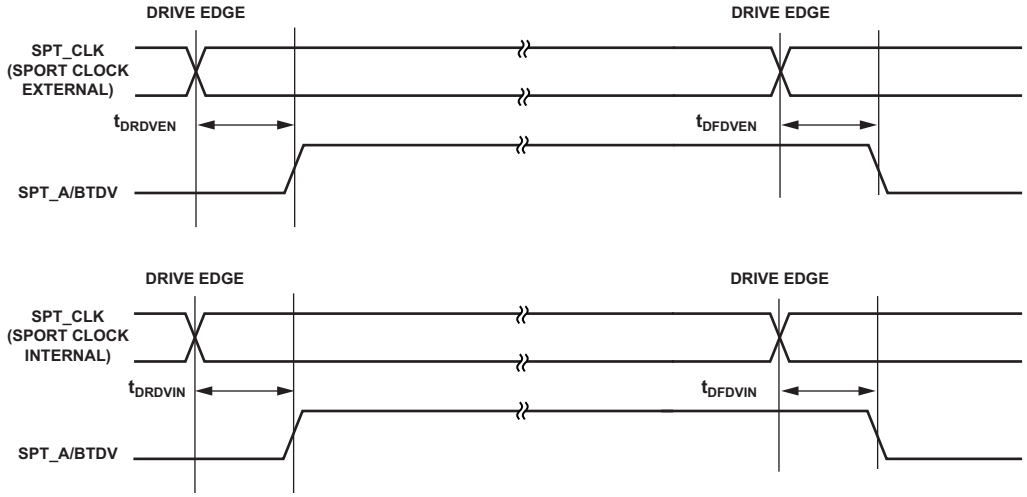


Figure 33. Serial Ports—Transmit Data Valid Internal and External Clock

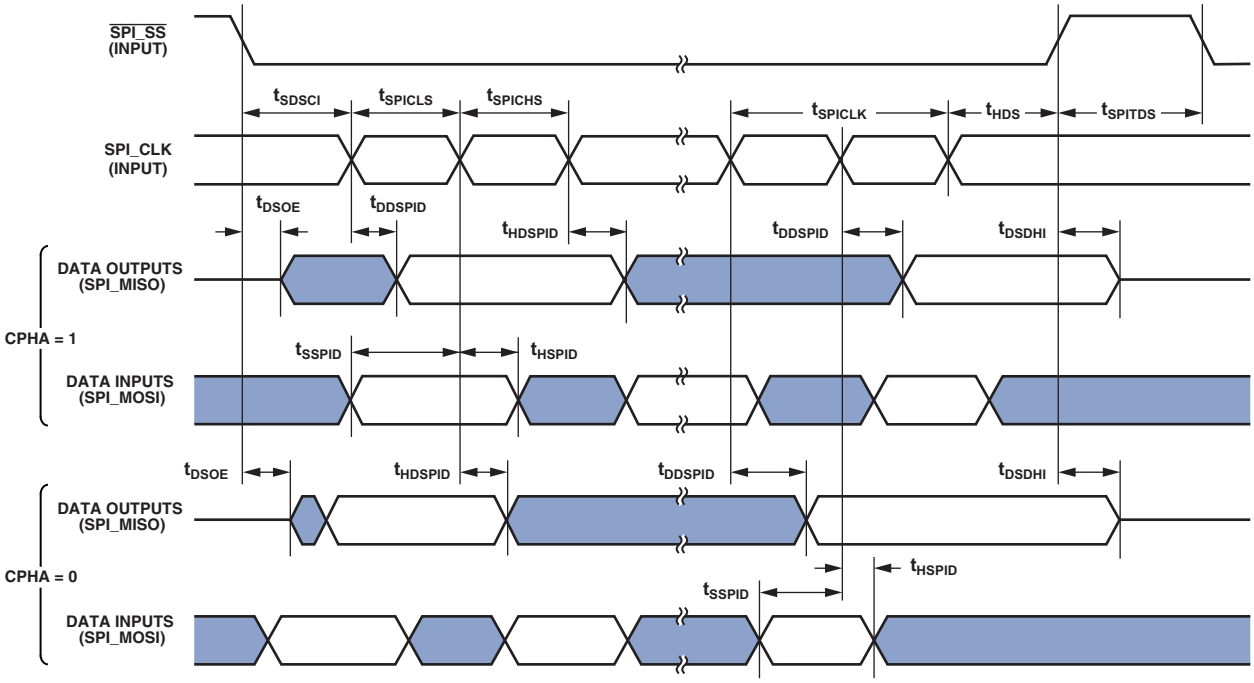


Figure 36. Serial Peripheral Interface (SPI) Port—Slave Timing

10/100 Ethernet MAC Controller (EMAC) Timing

Table 61 through Table 63 and Figure 52 through Figure 54 describe the 10/100 Ethernet MAC controller operations. Note the externally generated Ethernet MAC clock is called $f_{REFCLKEXT}$:

$$t_{REFCLKEXT} = \frac{1}{f_{REFCLKEXT}}$$

Table 61. 10/100 Ethernet MAC Controller (EMAC) Timing: RMII Receive Signal

Parameter[1]		Min	Max	Unit
Timing Requirements				
t_{REFCLK}	ETHx_REFCLK Period[2]	$t_{REFCLKEXT}$ – 1%		ns
$t_{REFCLKW}$	ETHx_REFCLK Width[2]	$t_{REFCLKEXT}$ × 35%	$t_{REFCLKEXT}$ × 65%	ns
$t_{REFCLKIS}$	Rx Input Valid to RMII ETHx_REFCLK Rising Edge (Data In Setup)	4		ns
$t_{REFCLKIH}$	RMII ETHx_REFCLK Rising Edge to Rx Input Invalid (Data In Hold)	2.0		ns

[1] RMII inputs synchronous to RMII REF_CLK are ERxDx, RMII CRS_DV, and ERxER.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external REF_CLK. For the external REF_CLK maximum frequency see the $t_{REFCLKEXT}$ specification in Table 27 Clock Related Operating Conditions.

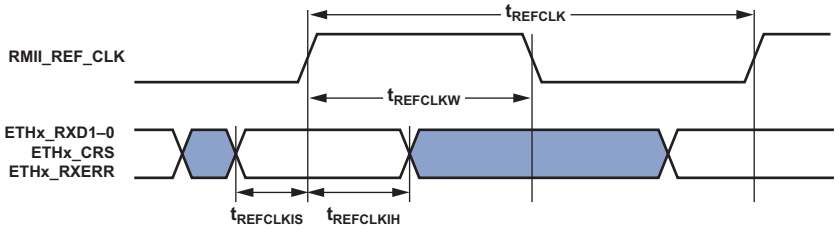


Figure 52. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal

Table 62. 10/100 Ethernet MAC Controller (EMAC) Timing: RMII Transmit Signal

Parameter[1]		Min	Max	Unit
Switching Characteristics				
$t_{REFCLKOV}$	RMII ETHx_REFCLK Rising Edge to Transmit Output Valid (Data Out Valid)		14	ns
$t_{REFCLKOH}$	RMII ETHx_REFCLK Rising Edge to Transmit Output Invalid (Data Out Hold)	2		ns

[1] RMII outputs synchronous to RMII REF_CLK are ETxDx.

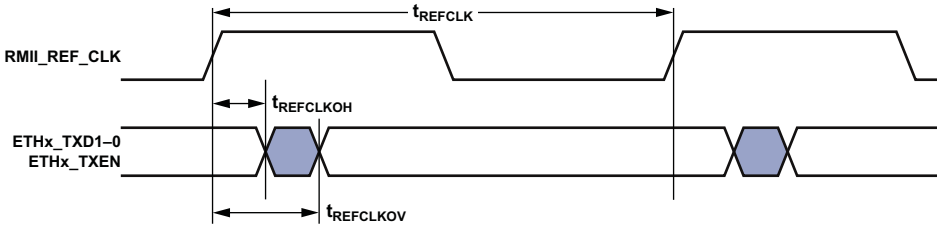
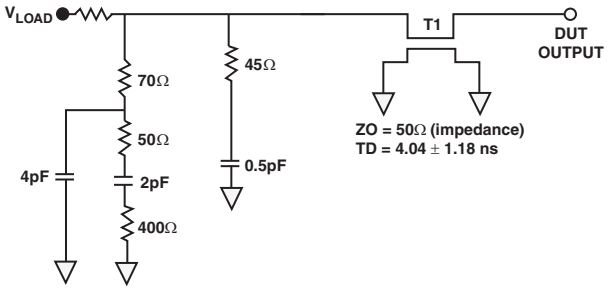


Figure 53. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD), IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 63. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

The graph of Figure 64 shows how output rise and fall times vary with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.

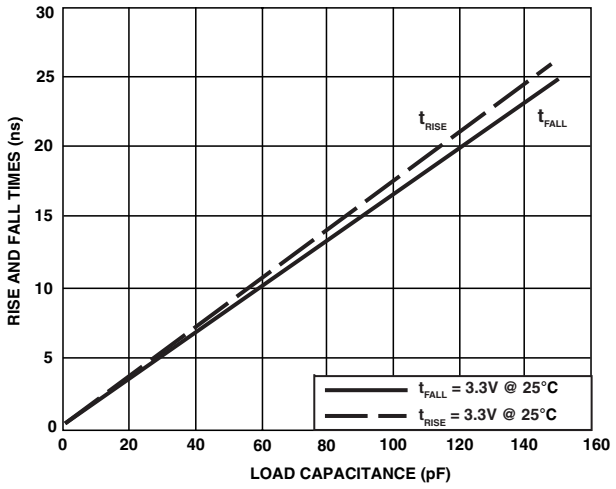


Figure 64. Driver Type A Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application printed circuit board, use the following equation:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C).

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 68, Table 69, and Table 70.

P_D = Power dissipation (see Total Power Dissipation (PD) on Page 67 for the method to calculate P_D).

Table 68. Thermal Characteristics (120-Lead LQFP)

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	21.5	°C/W
θ_{JA}	1 linear m/s air flow	19.2	°C/W
θ_{JA}	2 linear m/s air flow	18.4	°C/W
θ_{JC}		9.29	°C/W
Ψ_{JT}	0 linear m/s air flow	0.25	°C/W
Ψ_{JT}	1 linear m/s air flow	0.40	°C/W
Ψ_{JT}	2 linear m/s air flow	0.56	°C/W

Table 69. Thermal Characteristics (176-Lead LQFP)

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	21.5	°C/W
θ_{JA}	1 linear m/s air flow	19.3	°C/W
θ_{JA}	2 linear m/s air flow	18.5	°C/W
θ_{JC}		9.24	°C/W
Ψ_{JT}	0 linear m/s air flow	0.25	°C/W
Ψ_{JT}	1 linear m/s air flow	0.37	°C/W
Ψ_{JT}	2 linear m/s air flow	0.48	°C/W

Table 70. Thermal Characteristics (212-Ball BGA)

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	30.0	°C/W
θ_{JA}	1 linear m/s air flow	27.5	°C/W
θ_{JA}	2 linear m/s air flow	26.5	°C/W
θ_{JC}		9.2	°C/W
Ψ_{JT}	0 linear m/s air flow	0.15	°C/W
Ψ_{JT}	1 linear m/s air flow	0.24	°C/W
Ψ_{JT}	2 linear m/s air flow	0.27	°C/W