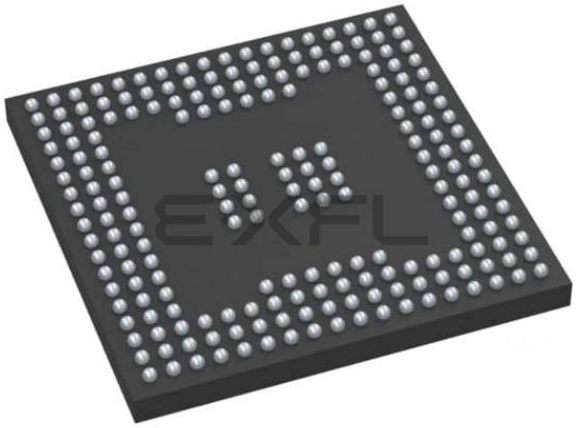

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	CAN, Ethernet, I²C, SPI, SPORT, UART/USART, USB
Clock Rate	240MHz
Non-Volatile Memory	FLASH (2MB)
On-Chip RAM	384kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	212-LBGA, CSPBGA
Supplier Device Package	212-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-cm409cbcz-af

GENERAL DESCRIPTION

The ADSP-CM40xF family of mixed-signal control processors is based on the ARM® Cortex-M4™ processor core with floating-point unit operating at frequencies up to 240 MHz and integrating up to 384 kB of SRAM memory, 2 MB of flash memory, accelerators and peripherals optimized for motor control and photo-voltaic (PV) inverter control and an analog module consisting of two 16-bit SAR ADCs and two 12-bit DACs. The ADSP-CM40xF family operates from a single voltage supply (VDD_EXT/VDD_ANA), generating its own internal voltage supplies using internal voltage regulators and an external pass transistor.

This family of mixed-signal control processors offers low static power consumption and is produced with a low power and low voltage design methodology, delivering world class processor and ADC performance with lower power consumption.

By integrating a rich set of industry-leading system peripherals and memory (shown in Table 1), the ADSP-CM40xF mixed-signal control processors are the platform of choice for next-generation applications that require RISC programmability, advanced communications and leading-edge signal processing in one integrated package. These applications span a wide array of markets including power/motor control, embedded industrial, instrumentation, medical and consumer.

Each ADSP-CM40xF family member contains the following modules.

- 8 GP timers with PWM output
- 3-phase PWM units with up to 4 output pairs per unit
- 2 CAN modules
- 1 two-wire interface (TWI) module
- 3 UARTs
- 1 ADC controller (ADCC) to control on-chip ADCs
- 1 DAC controller (DACC) to control on-chip DACs
- 4 Sinus Cardinalis (SINC) filter pairs
- 1 harmonic analysis engine (HAE)
- 2 SPI (1 connected to internal SPI flash memory)
- 3 half-SPORTs
- 1 watchdog timer unit
- 3 capture timer units
- 1 cyclic redundancy check (CRC)

Table 1 provides the additional product features shown by model.

Table 1. ADSP-CM4 0xF Family Product Features

Generic	**ADSP-CM402F**		**ADSP-CM403F**			**ADSP-CM407F**			**ADSP-CM408F**		**ADSP-CM409F**
Package	120-Lead LQFP					176-Lead LQFP					212-Ball BGA
GPIOs	40					91					
SMC	16-Bit Asynchronous/5 Address					16-Bit Asynchronous/24 Address					
ADC ENOB (No Averaging)	11+		13+			11+			13+		
ADC Inputs	24					16					24
DAC Outputs	2					N/A					2
SPORTs	3 Half-SPORTs					4 Half-SPORTs					
Ethernet	N/A					1	N/A	N/A	1	N/A	1
USB	N/A					1	1	N/A	1	1	1
External SPI	1					2					
HAE	1										
CAN	2										
UART	3										
Feature Set Code	E	F	C	E	F	A	B	D	A	B	A
L1 SRAM (kB)	128	128	384	128	128	384	384	128	384	384	384
Flash (kB)	512	256	2048	512	256	2048	2048	1024	2048	2048	2048
Core Clock (MHz)	150	100	240	150	100	240	240	150	240	240	240
Model	ADSP-CM402CSWZ-EF	ADSP-CM402CSWZ-FF	ADSP-CM403CSWZ-CF	ADSP-CM403CSWZ-EF	ADSP-CM403CSWZ-FF	ADSP-CM407CSWZ-AF	ADSP-CM407CSWZ-BF	ADSP-CM407CSWZ-DF	ADSP-CM408CSWZ-AF	ADSP-CM408CSWZ-BF	ADSP-CM409CBCZ-AF

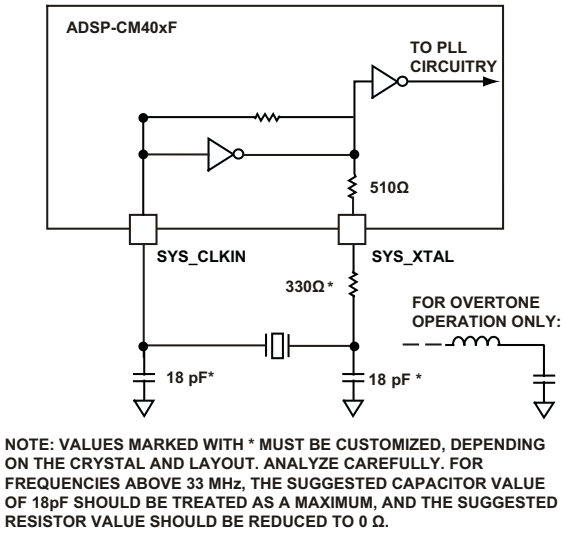

Figure 8. External Crystal Connection

The two capacitors and the 330 Ω series resistor shown in Figure 8 fine tune phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 8 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over temperature range.

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit as shown in Figure 8. A design procedure for third-overtone operation is discussed in detail in application note (EE-168) "Using Third Overtone Crystals with the ADSP-218x DSP" (www.analog.com/ee-168).

Oscillator Watchdog

A programmable oscillator watchdog unit is provided to allow verification of proper startup and harmonic mode of the external crystal. This allows the user to specify the expected frequency of oscillation, and to enable detection of non-oscillation and improper-oscillation faults. These events can be routed to the SYS_FAULT output pin and/or to cause a reset of the part.

Clock Generation Unit (CGU)

The clock generation unit (CGU) generates all on-chip clocks and synchronization signals. Multiplication factors are programmed to the PLLs to define the PLLCLK frequency. Programmable values divide the PLLCLK frequency to generate the core clock (CCLK), the system clocks (SCLK), and the output clock (OCLK). This is illustrated in Figure 10 on Page 64.

Writing to the CGU control registers does not affect the behavior of the PLL immediately. Registers are first programmed with a new value, and the PLL logic executes the changes so that it transitions smoothly from the current conditions to the new ones.

SYS_CLKIN oscillations start when power is applied to the VDD_EXT pins. The rising edge of SYS_HWRST can be applied as soon as all voltage supplies are within specifications (see Operating Conditions on Page 64), and SYS_CLKIN oscillations are stable.

Clock Out/External Clock

A SYS_CLKOUT output pin has programmable options to output divided-down versions of the on-chip clocks, including USB clocks. By default, the SYS_CLKOUT pin drives a buffered version of the SYS_CLKIN input. Clock generation faults (for example PLL unlock) may trigger a reset by hardware.

SYS_CLKOUT can be used to output one of several different clocks used on the processor. The clocks shown in Table 4 can be outputs from SYS_CLKOUT.

Table 4. SYS_CLKOUT Source and Divider Options

Clock Source	Divider
CCLK (Core Clock)	By 4
OCLK (Output Clock)	Programmable
USBCLK	Programmable
CLKBUF	None, direct from SYS_CLKIN

Power Management

As shown in Table 5 and Figure 4 on Page 6, the processor requires three different power domains, VDD_INT, VDD_EXT, and VDD_ANA. By isolating the internal logic of the processor into its own power domain, separate from other I/O, the processor can take advantage of dynamic power management without affecting the other I/O devices. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate Specifications table for processor operating conditions; even if the feature/peripheral is not used.

The dynamic power management feature of the processor allows the processor's core clock frequency (f_{CCLK}) to be dynamically controlled.

Table 5. Power Domains

Power Domain	V_{DD} Range
All Internal Logic	V_{DD_INT}
Digital I/O	V_{DD_EXT}
Analog	V_{DD_ANA}

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation. For more information on power pins, see Operating Conditions on Page 64.

Table 6. ADSP-CM40xF Detailed Signal Description (Continued)

Signal Name	Direction	Description
USB_ID	Input	**USB OTG ID.** Senses whether the controller is a host or device. This signal is pulled low when an A-type plug is sensed (signifying that the USB controller is the A device), but the input is high when a B-type plug is sensed (signifying that the USB controller is the B device).
USB_VBC	Output	**USB VBUS Control.** Controls an external voltage source to supply VBUS when in host mode. May be configured as open drain. Polarity is configurable as well.
USB_VBUS	I/O	**USB Bus Voltage.** Connects to bus voltage in host and device modes.
VREFn	I/O	**Voltage Reference for ADC.** When internal reference is selected for ADC, the VREF pin is used for connecting bypass caps. When external reference is selected, an external reference device should be connected to these pins to supply the external reference voltage. n=0,1.
VREG_BASE	Output	**Voltage Regulator Base Node.** Connected to Base of PNP transistor when using internal VDD_INT reference.

ADSP-CM402F/ADSP-CM403F GPIO MULTIPLEXING FOR 120-LEAD LQFP

Table 8 through Table 10 identify the pin functions that are multiplexed on the general-purpose I/O pins of the 120-lead LQFP package.

Table 8. Signal Multiplexing for Port A (120-Lead LQFP)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PA_00	PWM0_SYNC		SPT1_ACLK		
PA_01	PWM0_TRIP0		SPT1_AFS		
PA_02	PWM0_AH		SPT1_AD0		
PA_03	PWM0_AL		SPT1_AD1		
PA_04	PWM0_BH		SPT1_BCLK		
PA_05	PWM0_BL		SPT1_BFS		
PA_06	PWM0_CH		SPT1_BD0		
PA_07	PWM0_CL	SMC0_AMS2	SPT1_BD1		
PA_08	PWM1_CH		SMC0_D00		TM0_ACLK5
PA_09	PWM1_CL		SMC0_D01		TM0_ACLK4
PA_10	PWM1_SYNC		SMC0_D02		TM0_ACLK3
PA_11	PWM1_TRIP0	UART1_CTS	SMC0_D03		TM0_ACLK2
PA_12	PWM1_AH	TM0_TMR4	SMC0_D04		
PA_13	PWM1_AL	TM0_TMR5	SMC0_D05		
PA_14	PWM1_BH	TM0_TMR6	SMC0_D06		
PA_15	PWM1_BL	TM0_TMR3	SMC0_D07		

Table 9. Signal Multiplexing for Port B (120-Lead LQFP)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PB_00	PWM0_DH	TRACE_CLK	SPT0_ACLK	SMC0_D08	CNT0_ZM
PB_01	PWM0_DL	TRACE_D00	SPT0_AFS	SMC0_D09	CNT0_UD
PB_02	PWM1_DH	TRACE_D01	SPT0_AD0	SMC0_D10	CNT0_DG
PB_03	PWM1_DL	TRACE_D02	SPT0_AD1	SMC0_D11	CNT1_ZM
PB_04	PWM2_SYNC	UART0_RTS	SPT0_ATDV	SMC0_D12	CNT1_UD
PB_05	PWM2_TRIP0	UART0_CTS	TM0_TMR7	SMC0_D13	CNT1_DG
PB_06	PWM2_AH	TM0_CLK		SMC0_D14	
PB_07	PWM2_AL	TM0_TMR0		SMC0_D15	CPTMR0_IN0
PB_08	PWM2_BH	TM0_TMR1	UART1_RX	SMC0_ARDY	TM0_ACI2/ CPTMR0_IN1
PB_09	PWM2_BL	TM0_TMR2	UART1_TX	SMC0_ARE	CPTMR0_IN2
PB_10	SINC0_CLK0	SPI0_D2	CAN1_RX	SMC0_AWE	TM0_ACI1
PB_11	SINC0_D0	SPI0_D3	CAN1_TX	SMC0_AMS0	TM0_ACLK1
PB_12	SINC0_D1		UART2_RX	SMC0_AOE	TM0_ACI3
PB_13	SINC0_D2	CNT0_OUTA	SPI0_SEL2	SMC0_A01	TM0_ACLK0/ SYS_DSWAKE3
PB_14	SINC0_D3	CNT0_OUTB	SPI0_SEL3	SMC0_A02	SPI0_SS/ SYS_DSWAKE2
PB_15	CAN0_RX	SPT1_ATDV	UART1_RX	SMC0_A03	TM0_ACI4

Table 11. ADSP-CM407F/ADSP-CM408F 176-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_A06	SMC0 Address 6	D	PD_08
SMC0_A07	SMC0 Address 7	D	PD_09
SMC0_A08	SMC0 Address 8	D	PD_10
SMC0_A09	SMC0 Address 9	D	PD_11
SMC0_A10	SMC0 Address 10	D	PD_12
SMC0_A11	SMC0 Address 11	D	PD_13
SMC0_A12	SMC0 Address 12	D	PD_14
SMC0_A13	SMC0 Address 13	D	PD_15
SMC0_A14	SMC0 Address 14	E	PE_00
SMC0_A15	SMC0 Address 15	E	PE_01
SMC0_A16	SMC0 Address 16	E	PE_02
SMC0_A17	SMC0 Address 17	E	PE_03
SMC0_A18	SMC0 Address 18	E	PE_04
SMC0_A19	SMC0 Address 19	E	PE_05
SMC0_A20	SMC0 Address 20	E	PE_06
SMC0_A21	SMC0 Address 21	E	PE_07
SMC0_A22	SMC0 Address 22	E	PE_08
SMC0_A23	SMC0 Address 23	E	PE_09
SMC0_A24	SMC0 Address 24	E	PE_11
$\overline{\text{SMC0\_ABE0}}$	SMC0 Byte Enable 0	F	PF_10
$\overline{\text{SMC0\_ABE1}}$	SMC0 Byte Enable 1	F	PF_02
$\overline{\text{SMC0\_AMS0}}$	SMC0 Memory Select 0	B	PB_11
$\overline{\text{SMC0\_AMS0}}$	SMC0 Memory Select 0	Not Muxed	$\overline{\text{SMC0\_AMS0}}$
$\overline{\text{SMC0\_AMS1}}$	SMC0 Memory Select 1	E	PE_10
$\overline{\text{SMC0\_AMS2}}$	SMC0 Memory Select 2	A	PA_07
$\overline{\text{SMC0\_AMS3}}$	SMC0 Memory Select 3	C	PC_11
$\overline{\text{SMC0\_AOE}}$	SMC0 Output Enable	B	PB_12
$\overline{\text{SMC0\_AOE}}$	SMC0 Output Enable	F	PF_03
SMC0_ARDY	SMC0 Asynchronous Ready	B	PB_08
SMC0_ARDY	SMC0 Asynchronous Ready	F	PF_04
$\overline{\text{SMC0\_ARE}}$	SMC0 Read Enable	B	PB_09
$\overline{\text{SMC0\_ARE}}$	SMC0 Read Enable	Not Muxed	$\overline{\text{SMC0\_ARE}}$
$\overline{\text{SMC0\_AWE}}$	SMC0 Write Enable	B	PB_10
$\overline{\text{SMC0\_AWE}}$	SMC0 Write Enable	Not Muxed	$\overline{\text{SMC0\_AWE}}$
SMC0_D00	SMC0 Data 0	A	PA_08
SMC0_D00	SMC0 Data 0	C	PC_08
SMC0_D01	SMC0 Data 1	A	PA_09
SMC0_D01	SMC0 Data 1	C	PC_09
SMC0_D02	SMC0 Data 2	A	PA_10
SMC0_D02	SMC0 Data 2	C	PC_10
SMC0_D03	SMC0 Data 3	A	PA_11
SMC0_D03	SMC0 Data 3	C	PC_11
SMC0_D04	SMC0 Data 4	A	PA_12
SMC0_D04	SMC0 Data 4	C	PC_12
SMC0_D05	SMC0 Data 5	A	PA_13
SMC0_D05	SMC0 Data 5	C	PC_13

Table 11. ADSP-CM407F/ADSP-CM408F 176-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SMC0_D06	SMC0 Data 6	A	PA_14
SMC0_D06	SMC0 Data 6	C	PC_14
SMC0_D07	SMC0 Data 7	A	PA_15
SMC0_D07	SMC0 Data 7	C	PC_15
SMC0_D08	SMC0 Data 8	B	PB_00
SMC0_D08	SMC0 Data 8	D	PD_00
SMC0_D09	SMC0 Data 9	B	PB_01
SMC0_D09	SMC0 Data 9	D	PD_01
SMC0_D10	SMC0 Data 10	B	PB_02
SMC0_D10	SMC0 Data 10	D	PD_02
SMC0_D11	SMC0 Data 11	B	PB_03
SMC0_D11	SMC0 Data 11	D	PD_03
SMC0_D12	SMC0 Data 12	B	PB_04
SMC0_D12	SMC0 Data 12	D	PD_04
SMC0_D13	SMC0 Data 13	B	PB_05
SMC0_D13	SMC0 Data 13	D	PD_05
SMC0_D14	SMC0 Data 14	B	PB_06
SMC0_D14	SMC0 Data 14	D	PD_06
SMC0_D15	SMC0 Data 15	B	PB_07
SMC0_D15	SMC0 Data 15	D	PD_07
SPI0_CLK	SPI0 Clock	C	PC_03
SPI0_D2	SPI0 Data 2	B	PB_10
SPI0_D3	SPI0 Data 3	B	PB_11
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_04
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_05
SPI0_RDY	SPI0 Ready	C	PC_02
$\overline{\text{SPI0\_SEL1}}$	SPI0 Slave Select Output 1	C	PC_06
$\overline{\text{SPI0\_SEL2}}$	SPI0 Slave Select Output 2	B	PB_13
$\overline{\text{SPI0\_SEL3}}$	SPI0 Slave Select Output 3	B	PB_14
$\overline{\text{SPI0\_SS}}$	SPI0 Slave Select Input	B	PB_14
SPI1_CLK	SPI1 Clock	C	PC_12
SPI1_MISO	SPI1 Master In, Slave Out	C	PC_13
SPI1_MOSI	SPI1 Master Out, Slave In	C	PC_14
$\overline{\text{SPI1\_SEL1}}$	SPI1 Slave Select Output 1	C	PC_15
$\overline{\text{SPI1\_SEL2}}$	SPI1 Slave Select Output 2	B	PB_06
$\overline{\text{SPI1\_SEL3}}$	SPI1 Slave Select Output 3	B	PB_07
$\overline{\text{SPI1\_SS}}$	SPI1 Slave Select Input	C	PC_15
SPT0_ACLK	SPORT0 Channel A Clock	B	PB_00
SPT0_ACLK	SPORT0 Channel A Clock	E	PE_00
SPT0_AD0	SPORT0 Channel A Data 0	B	PB_02
SPT0_AD0	SPORT0 Channel A Data 0	E	PE_02
SPT0_AD1	SPORT0 Channel A Data 1	B	PB_03
SPT0_AD1	SPORT0 Channel A Data 1	E	PE_03
SPT0_AFS	SPORT0 Channel A Frame Sync	B	PB_01
SPT0_AFS	SPORT0 Channel A Frame Sync	E	PE_01
SPT0_ATDV	SPORT0 Channel A Transmit Data Valid	B	PB_04

Table 18. ADSP-CM409F 212-Ball BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SPT0_AD1	SPORT0 Channel A Data 1	B	PB_03
SPT0_AD1	SPORT0 Channel A Data 1	E	PE_03
SPT0_AFS	SPORT0 Channel A Frame Sync	B	PB_01
SPT0_AFS	SPORT0 Channel A Frame Sync	E	PE_01
SPT0_ATDV	SPORT0 Channel A Transmit Data Valid	B	PB_04
SPT0_BCLK	SPORT0 Channel B Clock	C	PC_08
SPT0_BD0	SPORT0 Channel B Data 0	C	PC_10
SPT0_BD1	SPORT0 Channel B Data 1	C	PC_11
SPT0_BFS	SPORT0 Channel B Frame Sync	C	PC_09
SPT0_BTDV	SPORT0 Channel B Transmit Data Valid	B	PB_12
SPT1_ACLK	SPORT1 Channel A Clock	A	PA_00
SPT1_AD0	SPORT1 Channel A Data 0	A	PA_02
SPT1_AD1	SPORT1 Channel A Data 1	A	PA_03
SPT1_AFS	SPORT1 Channel A Frame Sync	A	PA_01
SPT1_ATDV	SPORT1 Channel A Transmit Data Valid	B	PB_15
SPT1_BCLK	SPORT1 Channel B Clock	A	PA_04
SPT1_BD0	SPORT1 Channel B Data 0	A	PA_06
SPT1_BD1	SPORT1 Channel B Data 1	A	PA_07
SPT1_BFS	SPORT1 Channel B Frame Sync	A	PA_05
SPT1_BTDV	SPORT1 Channel B Transmit Data Valid	C	PC_00
SYS_BMODE0	Boot Mode Control 0	Not Muxed	SYS_BMODE0
SYS_BMODE1	Boot Mode Control 1	Not Muxed	SYS_BMODE1
SYS_CLKIN	Clock/Crystal Input	Not Muxed	SYS_CLKIN
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
SYS_DSWAKE0	Deep Sleep Wake-up 0	C	PC_06
SYS_DSWAKE1	Deep Sleep Wake-up 1	C	PC_07
SYS_DSWAKE2	Deep Sleep Wake-up 2	B	PB_14
SYS_DSWAKE3	Deep Sleep Wake-up 3	B	PB_13
$\overline{\text{SYS\_FAULT}}$	System Fault Output	Not Muxed	$\overline{\text{SYS\_FAULT}}$
$\overline{\text{SYS\_HWRST}}$	Processor Hardware Reset Control	Not Muxed	$\overline{\text{SYS\_HWRST}}$
$\overline{\text{SYS\_NMI}}$	Nonmaskable Interrupt	Not Muxed	$\overline{\text{SYS\_NMI}}$
$\overline{\text{SYS\_RESOUT}}$	Reset Output	Not Muxed	$\overline{\text{SYS\_RESOUT}}$
SYS_XTAL	Crystal Output	Not Muxed	SYS_XTAL
TM0_ACI1	TIMER0 Alternate Capture Input 1	B	PB_10
TM0_ACI1	TIMER0 Alternate Capture Input 1	D	PD_13
TM0_ACI2	TIMER0 Alternate Capture Input 2	B	PB_08
TM0_ACI2	TIMER0 Alternate Capture Input 2	D	PD_12
TM0_ACI3	TIMER0 Alternate Capture Input 3	B	PB_12
TM0_ACI3	TIMER0 Alternate Capture Input 3	D	PD_11
TM0_ACI4	TIMER0 Alternate Capture Input 4	B	PB_15
TM0_ACI4	TIMER0 Alternate Capture Input 4	D	PD_10
TM0_ACI5	TIMER0 Alternate Capture Input 5	C	PC_01
TM0_ACI5	TIMER0 Alternate Capture Input 5	D	PD_09
TM0_ACLK0	TIMER0 Alternate Clock 0	B	PB_13
TM0_ACLK1	TIMER0 Alternate Clock 1	B	PB_11
TM0_ACLK2	TIMER0 Alternate Clock 2	A	PA_11

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PA_15	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PA Position 15 | PWM1 Channel B Low Side | TM0 Timer 3 | SMC0 Data 7 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_00	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 0 | PWM0 Channel D High Side | Embedded Trace Module Clock | SPORT0 Channel A Clock | SMC0 Data 8 | CNT0 Count Zero Marker Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_01	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 1 | PWM0 Channel D Low Side | Embedded Trace Module Data 0 | SPORT0 Channel A Frame Sync | SMC0 Data 9 | CNT0 Count Up and Direction Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_02	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 2 | PWM1 Channel D High Side | Embedded Trace Module Data 1 | SPORT0 Channel A Data 0 | SMC0 Data 10 | CNT0 Count Down and Gate Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_03	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 3 | PWM1 Channel D Low Side | Embedded Trace Module Data 2 | SPORT0 Channel A Data 1 | SMC0 Data 11 | CNT1 Count Zero Marker Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_04	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 4 | PWM2 Sync | UART0 Request to Send | SPORT0 Channel A Transmit Data Valid | SMC0 Data 12 | CNT1 Count Up and Direction Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_05	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 5 | PWM2 Trip Input 0 | UART0 Clear to Send | TM0 Timer 7 | SMC0 Data 13 | CNT1 Count Down and Gate Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_06	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 6 | PWM2 Channel A High Side | TM0 Common Clock | SPI1 Slave Select Output 2 | SMC0 Data 14 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_07	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 7 | PWM2 Channel A Low Side | TM0 Timer 0 | SPI1 Slave Select Output 3 | SMC0 Data 15 | Capture Timer0 Input 0 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.

Table 25. ADSP-CM40xF Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Int Term	Reset Term	Reset Drive	Power Domain	Description and Notes
PB_08	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 8 | PWM2 Channel B High Side | TM0 Timer 1 | UART1 Receive | SMC0 Asynchronous Ready | TM0 Timer2 Alternate Capture Input | Capture Timer0 Input 1 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_09	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 9 | PWM2 Channel B Low Side | TM0 Timer 2 | UART1 Transmit | SMC0 Read Enable | Capture Timer0 Input 2 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_10	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 10 | SINC0 Clock 0 | SPI0 Data 2 | CAN1 Receive | SMC0 Write Enable | TM0 Timer1 Alternate Capture Input Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_11	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 11 | SINC0 Data 0 | SPI0 Data 3 | CAN1 Transmit | SMC0 Memory Select 0 | TM0 Timer1 Alternate Clock Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_12	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 12 | SINC0 Data 1 | SPORT0 Channel B Transmit Data Valid | UART2 Receive | SMC0 Output Enable | TM0 Timer3 Alternate Capture Input Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_13	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 13 | SINC0 Data 2 | CNT0 Output Divider A | SPI0 Slave Select Output 2 | SMC0 Address 1 | SYS0 Deep Sleep Wakeup 3 | TM0 Timer0 Alternate Clock Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_14	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 14 | SINC0 Data 3 | CNT0 Output Divider B | SPI0 Slave Select Output 3 | SMC0 Address 2 | SYS0 Deep Sleep Wakeup 2 | SPI0 Slave Select Input Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PB_15	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PB Position 15 | CAN0 Receive | SPORT1 Channel A Transmit Data Valid | UART1 Receive | SMC0 Address 3 | TM0 Timer4 Alternate Capture Input Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.
PC_00	I/O	A	pu or none	pu	none	VDD_EXT	Desc: PC Position 0 | CAN0 Transmit | SPORT1 Channel B Transmit Data Valid | UART1 Transmit | SMC0 Address 4 Notes: By default, the internal termination pull-up is active. The state of pull-ups can be configured by configuring the PORT_INEN and PADS_PCFG0 registers.

Table 27. Clock Related Operating Conditions

Parameter		Restriction	Min	Typ	Max	Unit
f_{PLLCLK}	PLL Clock Frequency		250		960	MHz
f_{CCLK}	Core Clock Frequency	$f_{CCLK} \geq f_{SCLK}$			240	MHz
f_{SCLK}	SCLK Frequency[1, 2]				100	MHz
f_{USBCLK}	USBCLK Frequency[3, 4]	$f_{SCLK} \geq f_{USBCLK}$			60	MHz
f_{OCLK}	Output Clock Frequency				50	MHz
f_{TCK}	JTG_TCK Frequency	$f_{TCK} \leq f_{SCLK}/2$			50	MHz
$f_{SYS\_CLKOUTJ}$	SYS_CLKOUT Period Jitter[5, 6]			±1		%
$f_{ADCC\_ACLK\_PROG}$	Programmed ADCC ADC0 (A) Clock				50	MHz
$f_{ADCC\_BCLK\_PROG}$	Programmed ADCC ADC1 (B) Clock				50	MHz
$f_{DACC\_ACLK\_PROG}$	Programmed DACC DAC0 (A) Clock				50	MHz
$f_{DACC\_BCLK\_PROG}$	Programmed DACC DAC1 (B) Clock				50	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Transmitting Data and Frame Sync				50	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Receiving Data and Frame Sync				50	MHz
$f_{SPTCLKEXT}$	External SPT Clock When Transmitting Data and Frame Sync[7, 8]	$f_{SPTCLKEXT} \leq f_{SCLK}$			50	MHz
$f_{SPTCLKEXT}$	External SPT Clock When Receiving Data and Frame Sync[7, 8]	$f_{SPTCLKEXT} \leq f_{SCLK}$			50	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Transmitting Data[7, 8]				50	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Receiving Data				50	MHz
$f_{SPICLKEXT}$	External SPI Clock When Transmitting Data[7, 8]	$f_{SPICLKEXT} \leq f_{SCLK}$			50	MHz
$f_{SPICLKEXT}$	External SPI Clock When Receiving Data[7, 8]	$f_{SPICLKEXT} \leq f_{SCLK}$			50	MHz
$f_{TMRCLKEXT}$	External TMR Clock	$f_{TMRCLKEXT} \leq f_{SCLK}/4$			25	MHz
$f_{SINCLKPROG}$	Programmed SINC Clock	$f_{SINCLKPROG} \leq f_{SCLK}/4$			20	MHz
$f_{REFCLKEXT}$	External Ethernet MAC Clock	$f_{REFCLKEXT} \leq f_{SCLK}$			50	MHz

[1] Supporting documents may use either SCLK or SYSCLK when referring to system clock frequency.

[2] SCLK is the clock for the system logic. Documentation may interchangeably refer to this clock as SYSCLK, for example, for PLL configuration MMR accesses.

[3] Supporting documents may use either USBCLK or DCLK when referring to USB clock frequency.

[4] USBCLK is the clock for the USB peripheral. Documentation may interchangeably refer to this clock as DCLK, for example, for PLL configuration MMR accesses.

[5] SYS_CLKOUT jitter is dependent on the application system design including pin switching activity, board layout, and the jitter characteristics of the SYS_CLKIN source. Due to the dependency on these factors the measured jitter may be higher or lower than this specification for each end application.

[6] The value in the Typ field is the percentage of the SYS_CLKOUT period.

[7] The maximum achievable frequency for any peripheral in external clock mode is dependent on being able to meet the setup and hold times in the ac timing specifications for that peripheral.

[8] The peripheral external clock frequency must also be less than or equal to f_{SCLK} that clocks the peripheral.

Total Power Dissipation (PD)

Total power dissipation is the sum of power dissipation for each V_{DD} domain, shown in the following equation.

$P_D = P_{D\_INT} + P_{D\_ANA} + P_{D\_EXT}$

where:

$P_{D\_INT} = V_{DD\_INT} \times I_{DD\_INT}$ – *Internal voltage domain power dissipation*

$P_{D\_ANA} = V_{DD\_ANA} \times I_{DD\_ANA}$ – *Analog 3.3 V voltage domain power dissipation*

$P_{D\_EXT} = V_{DD\_EXT} \times I_{DD\_EXT}$ – *Digital 3.3 V voltage domain power dissipation*

Total External Power Dissipation (IDD_EXT)

There are three different items that contribute to the digital 3.3 V supply power dissipation: I/O switching, flash subsystem, and analog subsystem (digital portion), shown in the following equation.

$I_{DDEXT\_TOT} = I_{DDEXT\_IO} + I_{DDEXT\_FLASH} + I_{DDEXT\_ANA}$

where:

$I_{DDEXT\_IO/ANA}$ (mA) = $\Sigma\{V_{DD\_EXT} \times C_L f/2 \times (O \times TR) \times U\}$ – *I/O switching current*

The I/O switching current is the sum of the switching current for all of the enabled peripherals. For each peripheral the capacitive load of each pin in Farads (C_L), operating frequency in MHz (f), number of output pins (O), toggle ratio for each pin (TR), and peripheral utilization (U) are considered.

I_{DDEXT_FLASH} (mA) = 25 mA – *maximum flash subsystem current*

Total Processor Internal Power Dissipation (IDD_INT)

Many operating conditions affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Total internal power dissipation for the processor subsystem has two components:

1. Static, including leakage current
2. Dynamic, due to transistors switching characteristics for each clock domain. Application-dependent currents, clock currents, and data transmission currents all contribute to dynamic power dissipation.

The following equation describes the internal current consumption.

$$I_{DDINT\_TOT} = I_{DDINT\_CCLK\_DYN} + I_{DDINT\_SCLK\_DYN} + I_{DDINT\_DMA\_DR\_DYN} + I_{DDINT\_STATIC}$$

Static Current

I_{DDINT_STATIC} is the current present in the device with all clocks stopped. I_{DDINT_STATIC} is specified as a function of temperature (see Figure 11).

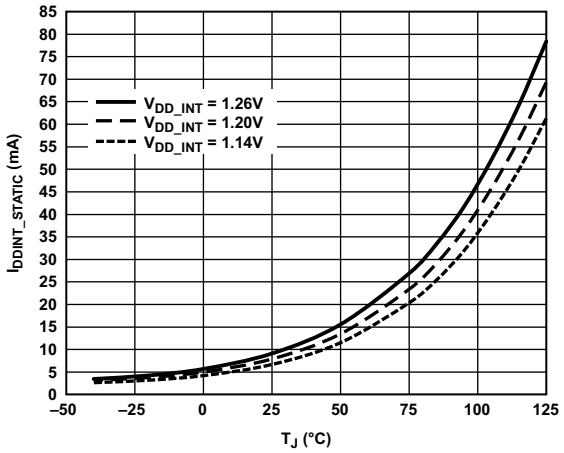

Figure 11. Static Current—I_{DDINT_STATIC} (mA)

Core Clock Application-Dependent Current

Core clock (CCLK) use is subject to an activity scaling factor (ASF) that represents application code running on the processor core and L1 memory (Table 28). The ASF is combined with the CCLK frequency to calculate this portion.

$I_{DDINT\_CCLK\_DYN}$ (mA) = 0.192 × f_{CCLK} (MHz) × *ASF* × V_{DD_INT} (V)

Table 28. Activity Scaling Factors (ASF)

I_{DD_INT} Power Vector	ASF
$I_{DD\text{-}PEAK}$	1.85
$I_{DD\text{-}COREMARK}$ (typical)	1.0
$I_{DD\text{-}IDLE}$	0.31

System Clock Current

The power dissipated by the system clock domain is dependent on operating frequency and a unique scaling factor.

$I_{DDINT\_SCLK\_DYN}$ (mA) = 0.308 × f_{SCLK} (MHz) × V_{DD_INT} (V)

Data Transmission Current

The data transmission current represents the power dissipated when transmitting data. This current is expressed in terms of data rate. The calculation is performed by adding the data rate (MB/s) of each DMA and core driven access to peripherals and L2/external memory. This number is then multiplied by a coefficient. The following equation provides an estimate of all data transmission current.

$I_{DDINT\_DMA\_DR\_DYN}$ (mA) = 0.0475 × *data rate* (MB/s) × V_{DD_INT} (V)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Throughput					ADC0_$V_{IN, 00–11}$, ADC1_$V_{IN, 00–11}$
Conversion Rate			2.63	MSPS	
Acquisition time		150		ns	
AC ACCURACY					ADC0_$V_{IN, 00–11}$, ADC1_$V_{IN, 00–11}$
Characteristic					
ADSP-CM403F/ADSP-CM408F/ ADSP-CM409F					
Signal-to-Noise Ratio (SNR)[1]	80.25	81.25		dB	
Signal-to-(Noise + Distortion) Ratio (SINAD)[1]	80	81		dB	
Total Harmonic Distortion (THD)[1]		–92		dB	
Spurious-Free Dynamic Range (SFDR)[1]		90		dBc	
Dynamic Range	82	83		dB	$V_{IN} = V_{REF}/2$ (dc)
Effective Number of Bits (ENOB)	13.0	13.2		Bits	
ADSP-CM402F/ADSP-CM407F					
Signal-to-Noise Ratio (SNR)[1]	73	74		dB	
Signal-to-(Noise + Distortion) Ratio (SINAD)[1]	72	73		dB	
Total Harmonic Distortion (THD)[1]		–88		dB	
Spurious-Free Dynamic Range (SFDR)[1]		88		dBc	
Dynamic Range	74.5	75.5		dB	$V_{IN} = V_{REF}/2$ (dc)
Effective Number of Bits (ENOB)	11.6	11.8		Bits	
Channel-to-Channel Isolation		–95		dB	Any channel pair referenced on same ADC Selected channel = 1 kHz, unselected channel = 10 kHz
ADC-to-ADC Isolation		–100		dB	Any channel pair referenced on opposite ADC

[1] f_{IN} = 1 kHz, 0 V to 2.5 V input, 2.63 MSPS.

FLASH SPECIFICATIONS

The Flash features include:

- 100,000 ERASE cycles per sector
- 20 years data retention

Flash PROGRAM/ERASE SUSPEND Command

Table 29 lists parameters for the Flash suspend command.

Table 29. Suspend Parameters

Parameter	Condition	Typ	Max	Unit
Erase to Suspend[1]	Sector erase or erase resume to erase suspend	700	–	µs
Program to Suspend[1]	Program resume to program suspend	5	–	µs
Subsector Erase to Suspend[1]	Subsector erase or subsector erase resume to erase suspend	50	–	µs
Suspend Latency[2]	Program	7	–	µs
Suspend Latency[2]	Subsector erase	15	–	µs
Suspend Latency[3]	Erase	15	–	µs

[1] Timing is not internally controlled.
[2] Any read command accepted.
[3] Any command except the following are accepted: sector, subsector, or bulk erase; write status register.

Flash AC Characteristics and Operating Conditions

Table 30 identifies Flash specific operating conditions.

Table 30. AC Characteristics and Operating Conditions

Parameter	Symbol	Min	Typ[1]	Max	Unit
Clock Frequency for All Commands other than Read (SPI-ER, QIO-SPI Protocol), T_J = 105°C	f_C	DC	–	100	MHz
Clock Frequency for All Commands other than Read (SPI-ER, QIO-SPI Protocol), T_J = 125°C	f_C	DC	–	97	MHz
Clock Frequency for Read Commands, T_J = 105°C	f_R	DC	–	50	MHz
Clock Frequency for Read Commands, T_J = 125°C	f_R	DC	–	45	MHz
Page Program Cycle Time (256 bytes)[2]	t_{PP}	–	0.5	5	ms
Page Program Cycle Time (n bytes)[2, 3]	t_{PP}	–	int(n/8) × 0.015	5	ms
Subsector Erase Cycle Time	t_{SSE}	–	0.3	1.5	sec
Sector Erase Cycle Time	t_{SE}	–	0.7	3	sec
Bulk Erase Cycle Time	t_{BE}	–	170	250	sec

[1] Typical values given for T_J = 25°C.
[2] When using the page program command to program consecutive bytes, optimized timings are obtained with one sequence including all the bytes vs. several sequences of only a few bytes (1 < n < 256).
[3] int(A) corresponds to the upper integer part of A. For example int(12/8) = 2, int(32/8) = 4 int(15.3) = 16.

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

Clock and Reset Timing

Table 34 and Figure 24 describe clock and reset operations related to the clock generation unit (CGU) and reset control unit (RCU). Per the CCLK, SCLK, USBCLK, and OCLK timing specifications in Table 27 Clock Related Operating Conditions, combinations of SYS_CLKIN and clock multipliers must not select clock rates in excess of the processor's maximum instruction rate.

Table 34. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
f_{CKIN}	SYS_CLKIN Frequency (Using a Crystal)[1, 2, 3]	20	50	MHz
f_{CKIN}	SYS_CLKIN Frequency (Using a Crystal Oscillator)[1, 2, 3]	20	60	MHz
t_{CKINL}	SYS_CLKIN Low Pulse[1]	6.67		ns
t_{CKINH}	SYS_CLKIN High Pulse[1]	6.67		ns
t_{WRST}	$\overline{\text{SYS\_HWRST}}$ Asserted Pulse Width Low[4]	11 × t_{CKIN}		ns

[1] Applies to PLL bypass mode and PLL nonbypass mode.
[2] The t_{CKIN} period (see Figure 24) equals $1/f_{CKIN}$.
[3] If the CGU_CTL.DF bit is set, the minimum f_{CKIN} specification is 40 MHz.
[4] Applies after power-up sequence is complete. See Table 35 and Figure 25 for power-up reset timing.

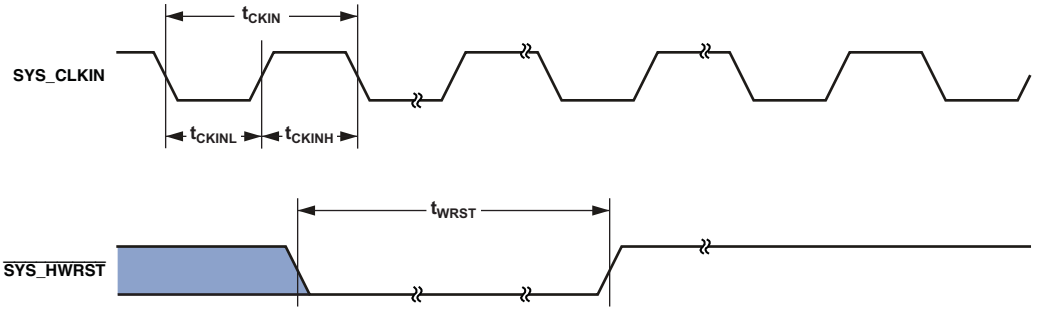

Figure 24. Clock and Reset Timing

Table 46. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data and Data-Valid Enable Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0[1]		14	ns
$t_{DDTENFS}$	Data Enable for MCE = 1, MFD = 0[1]	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified as well as standard serial mode, and MCE = 1, MFD = 0.

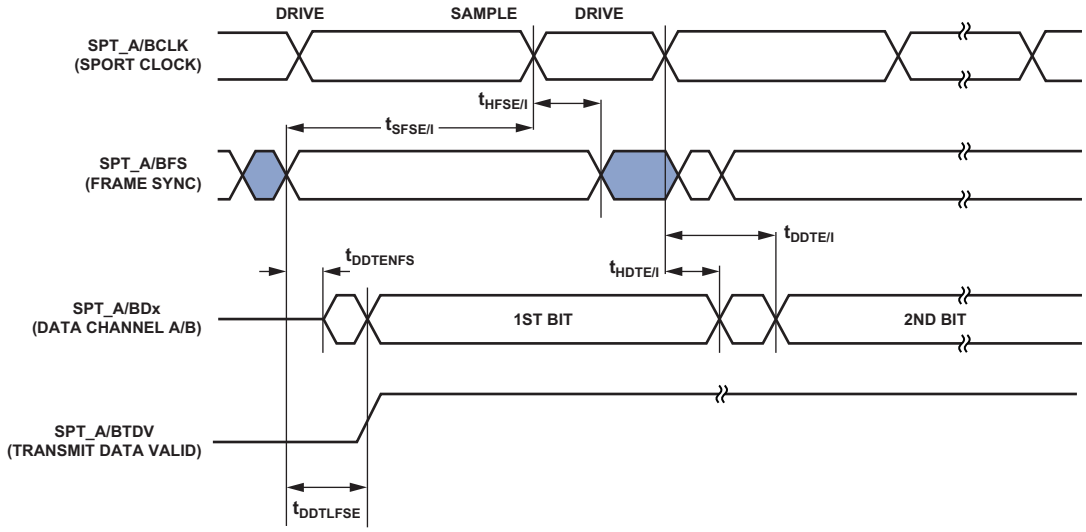

Figure 34. External Late Frame Sync

Serial Peripheral Interface (SPI) Port—Open Drain Mode (ODM) Timing

In Figure 39 and Figure 40, the outputs can be SPI_MOSI, SPI_MISO, SPI_D2, and/or SPI_D3 depending on the mode of operation.

Table 50. SPI Port—ODM Master Mode

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{HDSPIODMM}$	SPI_CLK Edge to High Impedance from Data Out Valid	–1		ns
$t_{DDSPIODMM}$	SPI_CLK Edge to Data Out Valid from High Impedance		6	ns

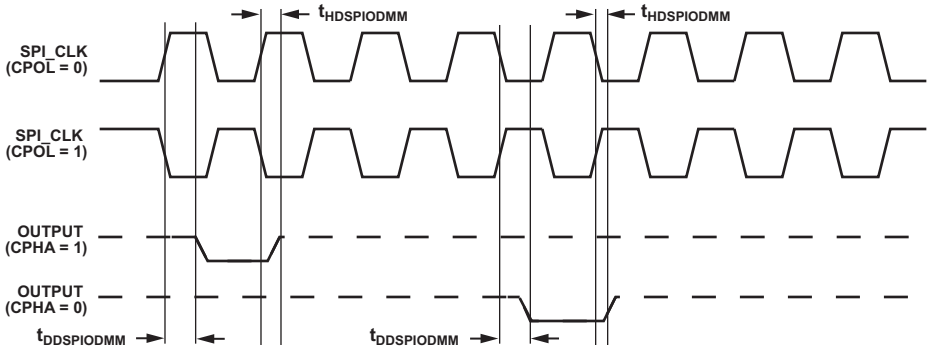

Figure 39. ODM Master

Table 51. SPI Port—ODM Slave Mode

Parameter		Min	Max	Unit
Timing Requirements				
$t_{HDSPIODMS}$	SPI_CLK Edge to High Impedance from Data Out Valid	0		ns
$t_{DDSPIODMS}$	SPI_CLK Edge to Data Out Valid from High Impedance		11	ns

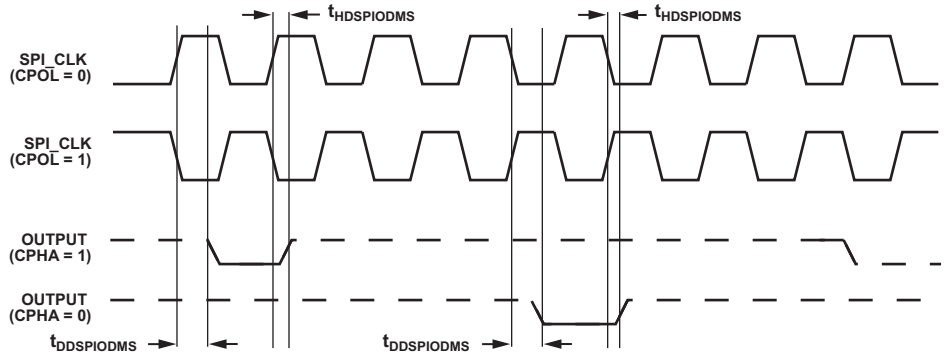

Figure 40. ODM Slave

PROCESSOR TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 59 shows the measurement point for ac measurements (except output enable/disable). The measurement point V_{MEAS} is $V_{DD\_EXT}/2$ for V_{DD_EXT} (nominal) = 3.3 V.

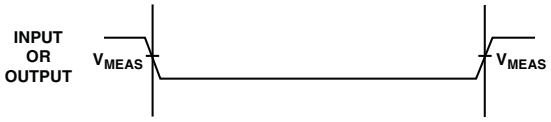

Figure 59. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time, t_{ENA}, is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 60. If multiple pins are enabled, the measurement value is that of the first pin to start driving.

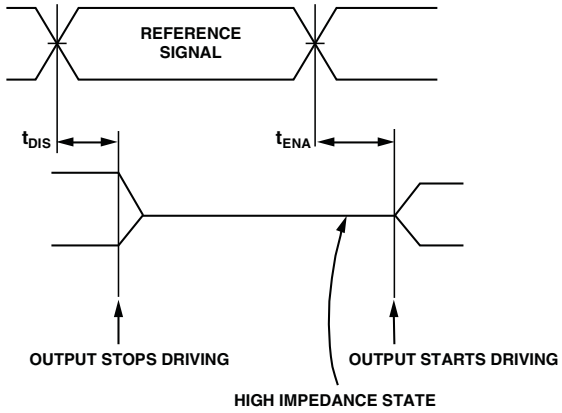

Figure 60. Output Enable/Disable

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time, t_{DIS}, is the interval from when a reference signal reaches a high or low voltage level to the point when the output stops driving as shown on the left side of Figure 60.

OUTPUT DRIVE CURRENTS

Figure 61 and Figure 62 show typical current-voltage characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

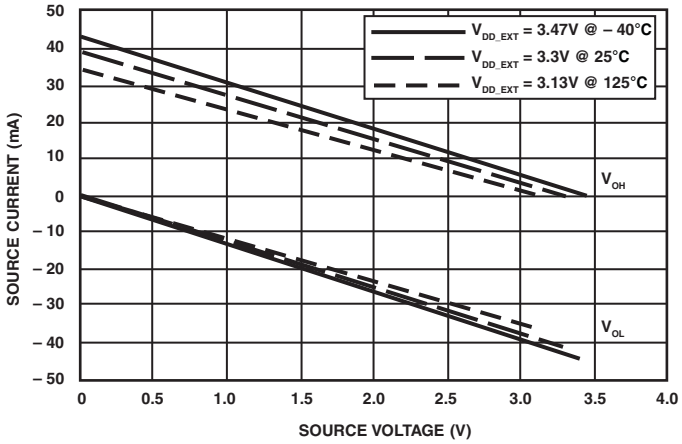

Figure 61. Driver Type A Current

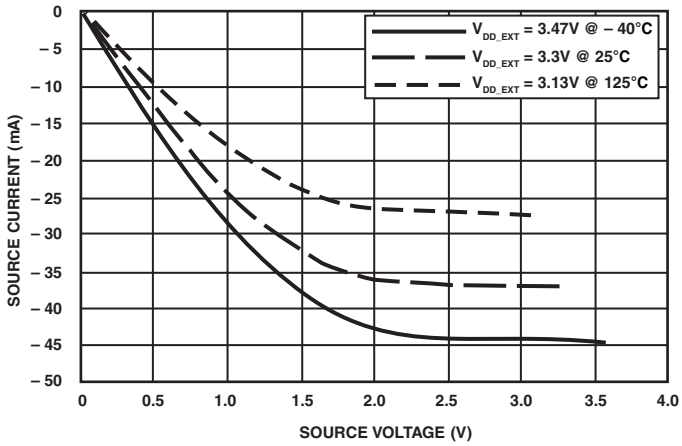

Figure 62. Driver Type B Current

Capacitive Loading

Output delay, hold, enable, and disable times are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 63). V_{LOAD} is equal to $(V_{DD\_EXT})/2$.

Figure 65 shows the top view of the 120-lead LQFP package lead configuration and Figure 66 shows the bottom view of the 120-lead LQFP package lead configuration.

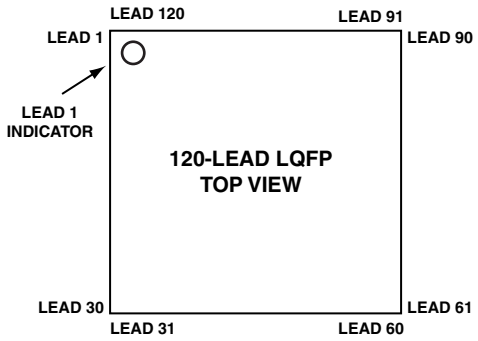

Figure 65. 120-Lead LQFP Lead Configuration (Top View)

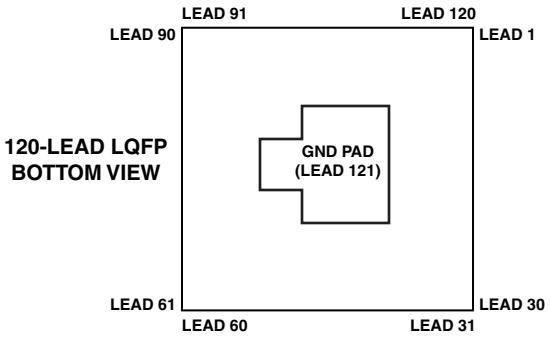

Figure 66. 120-Lead LQFP Lead Configuration (Bottom View)

Table 74. ADSP-CM407F/ADSP-CM408F 176-Lead LQFP Lead Assignments (Alphabetical by Pin Name) (Continued)

Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.
GND_ANA2	124	PC_04	54	PF_01	70	VDD_EXT	125
GND_ANA3	96	PC_05	51	PF_02	69	VDD_EXT	129
GND_VREF0	111	PC_06	52	PF_03	68	VDD_EXT	136
GND_VREF1	109	PC_07	49	PF_04	67	VDD_EXT	137
JTG_TCK/SWCLK	45	PC_08	39	PF_05	61	VDD_EXT	144
JTG_TDI	44	PC_09	40	PF_06	58	VDD_EXT	150
JTG_TDO/SWO	47	PC_10	38	PF_07	59	VDD_EXT	158
JTG_TMS/SWDIO	48	PC_11	10	PF_08	55	VDD_EXT	165
$\overline{\text{JTG\_TRST}}$	46	PC_12	11	PF_09	56	VDD_EXT	172
PA_00	25	PC_13	9	PF_10	53	VDD_INT	22
PA_01	21	PC_14	7	REFCAP	110	VDD_INT	65
PA_02	20	PC_15	5	$\overline{\text{SMC0\_AMS0}}$	147	VDD_INT	94
PA_03	19	PD_00	169	$\overline{\text{SMC0\_ARE}}$	149	VDD_INT	128
PA_04	18	PD_01	166	$\overline{\text{SMC0\_AWE}}$	148	VDD_INT	157
PA_05	17	PD_02	167	SYS_BMODE0	176	VDD_VREG	32
PA_06	16	PD_03	163	SYS_BMODE1	175	VREF0	112
PA_07	14	PD_04	164	SYS_CLKIN	30	VREF1	108
PA_08	13	PD_05	161	SYS_CLKOUT	174	VREG_BASE	31
PA_09	12	PD_06	146	$\overline{\text{SYS\_FAULT}}$	26		
PA_10	6	PD_07	145	$\overline{\text{SYS\_HWRST}}$	27		
PA_11	4	PD_08	142	$\overline{\text{SYS\_NMI}}$	132		

* Pin no. 177 is the GND supply (see Figure 68) for the processor; this pad **must** connect to GND.

Figure 67 shows the top view of the 176-lead LQFP lead configuration and Figure 68 shows the bottom view of the 176-lead LQFP lead configuration.

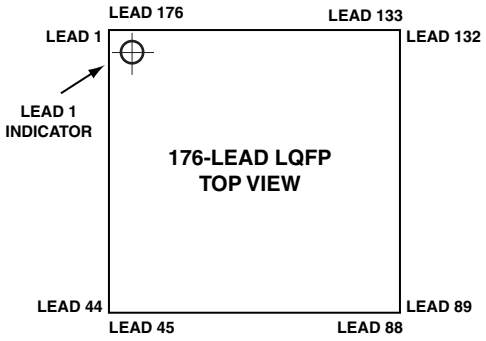

Figure 67. 176-Lead LQFP Lead Configuration (Top View)

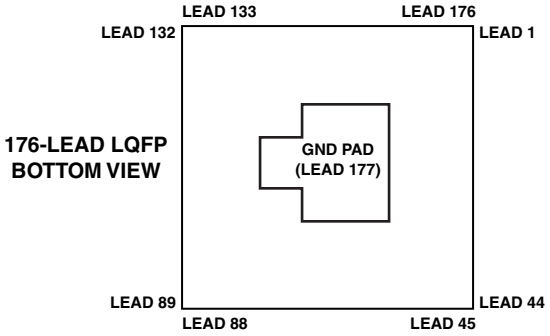

Figure 68. 176-Lead LQFP Lead Configuration (Bottom View)