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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	88
Number of Logic Elements/Cells	880
Total RAM Bits	-
Number of I/O	71
Number of Gates	10000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf6010antc100-3">https://www.e-xfl.com/product-detail/intel/epf6010antc100-3</a>

Table 4 shows FLEX 6000 performance for more complex designs.

<b>Table 4. FLEX 6000 Device Performance for Complex Designs</b> <i>Note (1)</i>					
Application	LEs Used	Performance			Units
		-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
8-bit, 16-tap parallel finite impulse response (FIR) filter	599	94	80	72	MSPS
8-bit, 512-point fast Fourier transform (FFT) function	1,182	75 63	89 53	109 43	μS MHz
16450 universal asynchronous receiver/transmitter (UART)	487	36	30	25	MHz
PCI bus target with zero wait states	609	56	49	42	MHz

**Note:**

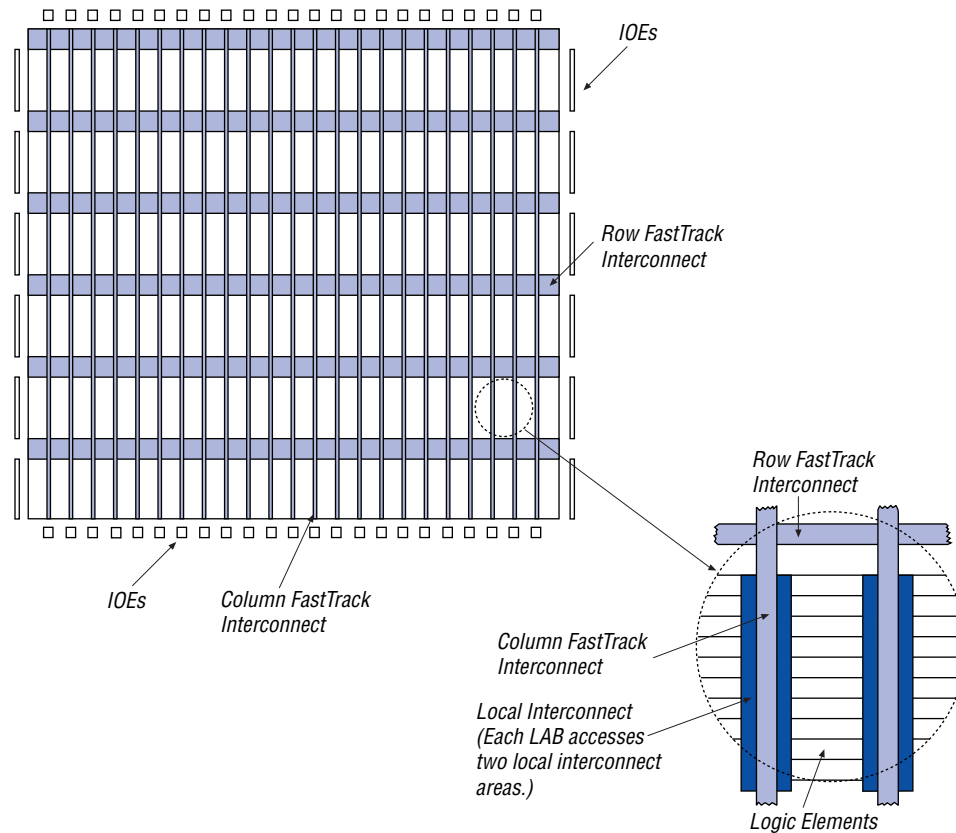
(1) The applications in this table were created using Altera MegaCore™ functions.

FLEX 6000 devices are supported by Altera development systems; a single, integrated package that offers schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development systems include DesignWare functions that are optimized for the FLEX 6000 architecture.

The Altera development system runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800.

f See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet* for more information.

**Figure 1. OptiFLEX Architecture Block Diagram**

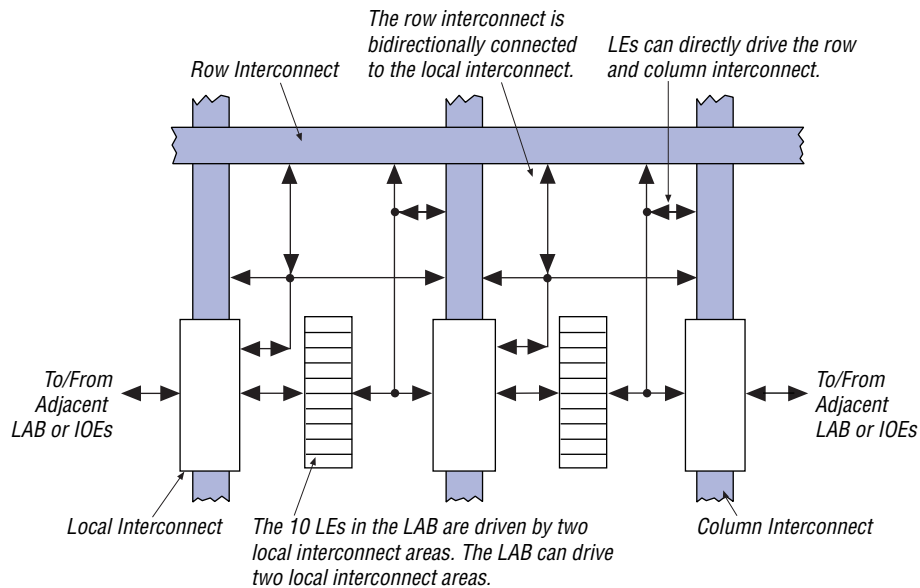
FLEX 6000 devices provide four dedicated, global inputs that drive the control inputs of the flipflops to ensure efficient distribution of high-speed, low-skew control signals. These inputs use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. These inputs can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device. The dedicated global routing structure is built into the device, eliminating the need to create a clock tree.

### Logic Array Block

An LAB consists of ten LEs, their associated carry and cascade chains, the LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 6000 architecture, and facilitates efficient routing with optimum device utilization and high performance.

The interleaved LAB structure—an innovative feature of the FLEX 6000 architecture—allows each LAB to drive two local interconnects. This feature minimizes the use of the FastTrack Interconnect, providing higher performance. An LAB can drive 20 LEs in adjacent LABs via the local interconnect, which maximizes fitting flexibility while minimizing die size. See [Figure 2](#).

**Figure 2. Logic Array Block**



In most designs, the registers only use global clock and clear signals. However, in some cases, other clock or asynchronous clear signals are needed. In addition, counters may also have synchronous clear or load signals. In a design that uses non-global clock and clear signals, inputs from the first LE in an LAB are re-routed to drive the control signals for that LAB. See [Figure 3](#).

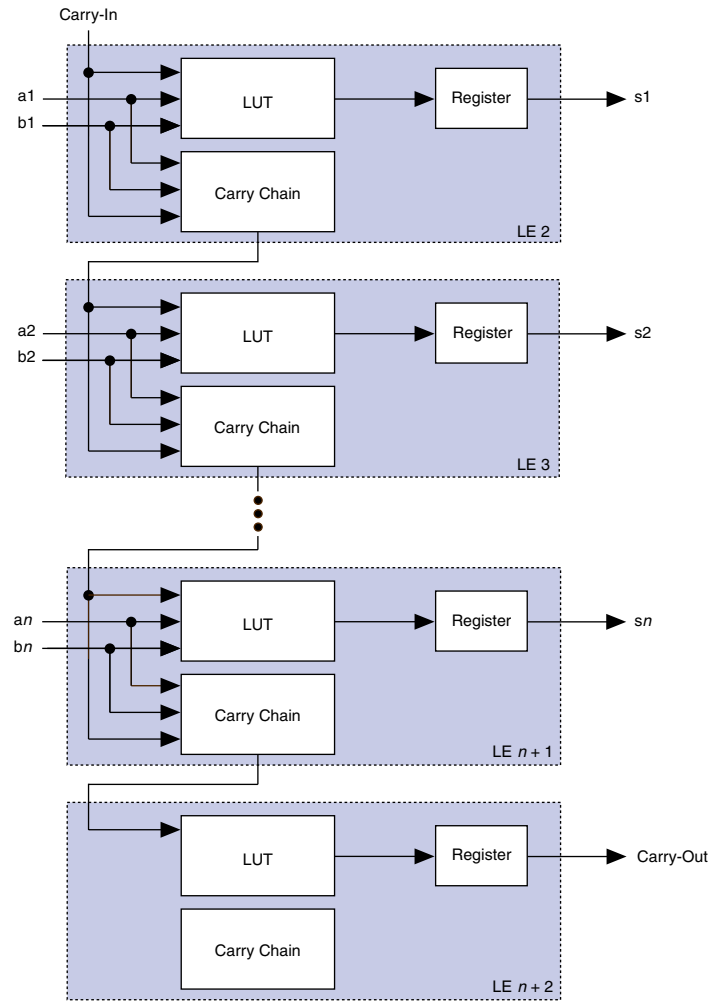
### *Carry Chain*

The carry chain provides a very fast (0.1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 6000 architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Altera software during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

Because the first LE of each LAB can generate control signals for that LAB, the first LE in each LAB is not included in carry chains. In addition, the inputs of the first LE in each LAB may be used to generate synchronous clear and load enable signals for counters implemented with carry chains.

Carry chains longer than nine LEs are implemented automatically by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from an even-numbered LAB to another even-numbered LAB, or from an odd-numbered LAB to another odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the second LE of the third LAB in the row. In addition, the carry chain does not cross the middle of the row. For instance, in the EPF6016 device, the carry chain stops at the 11th LAB in a row and a new carry chain begins at the 12th LAB.

Figure 5 shows how an  $n$ -bit full adder can be implemented in  $n + 1$  LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. Although the register can be bypassed for simple adders, it can be used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the FastTrack Interconnect.

**Figure 5. Carry Chain Operation**

### *Cascade Chain*

The cascade chain enables the FLEX 6000 architecture to implement very wide fan-in functions. Adjacent LUTs can be used to implement portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR gate (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 0.5 ns per LE. Cascade chain logic can be created automatically by the Altera software during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of cascade chains for the appropriate functions.

A cascade chain implementing an AND gate can use the register in the last LE; a cascade chain implementing an OR gate cannot use this register because of the inversion required to implement the OR gate.

Because the first LE of an LAB can generate control signals for that LAB, the first LE in each LAB is not included in cascade chains. Moreover, cascade chains longer than nine bits are automatically implemented by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from an even-numbered LAB to another even-numbered LAB, or from an odd-numbered LAB to another odd-numbered LAB. For example, the last LE of the first LAB in a row cascades to the second LE of the third LAB. The cascade chain does not cross the center of the row. For example, in an EPF6016 device, the cascade chain stops at the 11th LAB in a row and a new cascade chain begins at the 12th LAB.

Figure 6 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. In this example, functions of  $4n$  variables are implemented with  $n$  LEs. The cascade chain requires 3.4 ns to decode a 16-bit address.

**Normal Mode**

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The Altera software automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal.

**Arithmetic Mode**

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a 3-input function; the other generates a carry output. As shown in [Figure 7](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

The Altera software implements logic functions to use the arithmetic mode automatically where appropriate; the designer does not have to decide how the carry chain will be used.

**Counter Mode**

The counter mode offers counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in a LAB use counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. In addition, the Altera software automatically places registers that are not in the counter into other LABs.

The counter mode uses two 3-input LUTs: one generates the counter data and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load will override any signal carried on the cascade chain. The synchronous clear overrides the synchronous load.



A row channel can be driven by an LE or by one of two column channels. These three signals feed a 3-to-1 multiplexer that connects to six specific row channels. Row channels drive into the local interconnect via multiplexers.

Each column of LABs is served by a dedicated column interconnect. The LEs in an LAB can drive the column interconnect. The LEs in an LAB, a column IOE, or a row interconnect can drive the column interconnect. The column interconnect can then drive another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect must be routed to the row interconnect before it can enter an LAB.

Each LE has a FastTrack Interconnect output and a local output. The FastTrack interconnect output can drive six row and two column lines directly; the local output drives the local interconnect. Each local interconnect channel driven by an LE can drive four row and two column channels. This feature provides additional flexibility, because each LE can drive any of ten row lines and four column lines.

In addition, LEs can drive global control signals. This feature is useful for distributing internally generated clock, asynchronous clear, and asynchronous preset signals. A pin-driven global signal can also drive data signals, which is useful for high-fan-out data signals.

Each LAB drives two groups of local interconnects, which allows an LE to drive two LABs, or 20 LEs, via the local interconnect. The row-to-local multiplexers are used more efficiently, because the multiplexers can now drive two LABs. [Figure 10](#) shows how an LAB connects to row and column interconnects.

Table 5 summarizes the FastTrack Interconnect resources available in each FLEX 6000 device.

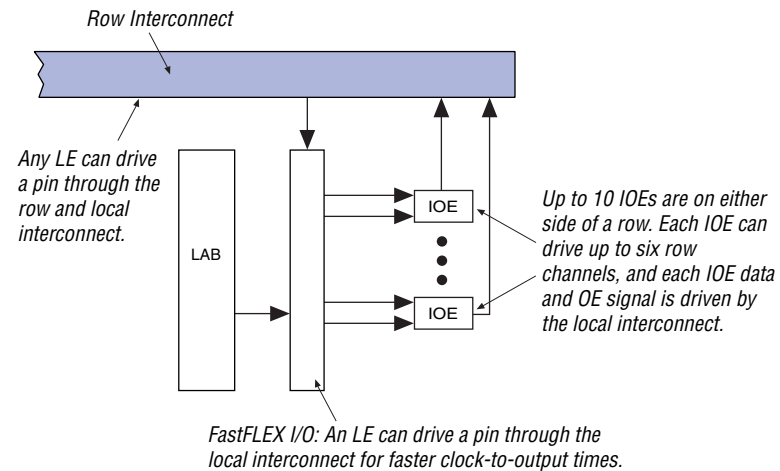
<b>Table 5. FLEX 6000 FastTrack Interconnect Resources</b>				
<b>Device</b>	<b>Rows</b>	<b>Channels per Row</b>	<b>Columns</b>	<b>Channels per Column</b>
EPF6010A	4	144	22	20
EPF6016 EPF6016A	6	144	22	20
EPF6024A	7	186	28	30

In addition to general-purpose I/O pins, FLEX 6000 devices have four dedicated input pins that provide low-skew signal distribution across the device. These four inputs can be used for global clock and asynchronous clear control signals. These signals are available as control signals for all LEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device. Using dedicated inputs to route data signals provides a fast path for high fan-out signals.

The local interconnect from LABs located at either end of two rows can drive a global control signal. For instance, in an EPF6016 device, LABs C1, D1, C22, and D22 can all drive global control signals. When an LE drives a global control signal, the dedicated input pin that drives that signal cannot be used. Any LE in the device can drive a global control signal by driving the FastTrack Interconnect into the appropriate LAB. To minimize delay, however, the Altera software places the driving LE in the appropriate LAB. The LE-driving-global signal feature is optimized for speed for control signals; regular data signals are better routed on the FastTrack Interconnect and do not receive any advantage from being routed on global signals. This LE-driving-global control signal feature is controlled by the designer and is not used automatically by the Altera software. See Figure 11.

Each IOE drives a row or column interconnect when used as an input or bidirectional pin. A row IOE can drive up to six row lines; a column IOE can drive up to two column lines. The input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time. Figure 13 shows how an IOE connects to a row interconnect, and Figure 14 shows how an IOE connects to a column interconnect.

**Figure 13. IOE Connection to Row Interconnect**



## MultiVolt I/O Interface

The FLEX 6000 device architecture supports the MultiVolt I/O interface feature, which allows FLEX 6000 devices to interface with systems of differing supply voltages. The EPF6016 device can be set for 3.3-V or 5.0-V I/O pin operation. This device has one set of  $V_{CC}$  pins for internal operation and input buffers ( $V_{CCINT}$ ), and another set for output drivers ( $V_{CCIO}$ ).

The  $V_{CCINT}$  pins on 5.0-V FLEX 6000 devices must always be connected to a 5.0-V power supply. With a 5.0-V  $V_{CCINT}$  level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The  $V_{CCIO}$  pins on 5.0-V FLEX 6000 devices can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the  $V_{CCIO}$  pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the  $V_{CCIO}$  pins are connected to a 3.3-V power supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with  $V_{CCIO}$  levels lower than 4.75 V incur a nominally greater timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ .

On 3.3-V FLEX 6000 devices, the  $V_{CCINT}$  pins must be connected to a 3.3-V power supply. Additionally, 3.3-V FLEX 6000A devices can interface with 2.5-V, 3.3-V, or 5.0-V systems when the  $V_{CCIO}$  pins are tied to 2.5 V. The output can drive 2.5-V systems, and the inputs can be driven by 2.5-V, 3.3-V, or 5.0-V systems. When the  $V_{CCIO}$  pins are tied to 3.3 V, the output can drive 3.3-V or 5.0-V systems. MultiVolt I/Os are not supported on 100-pin TQFP or 100-pin FineLine BGA packages.

Table 7 describes FLEX 6000 MultiVolt I/O support.

<b>Table 7. FLEX 6000 MultiVolt I/O Support</b>							
<b><math>V_{CCINT}</math> (V)</b>	<b><math>V_{CCIO}</math> (V)</b>	<b>Input Signal (V)</b>			<b>Output Signal (V)</b>		
		<b>2.5</b>	<b>3.3</b>	<b>5.0</b>	<b>2.5</b>	<b>3.3</b>	<b>5.0</b>
3.3	2.5	v	v	v	v		
3.3	3.3	v	v	v	v (1)	v	v
5.0	3.3		v	v		v	v
5.0	5.0		v	v			v

**Note:**

- (1) When  $V_{CCIO} = 3.3$  V, a FLEX 6000 device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V or 3.3-V FLEX 6000 devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a  $V_{IH}$  of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The  $I_{OL}$  current specification should be considered when selecting a pull-up resistor.

Output pins on 5.0-V FLEX 6000 devices with  $V_{CCIO} = 3.3$  V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

### Power Sequencing & Hot-Socketing

Because FLEX 6000 family devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The  $V_{CCIO}$  and  $V_{CCINT}$  power planes can be powered in any order.

Signals can be driven into 3.3-V FLEX 6000 devices before and during power up without damaging the device. Additionally, FLEX 6000 devices do not drive out during power up. Once operating conditions are reached, FLEX 6000 devices operate as specified by the user.

### IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 6000 devices provide JTAG BST circuitry that comply with the IEEE Std. 1149.1-1990 specification. [Table 8](#) shows JTAG instructions for FLEX 6000 devices. JTAG BST can be performed before or after configuration, but not during configuration (except when you disable JTAG support in user mode).

- 1 See [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#) for more information on JTAG BST circuitry.

**Table 8. FLEX 6000 JTAG Instructions**

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test result at the input pins.
BYPASS	Places the 1-bit bypass register between the $TDI$ and $TDO$ pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.

**Table 10. JTAG Timing Parameters & Values**

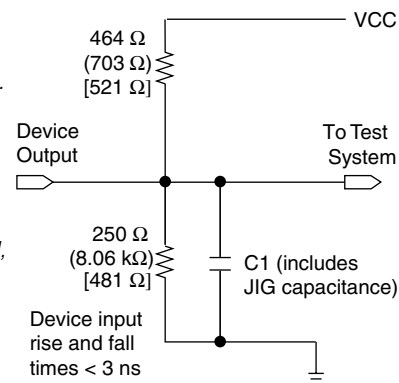
Symbol	Parameter	Min	Max	Unit
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock-to-output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock-to-output		35	ns
$t_{JSZX}$	Update register high impedance to valid output		35	ns
$t_{JSXZ}$	Update register valid output to high impedance		35	ns

## Generic Testing

Each FLEX 6000 device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 6000 devices are made under conditions equivalent to those shown in [Figure 17](#). Multiple test patterns can be used to configure devices during all stages of the production flow.

**Figure 17. AC Test Conditions**

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers without parentheses are for 5.0-V devices or outputs. Numbers in parentheses are for 3.3-V devices or outputs. Numbers in brackets are for 2.5-V devices or outputs.



**Table 13. FLEX 6000 5.0-V Device DC Operating Conditions** Notes (5), (6)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	High-level input voltage		2.0		$V_{CCINT} + 0.5$	V
$V_{IL}$	Low-level input voltage		-0.5		0.8	V
$V_{OH}$	5.0-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 4.75$ V (7)	2.4			V
	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (7)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (7)	$V_{CCIO} - 0.2$			V
$V_{OL}$	5.0-V low-level TTL output voltage	$I_{OL} = 8$ mA DC, $V_{CCIO} = 4.75$ V (8)			0.45	V
	3.3-V low-level TTL output voltage	$I_{OL} = 8$ mA DC, $V_{CCIO} = 3.00$ V (8)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (8)			0.2	V
$I_I$	Input pin leakage current	$V_I = V_{CC}$ or ground (8)	-10		10	$\mu$ A
$I_{OZ}$	Tri-stated I/O pin leakage current	$V_O = V_{CC}$ or ground (8)	-40		40	$\mu$ A
$I_{CC0}$	$V_{CC}$ supply current (standby)	$V_I =$ ground, no load		0.5	5	mA

**Table 14. FLEX 6000 5.0-V Device Capacitance** Note (9)

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance for I/O pin	$V_{IN} = 0$ V, $f = 1.0$ MHz		8	pF
$C_{INCLK}$	Input capacitance for dedicated input	$V_{IN} = 0$ V, $f = 1.0$ MHz		12	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		8	pF

**Notes to tables:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum  $V_{CC}$  rise time to 100 ms.  $V_{CC}$  must rise monotonically.
- (5) Typical values are for  $T_A = 25^\circ$  C and  $V_{CC} = 5.0$  V.
- (6) These values are specified under the FLEX 6000 Recommended Operating Conditions shown in Table 12 on page 31.
- (7) The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current.
- (8) The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (9) Capacitance is sample-tested only.

## Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row can be calculated by adding the following parameters:

- LE register clock-to-output delay ( $t_{CO} + t_{REG\_TO\_OUT}$ )
- Routing delay ( $t_{ROW} + t_{LOCAL}$ )
- LE LUT delay ( $t_{DATA\_TO\_REG}$ )
- LE register setup time ( $t_{SU}$ )

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

Timing simulation and delay prediction are available with the Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 19 shows the overall timing model, which maps the possible routing paths to and from the various elements of the FLEX 6000 device.



Tables 19 through 21 describe the FLEX 6000 internal timing microparameters, which are expressed as worst-case values. Using hand calculations, these parameters can be used to estimate design performance. However, before committing designs to silicon, actual worst-case performance should be modeled using timing simulation and timing analysis. Tables 22 and 23 describe FLEX 6000 external timing parameters.

<b>Table 19. LE Timing Microparameters</b> <i>Note (1)</i>		
<b>Symbol</b>	<b>Parameter</b>	<b>Conditions</b>
$t_{REG\_TO\_REG}$	LUT delay for LE register feedback in carry chain	
$t_{CASC\_TO\_REG}$	Cascade-in to register delay	
$t_{CARRY\_TO\_REG}$	Carry-in to register delay	
$t_{DATA\_TO\_REG}$	LE input to register delay	
$t_{CASC\_TO\_OUT}$	Cascade-in to LE output delay	
$t_{CARRY\_TO\_OUT}$	Carry-in to LE output delay	
$t_{DATA\_TO\_OUT}$	LE input to LE output delay	
$t_{REG\_TO\_OUT}$	Register output to LE output delay	
$t_{SU}$	LE register setup time before clock; LE register recovery time after asynchronous clear	
$t_H$	LE register hold time after clock	
$t_{CO}$	LE register clock-to-output delay	
$t_{CLR}$	LE register clear delay	
$t_C$	LE register control signal delay	
$t_{LD\_CLR}$	Synchronous load or clear delay in counter mode	
$t_{CARRY\_TO\_CARRY}$	Carry-in to carry-out delay	
$t_{REG\_TO\_CARRY}$	Register output to carry-out delay	
$t_{DATA\_TO\_CARRY}$	LE input to carry-out delay	
$t_{CARRY\_TO\_CASC}$	Carry-in to cascade-out delay	
$t_{CASC\_TO\_CASC}$	Cascade-in to cascade-out delay	
$t_{REG\_TO\_CASC}$	Register-out to cascade-out delay	
$t_{DATA\_TO\_CASC}$	LE input to cascade-out delay	
$t_{CH}$	LE register clock high time	
$t_{CL}$	LE register clock low time	

**Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 2 of 2)**

Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 2 of 2)							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{CO}$		0.3		0.4		0.4	ns
$t_{CLR}$		0.4		0.4		0.5	ns
$t_C$		1.8		2.1		2.6	ns
$t_{LD\_CLR}$		1.8		2.1		2.6	ns
$t_{CARRY\_TO\_CARRY}$		0.1		0.1		0.1	ns
$t_{REG\_TO\_CARRY}$		1.6		1.9		2.3	ns
$t_{DATA\_TO\_CARRY}$		2.1		2.5		3.0	ns
$t_{CARRY\_TO\_CASC}$		1.0		1.1		1.4	ns
$t_{CASC\_TO\_CASC}$		0.5		0.6		0.7	ns
$t_{REG\_TO\_CASC}$		1.4		1.7		2.1	ns
$t_{DATA\_TO\_CASC}$		1.1		1.2		1.5	ns
$t_{CH}$	2.5		3.0		3.5		ns
$t_{CL}$	2.5		3.0		3.5		ns

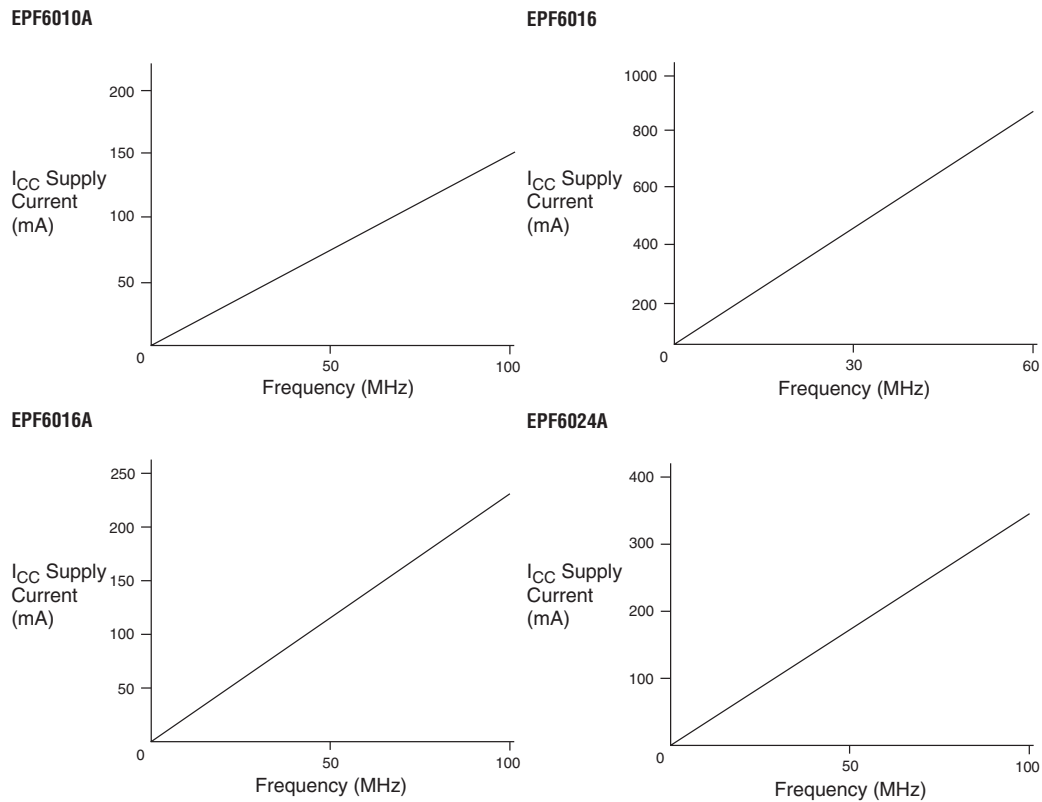
**Table 25. IOE Timing Microparameters for EPF6010A & EPF6016A Devices**

Table 25. IOE Timing Microparameters for EPF6010A & EPF6016A Devices							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{OD1}$		1.9		2.2		2.7	ns
$t_{OD2}$		4.1		4.8		5.8	ns
$t_{OD3}$		5.8		6.8		8.3	ns
$t_{XZ}$		1.4		1.7		2.1	ns
$t_{XZ1}$		1.4		1.7		2.1	ns
$t_{XZ2}$		3.6		4.3		5.2	ns
$t_{XZ3}$		5.3		6.3		7.7	ns
$t_{IOE}$		0.5		0.6		0.7	ns
$t_{IN}$		3.6		4.1		5.1	ns
$t_{IN\_DELAY}$		4.8		5.4		6.7	ns

Tables 29 through 33 show the timing information for EPF6016 devices.

Table 29. LE Timing Microparameters for EPF6016 Devices					
Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
$t_{REG\_TO\_REG}$		2.2		2.8	ns
$t_{CASC\_TO\_REG}$		0.9		1.2	ns
$t_{CARRY\_TO\_REG}$		1.6		2.1	ns
$t_{DATA\_TO\_REG}$		2.4		3.0	ns
$t_{CASC\_TO\_OUT}$		1.3		1.7	ns
$t_{CARRY\_TO\_OUT}$		2.4		3.0	ns
$t_{DATA\_TO\_OUT}$		2.7		3.4	ns
$t_{REG\_TO\_OUT}$		0.3		0.5	ns
$t_{SU}$	1.1		1.6		ns
$t_H$	1.8		2.3		ns
$t_{CO}$		0.3		0.4	ns
$t_{CLR}$		0.5		0.6	ns
$t_C$		1.2		1.5	ns
$t_{LD\_CLR}$		1.2		1.5	ns
$t_{CARRY\_TO\_CARRY}$		0.2		0.4	ns
$t_{REG\_TO\_CARRY}$		0.8		1.1	ns
$t_{DATA\_TO\_CARRY}$		1.7		2.2	ns
$t_{CARRY\_TO\_CASC}$		1.7		2.2	ns
$t_{CASC\_TO\_CASC}$		0.9		1.2	ns
$t_{REG\_TO\_CASC}$		1.6		2.0	ns
$t_{DATA\_TO\_CASC}$		1.7		2.1	ns
$t_{CH}$	4.0		4.0		ns
$t_{CL}$	4.0		4.0		ns

Table 30. IOE Timing Microparameters for EPF6016 Devices					
Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
$t_{OD1}$		2.3		2.8	ns
$t_{OD2}$		4.6		5.1	ns

**Figure 20.  $I_{CCACTIVE}$  vs. Operating Frequency**

## Device Configuration & Operation

The FLEX 6000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.

- f** See [Application Note 116 \(Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices\)](#) for detailed information on configuring FLEX 6000 devices, including sample schematics, timing diagrams, configuration options, pins names, and timing parameters.

## Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.