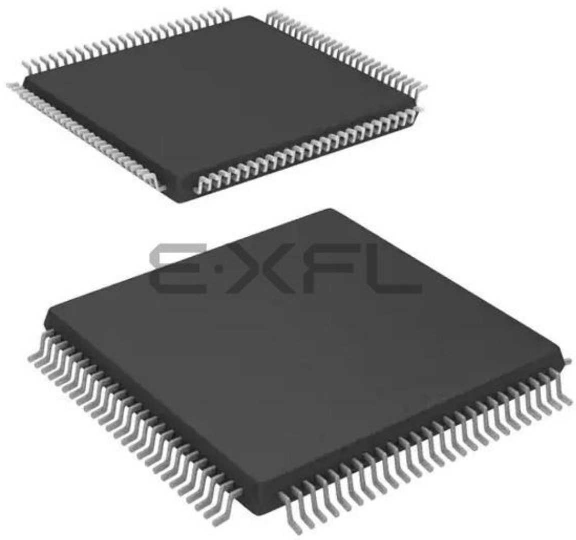

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

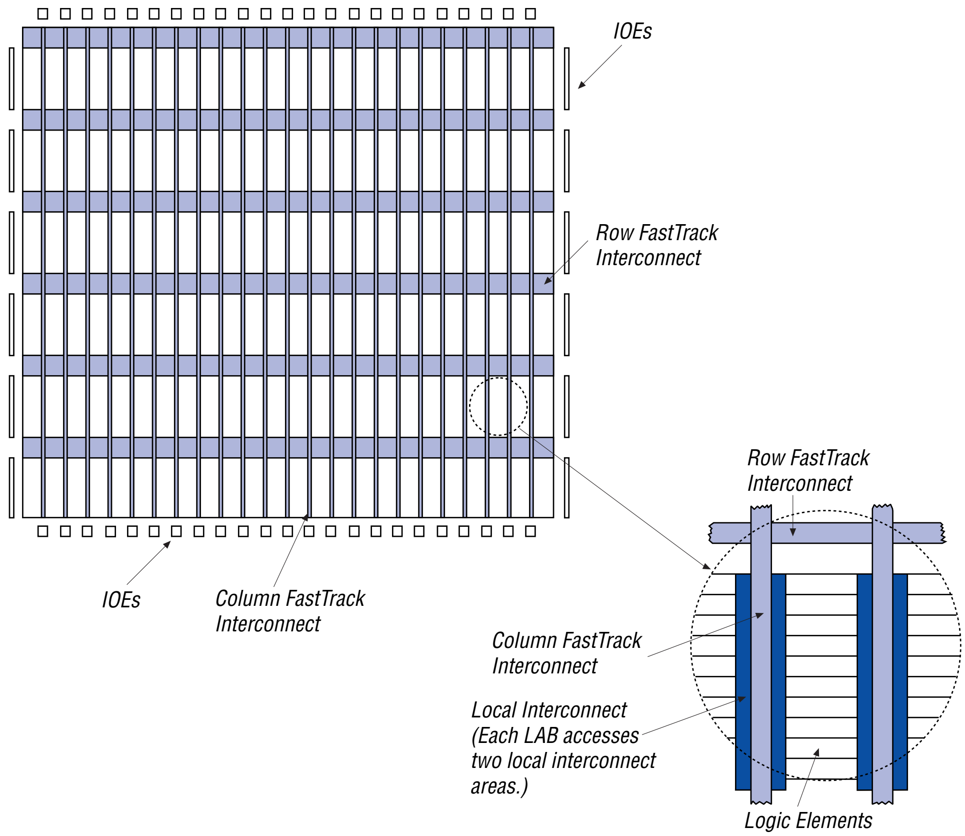
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	88
Number of Logic Elements/Cells	880
Total RAM Bits	-
Number of I/O	71
Number of Gates	10000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf6010atc100-3n

Figure 1. OptiFLEX Architecture Block Diagram



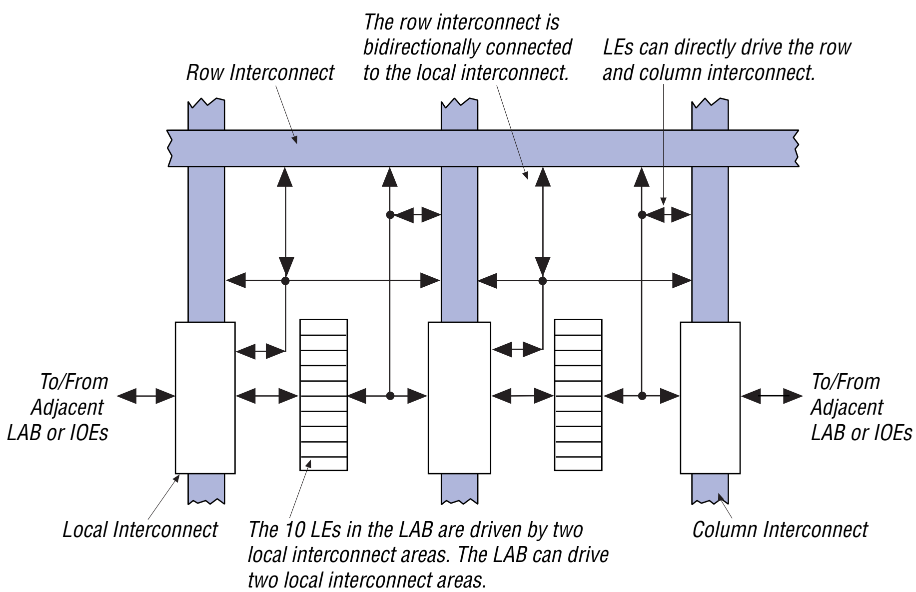
FLEX 6000 devices provide four dedicated, global inputs that drive the control inputs of the flipflops to ensure efficient distribution of high-speed, low-skew control signals. These inputs use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. These inputs can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device. The dedicated global routing structure is built into the device, eliminating the need to create a clock tree.

Logic Array Block

An LAB consists of ten LEs, their associated carry and cascade chains, the LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 6000 architecture, and facilitates efficient routing with optimum device utilization and high performance.

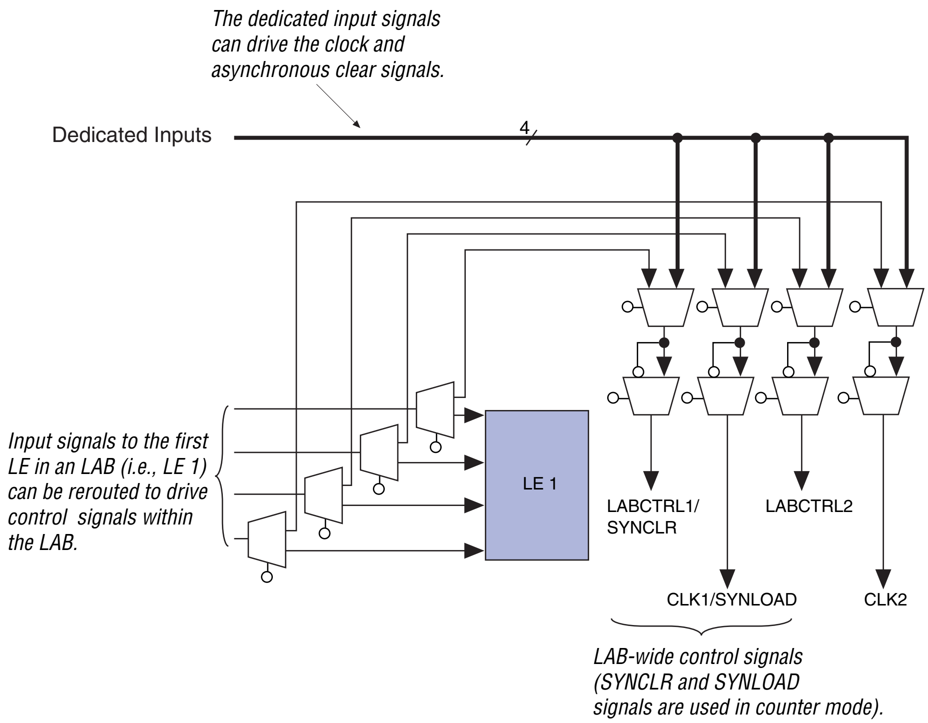
The interleaved LAB structure—an innovative feature of the FLEX 6000 architecture—allows each LAB to drive two local interconnects. This feature minimizes the use of the FastTrack Interconnect, providing higher performance. An LAB can drive 20 LEs in adjacent LABs via the local interconnect, which maximizes fitting flexibility while minimizing die size. See Figure 2.

Figure 2. Logic Array Block



In most designs, the registers only use global clock and clear signals. However, in some cases, other clock or asynchronous clear signals are needed. In addition, counters may also have synchronous clear or load signals. In a design that uses non-global clock and clear signals, inputs from the first LE in an LAB are re-routed to drive the control signals for that LAB. See Figure 3.

Figure 3. LAB Control Signals



Logic Element

An LE, the smallest unit of logic in the FLEX 6000 architecture, has a compact size that provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. An LE contains a programmable flipflop, carry and cascade chains. Additionally, each LE drives both the local and the FastTrack Interconnect. See Figure 4.

Carry Chain

The carry chain provides a very fast (0.1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 6000 architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Altera software during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

Because the first LE of each LAB can generate control signals for that LAB, the first LE in each LAB is not included in carry chains. In addition, the inputs of the first LE in each LAB may be used to generate synchronous clear and load enable signals for counters implemented with carry chains.

Carry chains longer than nine LEs are implemented automatically by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from an even-numbered LAB to another even-numbered LAB, or from an odd-numbered LAB to another odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the second LE of the third LAB in the row. In addition, the carry chain does not cross the middle of the row. For instance, in the EPF6016 device, the carry chain stops at the 11th LAB in a row and a new carry chain begins at the 12th LAB.

Figure 5 shows how an n-bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. Although the register can be bypassed for simple adders, it can be used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the FastTrack Interconnect.

A row channel can be driven by an LE or by one of two column channels. These three signals feed a 3-to-1 multiplexer that connects to six specific row channels. Row channels drive into the local interconnect via multiplexers.

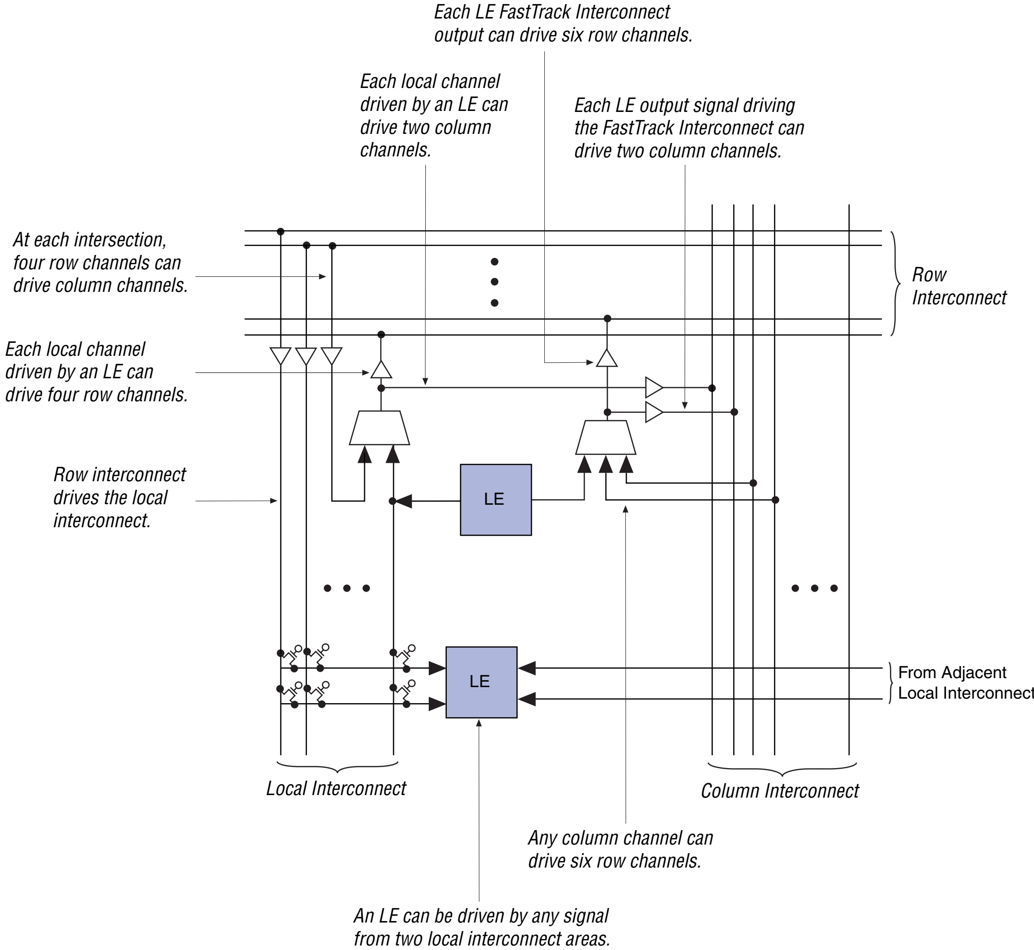
Each column of LABs is served by a dedicated column interconnect. The LEs in an LAB can drive the column interconnect. The LEs in an LAB, a column IOE, or a row interconnect can drive the column interconnect. The column interconnect can then drive another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect must be routed to the row interconnect before it can enter an LAB.

Each LE has a FastTrack Interconnect output and a local output. The FastTrack interconnect output can drive six row and two column lines directly; the local output drives the local interconnect. Each local interconnect channel driven by an LE can drive four row and two column channels. This feature provides additional flexibility, because each LE can drive any of ten row lines and four column lines.

In addition, LEs can drive global control signals. This feature is useful for distributing internally generated clock, asynchronous clear, and asynchronous preset signals. A pin-driven global signal can also drive data signals, which is useful for high-fan-out data signals.

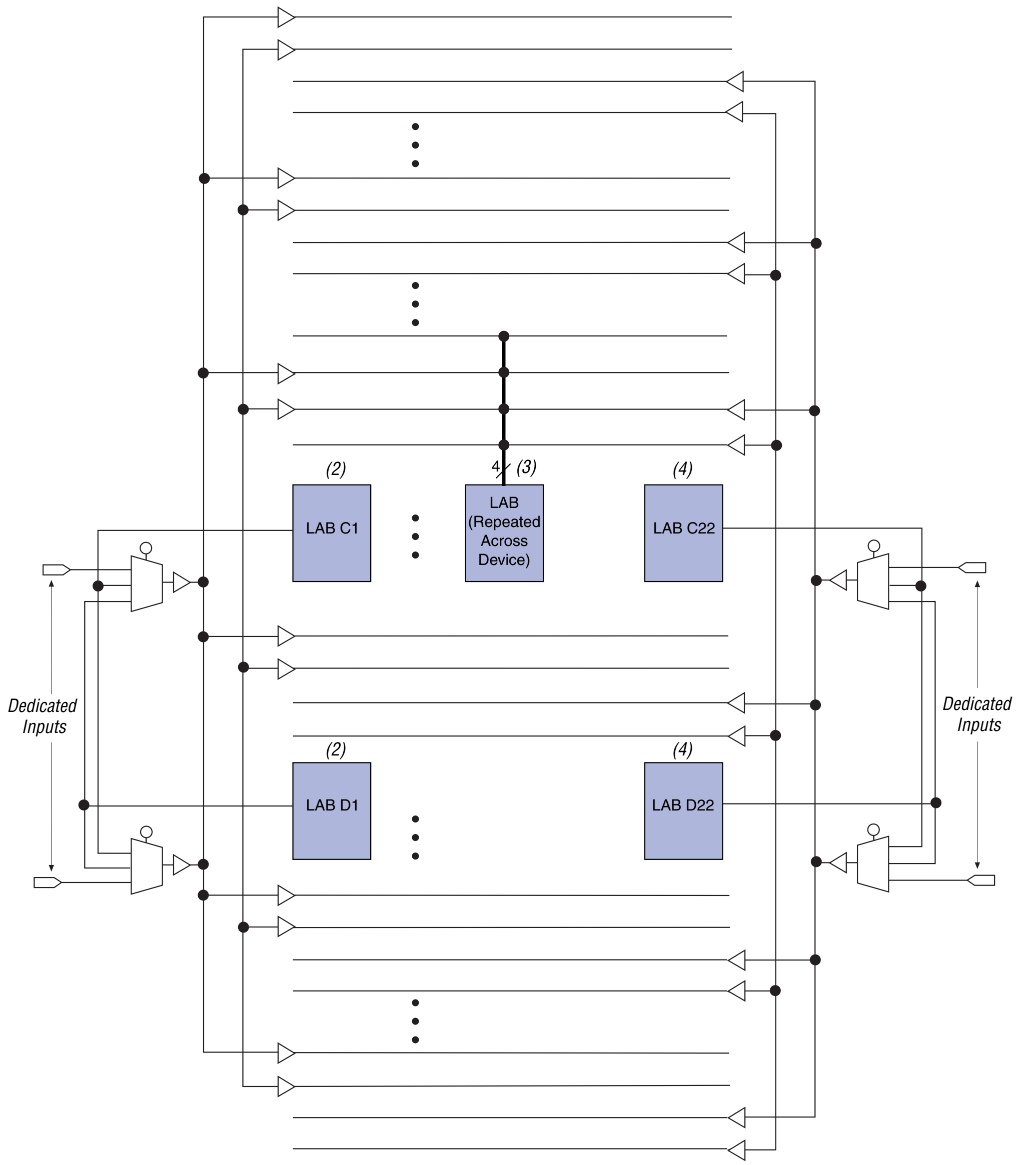
Each LAB drives two groups of local interconnects, which allows an LE to drive two LABs, or 20 LEs, via the local interconnect. The row-to-local multiplexers are used more efficiently, because the multiplexers can now drive two LABs. Figure 10 shows how an LAB connects to row and column interconnects.

Figure 10. LAB Connections to Row & Column Interconnects



For improved routability, the row interconnect consists of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-length channel, which saves the other half of the channel for the other half of the row. One-third of the row channels are half-length channels.

Figure 11. Global Clock & Clear Distribution *Note (1)*



Notes:

(1) The global clock and clear distribution signals are shown for EPF6016 and EPF6016A devices. In EPF6010A devices, LABs in rows B and C drive global signals. In EPF6024A devices, LABs in rows C and E drive global signals.
(2) The local interconnect from LABs C1 and D1 can drive two global control signals on the left side.
(3) Global signals drive into every LAB as clock, asynchronous clear, preset, and data signals.
(4) The local interconnect from LABs C22 and D22 can drive two global control signals on the right side.

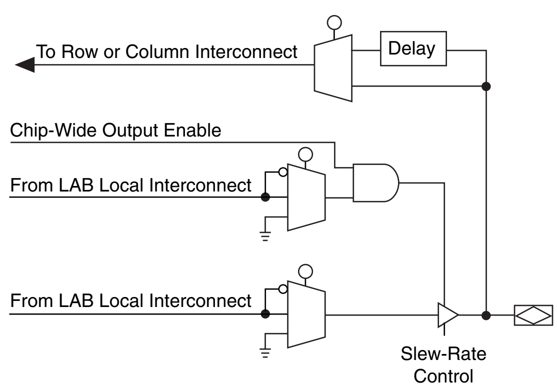
I/O Elements

An IOE contains a bidirectional I/O buffer and a tri-state buffer. IOEs can be used as input, output, or bidirectional pins. An IOE receives its data signals from the adjacent local interconnect, which can be driven by a row or column interconnect (allowing any LE in the device to drive the IOE) or by an adjacent LE (allowing fast clock-to-output delays). A FastFLEX™ I/O pin is a row or column output pin that receives its data signals from the adjacent local interconnect driven by an adjacent LE. The IOE receives its output enable signal through the same path, allowing individual output enables for every pin and permitting emulation of open-drain buffers. The Altera Compiler uses programmable inversion to invert the data or output enable signals automatically where appropriate. Open-drain emulation is provided by driving the data input low and toggling the OE of each IOE. This emulation is possible because there is one OE per pin.

A chip-wide output enable feature allows the designer to disable all pins of the device by asserting one pin (DEV_OE). This feature is useful during board debugging or testing.

Figure 12 shows the IOE block diagram.

Figure 12. IOE Block Diagram



Each IOE drives a row or column interconnect when used as an input or bidirectional pin. A row IOE can drive up to six row lines; a column IOE can drive up to two column lines. The input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time. Figure 13 shows how an IOE connects to a row interconnect, and Figure 14 shows how an IOE connects to a column interconnect.

Figure 13. IOE Connection to Row Interconnect

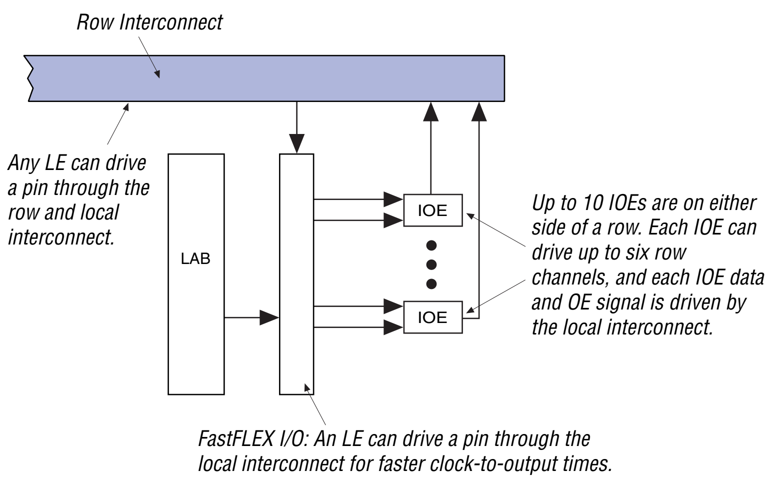
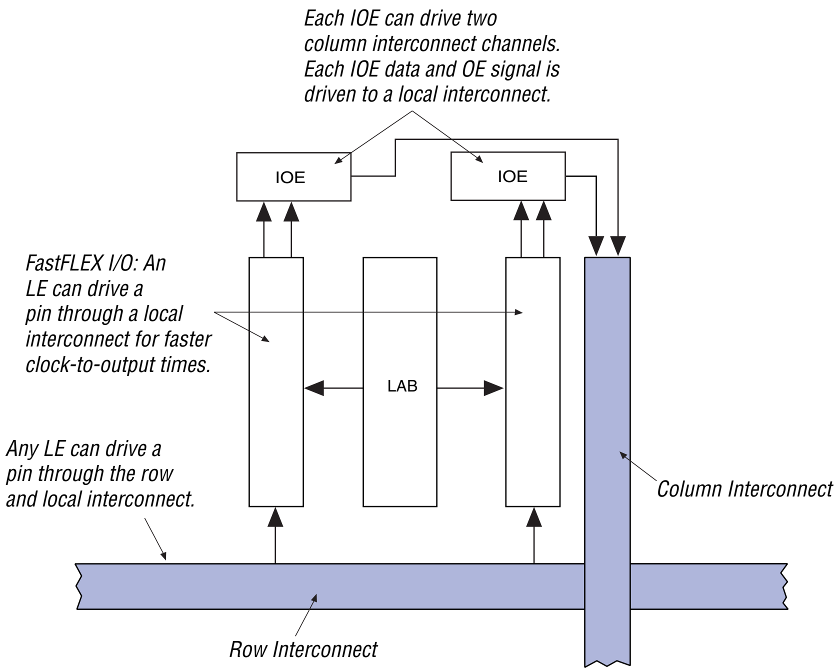


Figure 14. IOE Connection to Column Interconnect



SameFrame Pin-Outs

3.3-V FLEX 6000 devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support an EPF6016A device in a 100-pin FineLine BGA package or an EPF6024A device in a 256-pin FineLine BGA package.

The Altera software packages provide support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software packages generate pin-outs describing how to lay out a board to take advantage of this migration (see Figure 15).

Open-drain output pins on 5.0-V or 3.3-V FLEX 6000 devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Output pins on 5.0-V FLEX 6000 devices with V_{CCIO} = 3.3 V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

Power Sequencing & Hot-Socketing

Because FLEX 6000 family devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into 3.3-V FLEX 6000 devices before and during power up without damaging the device. Additionally, FLEX 6000 devices do not drive out during power up. Once operating conditions are reached, FLEX 6000 devices operate as specified by the user.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 6000 devices provide JTAG BST circuitry that comply with the IEEE Std. 1149.1-1990 specification. Table 8 shows JTAG instructions for FLEX 6000 devices. JTAG BST can be performed before or after configuration, but not during configuration (except when you disable JTAG support in user mode).

1 See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG BST circuitry.

Table 8. FLEX 6000 JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test result at the input pins.
BYPASS	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.

Table 17. FLEX 6000 3.3-V Device DC Operating Conditions *Notes (5), (6)*						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{IH}	High-level input voltage		1.7		5.75	V
V_{IL}	Low-level input voltage		–0.5		0.8	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –8 mA DC, V_{CCIO} = 3.00 V *(7)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(7)*	V_{CCIO} – 0.2			V
	2.5-V high-level output voltage	I_{OH} = –100 µA DC, V_{CCIO} = 2.30 V *(7)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(7)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(7)*	1.7			V
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 8 mA DC, V_{CCIO} = 3.00 V *(8)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(8)*			0.2	V
	2.5-V low-level output voltage	I_{OL} = 100 µA DC, V_{CCIO} = 2.30 V *(8)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(8)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(8)*			0.7	V
I_I	Input pin leakage current	V_I = 5.3 V to ground *(8)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 5.3 V to ground *(8)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.5	5	mA

Table 18. FLEX 6000 3.3-V Device Capacitance *Note (9)*					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
C_{IN}	Input capacitance for I/O pin	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance for dedicated input	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) The minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
(5) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.
(6) These values are specified under Table 16 on page 33.
(7) The I_{OH} parameter refers to high-level TTL or CMOS output current.
(8) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(9) Capacitance is sample-tested only.

Figure 18 shows the typical output drive characteristics of 5.0-V and 3.3-V FLEX 6000 devices with 5.0-V, 3.3-V, and 2.5-V V_{CCIO}. When V_{CCIO} = 5.0 V on EPF6016 devices, the output driver is compliant with the ***PCI Local Bus Specification*, *Revision 2.2*** for 5.0-V operation. When V_{CCIO} = 3.3 V on the EPF6010A and EPF6016A devices, the output driver is compliant with the ***PCI Local Bus Specification*, *Revision 2.2*** for 3.3-V operation.

Figure 18. Output Drive Characteristics

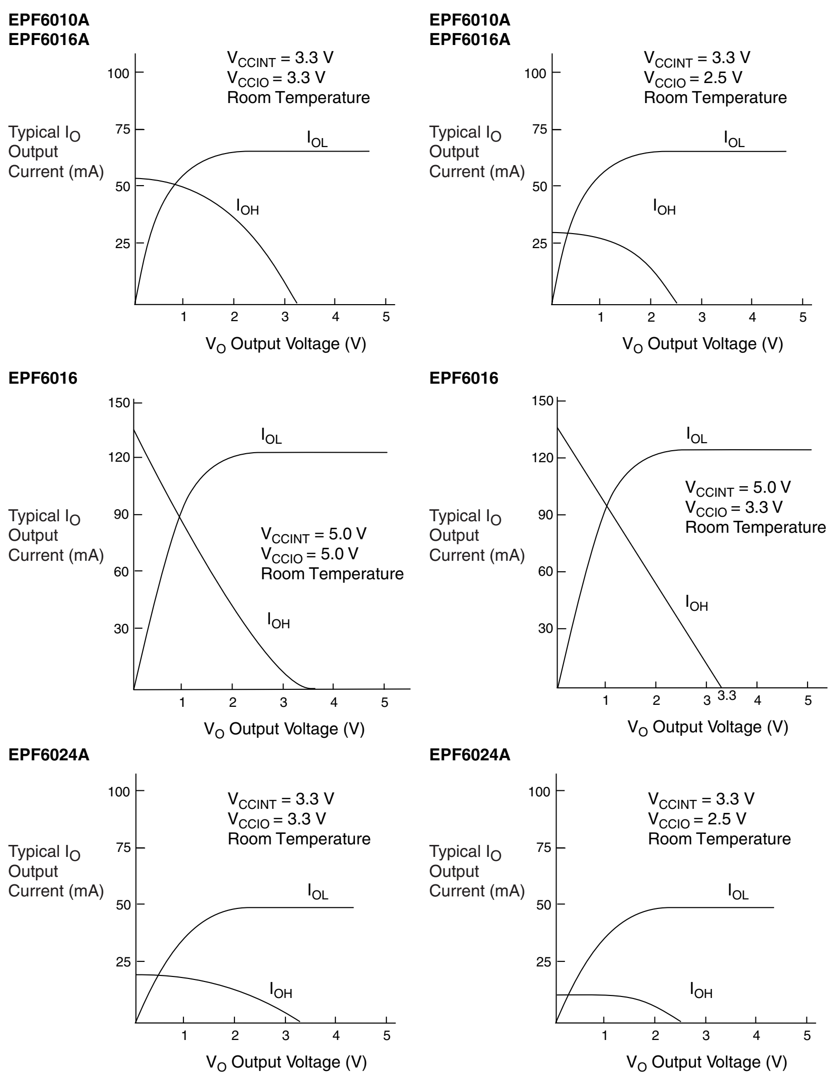


Table 23. External Timing Parameters		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time with global clock at LE register	(8)
t_{INH}	Hold time with global clock at LE register	(8)
t_{OUTCO}	Clock-to-output delay with global clock with LE register using FastFLEX I/O pin	(8)

Notes to tables:

(1) Microparameters are timing delays contributed by individual architectural elements and cannot be measured explicitly.
(2) Operating conditions:
V_{CCIO} = 5.0 V ±5% for commercial use in 5.0-V FLEX 6000 devices.
V_{CCIO} = 5.0 V ±10% for industrial use in 5.0-V FLEX 6000 devices.
V_{CCIO} = 3.3 V ±10% for commercial or industrial use in 3.3-V FLEX 6000 devices.
(3) Operating conditions:
V_{CCIO} = 3.3 V ±10% for commercial or industrial use in 5.0-V FLEX 6000 devices.
V_{CCIO} = 2.5 V ±0.2 V for commercial or industrial use in 3.3-V FLEX 6000 devices.
(4) Operating conditions:
V_{CCIO} = 2.5 V, 3.3 V, or 5.0 V.
(5) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
(6) This timing parameter shows the delay of a register-to-register test pattern and is used to determine speed grades. There are 12 LEs, including source and destination registers. The row and column interconnects between the registers vary in length.
(7) This timing parameter is shown for reference and is specified by characterization.
(8) This timing parameter is specified by characterization.

Tables 24 through 28 show the timing information for EPF6010A and EPF6016A devices.

Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 1 of 2)							
Parameter	**Speed Grade**						**Unit**
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{REG\_TO\_REG}$		1.2		1.3		1.7	ns
$t_{CASC\_TO\_REG}$		0.9		1.0		1.2	ns
$t_{CARRY\_TO\_REG}$		0.9		1.0		1.2	ns
$t_{DATA\_TO\_REG}$		1.1		1.2		1.5	ns
$t_{CASC\_TO\_OUT}$		1.3		1.4		1.8	ns
$t_{CARRY\_TO\_OUT}$		1.6		1.8		2.3	ns
$t_{DATA\_TO\_OUT}$		1.7		2.0		2.5	ns
$t_{REG\_TO\_OUT}$		0.4		0.4		0.5	ns
t_{SU}	0.9		1.0		1.3		ns
t_H	1.4		1.7		2.1		ns

Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 2 of 2)							
Parameter	**Speed Grade**						**Unit**
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{CO}		0.3		0.4		0.4	ns
t_{CLR}		0.4		0.4		0.5	ns
t_{C}		1.8		2.1		2.6	ns
t_{LD_CLR}		1.8		2.1		2.6	ns
$t_{CARRY\_TO\_CARRY}$		0.1		0.1		0.1	ns
$t_{REG\_TO\_CARRY}$		1.6		1.9		2.3	ns
$t_{DATA\_TO\_CARRY}$		2.1		2.5		3.0	ns
$t_{CARRY\_TO\_CASC}$		1.0		1.1		1.4	ns
$t_{CASC\_TO\_CASC}$		0.5		0.6		0.7	ns
$t_{REG\_TO\_CASC}$		1.4		1.7		2.1	ns
$t_{DATA\_TO\_CASC}$		1.1		1.2		1.5	ns
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

Table 25. IOE Timing Microparameters for EPF6010A & EPF6016A Devices							
Parameter	**Speed Grade**						**Unit**
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{OD1}		1.9		2.2		2.7	ns
t_{OD2}		4.1		4.8		5.8	ns
t_{OD3}		5.8		6.8		8.3	ns
t_{XZ}		1.4		1.7		2.1	ns
t_{XZ1}		1.4		1.7		2.1	ns
t_{XZ2}		3.6		4.3		5.2	ns
t_{XZ3}		5.3		6.3		7.7	ns
t_{IOE}		0.5		0.6		0.7	ns
t_{IN}		3.6		4.1		5.1	ns
t_{IN_DELAY}		4.8		5.4		6.7	ns

Table 26. Interconnect Timing Microparameters for EPF6010A & EPF6016A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LOCAL}		0.7		0.7		1.0	ns
t_{ROW}		2.9		3.2		3.2	ns
t_{COL}		1.2		1.3		1.4	ns
t_{DIN_D}		5.4		5.7		6.4	ns
t_{DIN_C}		4.3		5.0		6.1	ns
$t_{LEGLOBAL}$		2.6		3.0		3.7	ns
$t_{LABCARRY}$		0.7		0.8		0.9	ns
$t_{LABCASC}$		1.3		1.4		1.8	ns

Table 27. External Reference Timing Parameters for EPF6010A & EPF6016A Devices

Parameter	Device	Speed Grade						Unit
		-1		-2		-3		
		Min	Max	Min	Max	Min	Max	
t_1	EPF6010A		37.6		43.6		53.7	ns
	EPF6016A		38.0		44.0		54.1	ns

Table 28. External Timing Parameters for EPF6010A & EPF6016A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.1 *(1)*		2.4 *(1)*		3.3 *(1)*		ns
t_{INH}	0.2 *(2)*		0.3 *(2)*		0.1 *(2)*		ns
t_{OUTCO}	2.0	7.1	2.0	8.2	2.0	10.1	ns

Notes:

(1) Setup times are longer when the *Increase Input Delay* option is turned on. The setup time values are shown with the *Increase Input Delay* option turned off.

(2) Hold time is zero when the *Increase Input Delay* option is turned on.

Tables 29 through 33 show the timing information for EPF6016 devices.

Table 29. LE Timing Microparameters for EPF6016 Devices					
Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
$t_{REG\_TO\_REG}$		2.2		2.8	ns
$t_{CASC\_TO\_REG}$		0.9		1.2	ns
$t_{CARRY\_TO\_REG}$		1.6		2.1	ns
$t_{DATA\_TO\_REG}$		2.4		3.0	ns
$t_{CASC\_TO\_OUT}$		1.3		1.7	ns
$t_{CARRY\_TO\_OUT}$		2.4		3.0	ns
$t_{DATA\_TO\_OUT}$		2.7		3.4	ns
$t_{REG\_TO\_OUT}$		0.3		0.5	ns
t_{SU}	1.1		1.6		ns
t_{H}	1.8		2.3		ns
t_{CO}		0.3		0.4	ns
t_{CLR}		0.5		0.6	ns
t_{C}		1.2		1.5	ns
t_{LD_CLR}		1.2		1.5	ns
$t_{CARRY\_TO\_CARRY}$		0.2		0.4	ns
$t_{REG\_TO\_CARRY}$		0.8		1.1	ns
$t_{DATA\_TO\_CARRY}$		1.7		2.2	ns
$t_{CARRY\_TO\_CASC}$		1.7		2.2	ns
$t_{CASC\_TO\_CASC}$		0.9		1.2	ns
$t_{REG\_TO\_CASC}$		1.6		2.0	ns
$t_{DATA\_TO\_CASC}$		1.7		2.1	ns
t_{CH}	4.0		4.0		ns
t_{CL}	4.0		4.0		ns

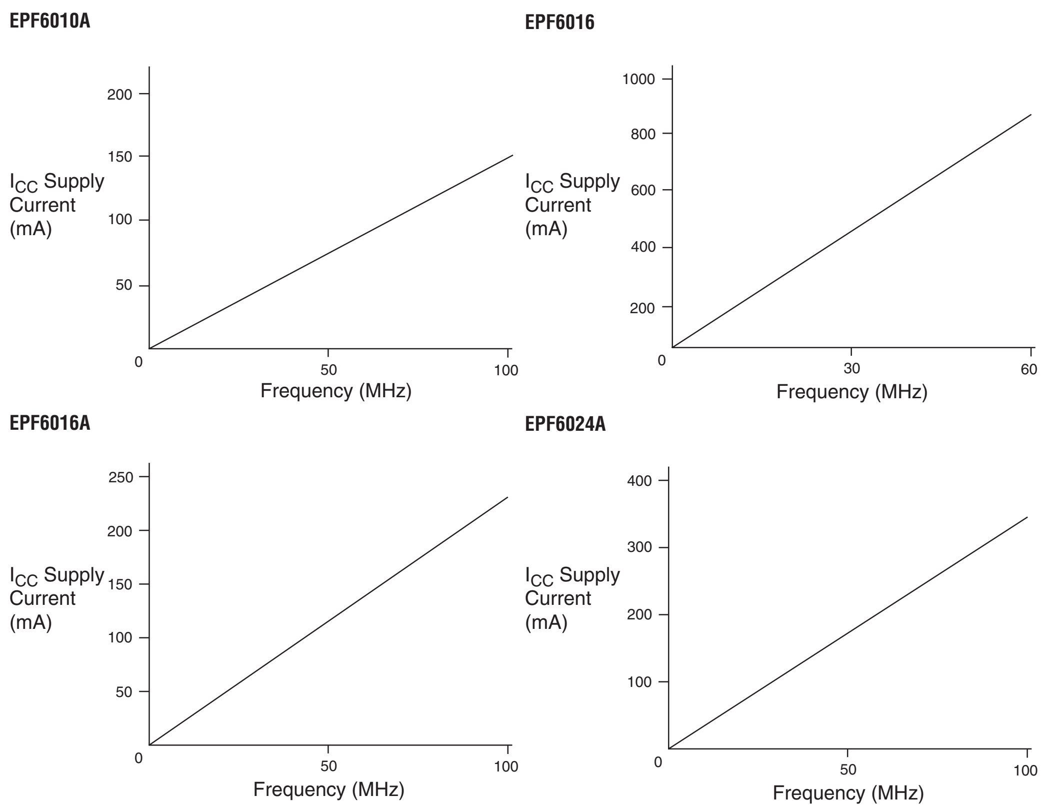
Table 30. IOE Timing Microparameters for EPF6016 Devices					
Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
t_{OD1}		2.3		2.8	ns
t_{OD2}		4.6		5.1	ns

Table 33. External Timing Parameters for EPF6016 Devices					
Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
t_{INSU}	3.2		4.1		ns
t_{INH}	0.0		0.0		ns
t_{OUTCO}	2.0	7.9	2.0	9.9	ns

Tables 34 through 38 show the timing information for EPF6024A devices.

Table 34. LE Timing Microparameters for EPF6024A Devices							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{REG\_TO\_REG}$		1.2		1.3		1.6	ns
$t_{CASC\_TO\_REG}$		0.7		0.8		1.0	ns
$t_{CARRY\_TO\_REG}$		1.6		1.8		2.2	ns
$t_{DATA\_TO\_REG}$		1.3		1.4		1.7	ns
$t_{CASC\_TO\_OUT}$		1.2		1.3		1.6	ns
$t_{CARRY\_TO\_OUT}$		2.0		2.2		2.6	ns
$t_{DATA\_TO\_OUT}$		1.8		2.1		2.6	ns
$t_{REG\_TO\_OUT}$		0.3		0.3		0.4	ns
t_{SU}	0.9		1.0		1.2		ns
t_{H}	1.3		1.4		1.7		ns
t_{CO}		0.2		0.3		0.3	ns
t_{CLR}		0.3		0.3		0.4	ns
t_{C}		1.9		2.1		2.5	ns
t_{LD_CLR}		1.9		2.1		2.5	ns
$t_{CARRY\_TO\_CARRY}$		0.2		0.2		0.3	ns
$t_{REG\_TO\_CARRY}$		1.4		1.6		1.9	ns
$t_{DATA\_TO\_CARRY}$		1.3		1.4		1.7	ns
$t_{CARRY\_TO\_CASC}$		1.1		1.2		1.4	ns
$t_{CASC\_TO\_CASC}$		0.7		0.8		1.0	ns
$t_{REG\_TO\_CASC}$		1.4		1.6		1.9	ns
$t_{DATA\_TO\_CASC}$		1.0		1.1		1.3	ns
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

Figure 20. $I_{CCACTIVE}$ vs. Operating Frequency



Device Configuration & Operation

The FLEX 6000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.

f See *Application Note 116 (Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices)* for detailed information on configuring FLEX 6000 devices, including sample schematics, timing diagrams, configuration options, pins names, and timing parameters.

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