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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	88
Number of Logic Elements/Cells	880
Total RAM Bits	-
Number of I/O	102
Number of Gates	10000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf6010atc144-3n">https://www.e-xfl.com/product-detail/intel/epf6010atc144-3n</a>

## Functional Description

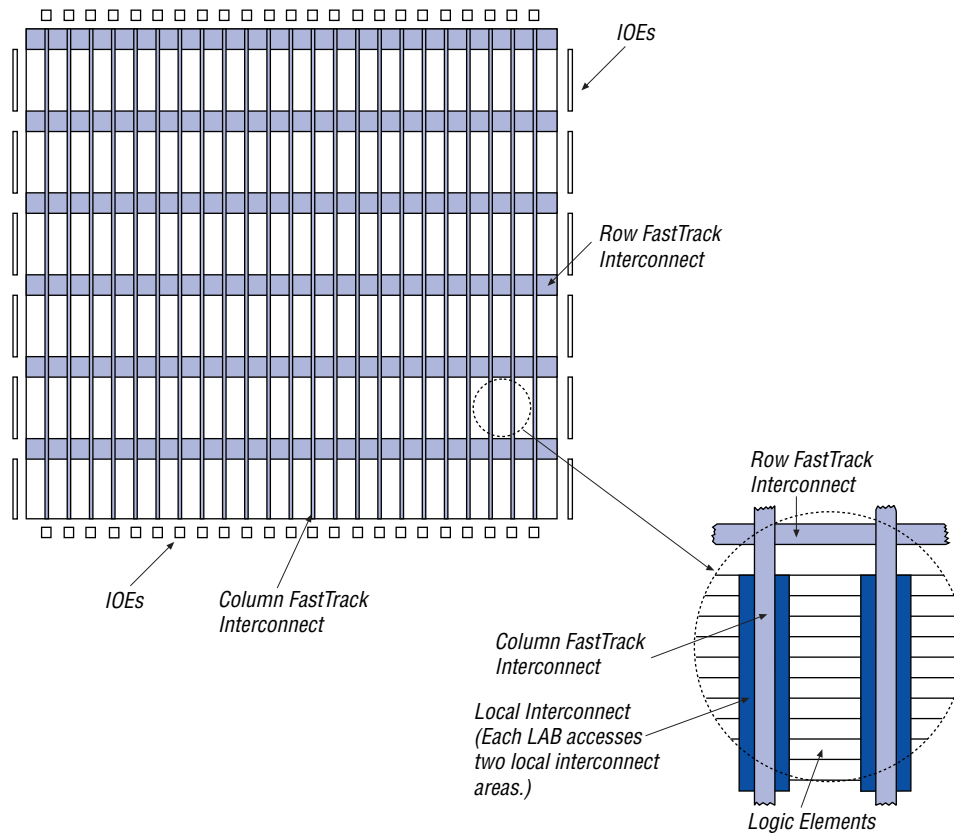
The FLEX 6000 OptiFLEX architecture consists of logic elements (LEs). Each LE includes a 4-input look-up table (LUT), which can implement any 4-input function, a register, and dedicated paths for carry and cascade chain functions. Because each LE contains a register, a design can be easily pipelined without consuming more LEs. The specified gate count for FLEX 6000 devices includes all LUTs and registers.

LEs are combined into groups called logic array blocks (LABs); each LAB contains 10 LEs. The Altera software automatically places related LEs into the same LAB, minimizing the number of required interconnects. Each LAB can implement a medium-sized block of logic, such as a counter or multiplexer.

Signal interconnections within FLEX 6000 devices—and to and from device pins—are provided via the routing structure of the FastTrack Interconnect. The routing structure is a series of fast, continuous row and column channels that run the entire length and width of the device. Any LE or pin can feed or be fed by any other LE or pin via the FastTrack Interconnect. See “FastTrack Interconnect” on [page 17](#) of this data sheet for more information.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer. Each IOE is placed next to an LAB, where it can be driven by the local interconnect of that LAB. This feature allows fast clock-to-output times of less than 8 ns when a pin is driven by any of the 10 LEs in the adjacent LAB. Also, any LE can drive any pin via the row and column interconnect. I/O pins can drive the LE registers via the row and column interconnect, providing setup times as low as 2 ns and hold times of 0 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, and tri-state buffers.

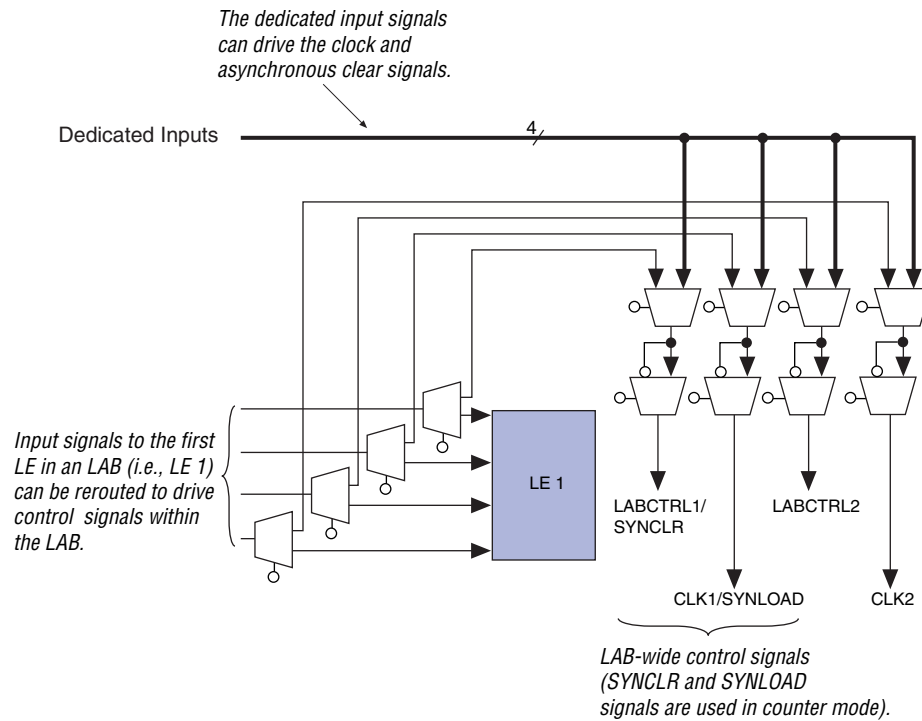
[Figure 1](#) shows a block diagram of the FLEX 6000 OptiFLEX architecture. Each group of ten LEs is combined into an LAB, and the LABs are arranged into rows and columns. The LABs are interconnected by the FastTrack Interconnect. IOEs are located at the end of each FastTrack Interconnect row and column.

**Figure 1. OptiFLEX Architecture Block Diagram**

FLEX 6000 devices provide four dedicated, global inputs that drive the control inputs of the flipflops to ensure efficient distribution of high-speed, low-skew control signals. These inputs use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. These inputs can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device. The dedicated global routing structure is built into the device, eliminating the need to create a clock tree.

### Logic Array Block

An LAB consists of ten LEs, their associated carry and cascade chains, the LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 6000 architecture, and facilitates efficient routing with optimum device utilization and high performance.

**Figure 3. LAB Control Signals**

## Logic Element

An LE, the smallest unit of logic in the FLEX 6000 architecture, has a compact size that provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. An LE contains a programmable flipflop, carry and cascade chains. Additionally, each LE drives both the local and the FastTrack Interconnect. See [Figure 4](#).

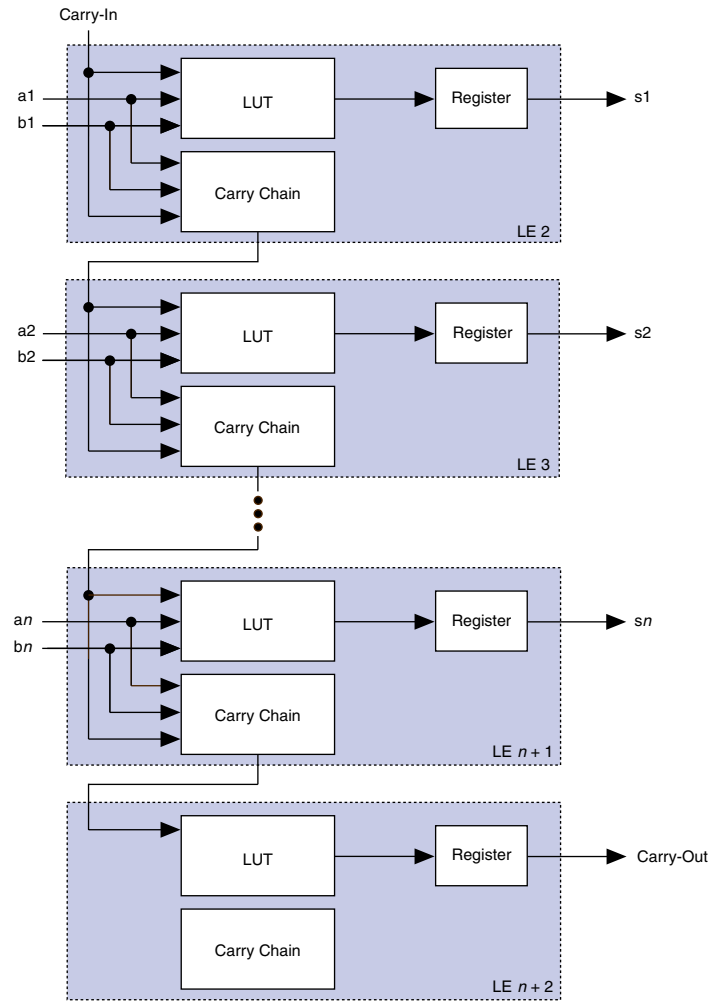
### *Carry Chain*

The carry chain provides a very fast (0.1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 6000 architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Altera software during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

Because the first LE of each LAB can generate control signals for that LAB, the first LE in each LAB is not included in carry chains. In addition, the inputs of the first LE in each LAB may be used to generate synchronous clear and load enable signals for counters implemented with carry chains.

Carry chains longer than nine LEs are implemented automatically by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from an even-numbered LAB to another even-numbered LAB, or from an odd-numbered LAB to another odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the second LE of the third LAB in the row. In addition, the carry chain does not cross the middle of the row. For instance, in the EPF6016 device, the carry chain stops at the 11th LAB in a row and a new carry chain begins at the 12th LAB.

Figure 5 shows how an  $n$ -bit full adder can be implemented in  $n + 1$  LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. Although the register can be bypassed for simple adders, it can be used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the FastTrack Interconnect.

**Figure 5. Carry Chain Operation**

**Normal Mode**

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The Altera software automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal.

**Arithmetic Mode**

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a 3-input function; the other generates a carry output. As shown in [Figure 7](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

The Altera software implements logic functions to use the arithmetic mode automatically where appropriate; the designer does not have to decide how the carry chain will be used.

**Counter Mode**

The counter mode offers counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in a LAB use counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. In addition, the Altera software automatically places registers that are not in the counter into other LABs.

The counter mode uses two 3-input LUTs: one generates the counter data and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load will override any signal carried on the cascade chain. The synchronous clear overrides the synchronous load.

Either the counter enable or the up/down control may be used for a given counter. Moreover, the synchronous load can be used as a count enable by routing the register output into the data input automatically when requested by the designer.

The second LE of each LAB has a special function for counter mode; the carry-in of the LE can be driven by a fast feedback path from the register. This function gives a faster counter speed for counter carry chains starting in the second LE of an LAB.

The Altera software implements functions to use the counter mode automatically where appropriate. The designer does not have to decide how the carry chain will be used.

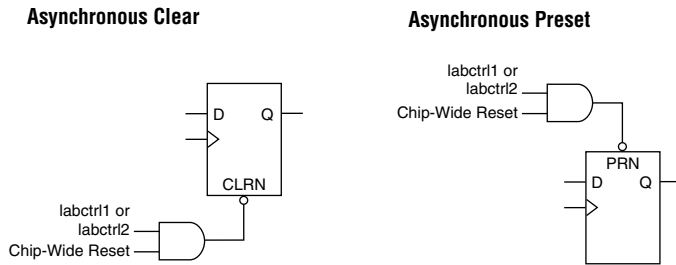
### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

### *Clear & Preset Logic Control*

Logic for the programmable register's clear and preset functions is controlled by the LAB-wide signals LABCTRL1 and LABCTRL2. The LE register has an asynchronous clear that can implement an asynchronous preset. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear or preset. Because the clear and preset functions are active-low, the Altera software automatically assigns a logic high to an unused clear or preset signal. The clear and preset logic is implemented in either the asynchronous clear or asynchronous preset mode, which is chosen during design entry (see [Figure 8](#)).



**Figure 8. LE Clear & Preset Modes****Asynchronous Clear**

The flipflop can be cleared by either LABCTRL1 or LABCTRL2.

**Asynchronous Preset**

An asynchronous preset is implemented with an asynchronous clear. The Altera software provides preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, this technique can be used when a register drives logic or drives a pin.

In addition to the two clear and preset modes, FLEX 6000 devices provide a chip-wide reset pin (DEV\_CLRn) that can reset all registers in the device. The option to use this pin is set in the Altera software before compilation. The chip-wide reset overrides all other control signals. Any register with an asynchronous preset will be preset when the chip-wide reset is asserted because of the inversion technique used to implement the asynchronous preset.

The Altera software can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses an additional three LEs per register.

**FastTrack Interconnect**

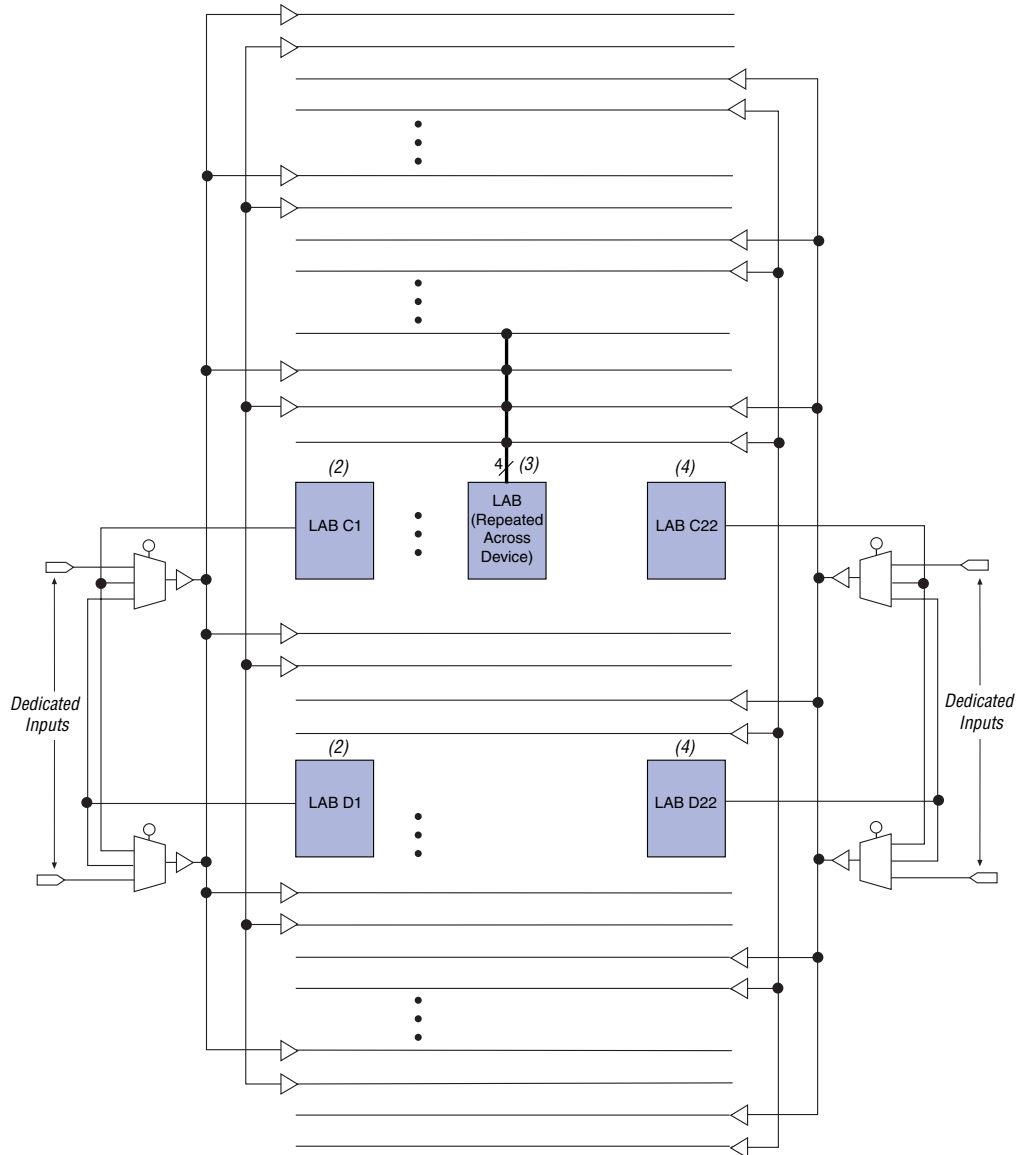
In the FLEX 6000 OptiFLEX architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even for complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

Table 5 summarizes the FastTrack Interconnect resources available in each FLEX 6000 device.

<b>Table 5. FLEX 6000 FastTrack Interconnect Resources</b>				
<b>Device</b>	<b>Rows</b>	<b>Channels per Row</b>	<b>Columns</b>	<b>Channels per Column</b>
EPF6010A	4	144	22	20
EPF6016 EPF6016A	6	144	22	20
EPF6024A	7	186	28	30

In addition to general-purpose I/O pins, FLEX 6000 devices have four dedicated input pins that provide low-skew signal distribution across the device. These four inputs can be used for global clock and asynchronous clear control signals. These signals are available as control signals for all LEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device. Using dedicated inputs to route data signals provides a fast path for high fan-out signals.

The local interconnect from LABs located at either end of two rows can drive a global control signal. For instance, in an EPF6016 device, LABs C1, D1, C22, and D22 can all drive global control signals. When an LE drives a global control signal, the dedicated input pin that drives that signal cannot be used. Any LE in the device can drive a global control signal by driving the FastTrack Interconnect into the appropriate LAB. To minimize delay, however, the Altera software places the driving LE in the appropriate LAB. The LE-driving-global signal feature is optimized for speed for control signals; regular data signals are better routed on the FastTrack Interconnect and do not receive any advantage from being routed on global signals. This LE-driving-global control signal feature is controlled by the designer and is not used automatically by the Altera software. See Figure 11.

**Figure 11. Global Clock & Clear Distribution** *Note (1)***Notes:**

- (1) The global clock and clear distribution signals are shown for EPF6016 and EPF6016A devices. In EPF6010A devices, LABs in rows B and C drive global signals. In EPF6024A devices, LABs in rows C and E drive global signals.
- (2) The local interconnect from LABs C1 and D1 can drive two global control signals on the left side.
- (3) Global signals drive into every LAB as clock, asynchronous clear, preset, and data signals.
- (4) The local interconnect from LABs C22 and D22 can drive two global control signals on the right side.

## MultiVolt I/O Interface

The FLEX 6000 device architecture supports the MultiVolt I/O interface feature, which allows FLEX 6000 devices to interface with systems of differing supply voltages. The EPF6016 device can be set for 3.3-V or 5.0-V I/O pin operation. This device has one set of  $V_{CC}$  pins for internal operation and input buffers ( $V_{CCINT}$ ), and another set for output drivers ( $V_{CCIO}$ ).

The  $V_{CCINT}$  pins on 5.0-V FLEX 6000 devices must always be connected to a 5.0-V power supply. With a 5.0-V  $V_{CCINT}$  level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The  $V_{CCIO}$  pins on 5.0-V FLEX 6000 devices can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the  $V_{CCIO}$  pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the  $V_{CCIO}$  pins are connected to a 3.3-V power supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with  $V_{CCIO}$  levels lower than 4.75 V incur a nominally greater timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ .

On 3.3-V FLEX 6000 devices, the  $V_{CCINT}$  pins must be connected to a 3.3-V power supply. Additionally, 3.3-V FLEX 6000A devices can interface with 2.5-V, 3.3-V, or 5.0-V systems when the  $V_{CCIO}$  pins are tied to 2.5 V. The output can drive 2.5-V systems, and the inputs can be driven by 2.5-V, 3.3-V, or 5.0-V systems. When the  $V_{CCIO}$  pins are tied to 3.3 V, the output can drive 3.3-V or 5.0-V systems. MultiVolt I/Os are not supported on 100-pin TQFP or 100-pin FineLine BGA packages.

Table 7 describes FLEX 6000 MultiVolt I/O support.

<b>Table 7. FLEX 6000 MultiVolt I/O Support</b>							
<b><math>V_{CCINT}</math> (V)</b>	<b><math>V_{CCIO}</math> (V)</b>	<b>Input Signal (V)</b>			<b>Output Signal (V)</b>		
		<b>2.5</b>	<b>3.3</b>	<b>5.0</b>	<b>2.5</b>	<b>3.3</b>	<b>5.0</b>
3.3	2.5	v	v	v	v		
3.3	3.3	v	v	v	v (1)	v	v
5.0	3.3		v	v		v	v
5.0	5.0		v	v			v

**Note:**

- (1) When  $V_{CCIO} = 3.3$  V, a FLEX 6000 device can drive a 2.5-V device that has 3.3-V tolerant inputs.

The instruction register length for FLEX 6000 devices is three bits. [Table 9](#) shows the boundary-scan register length for FLEX 6000 devices.

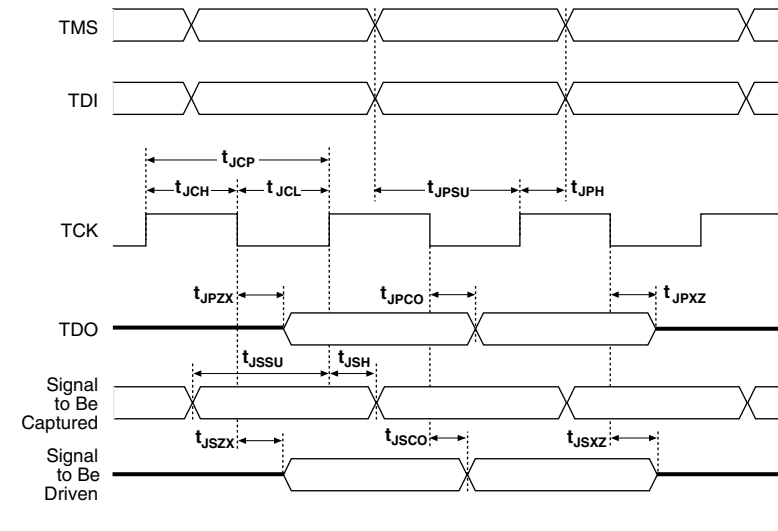
<b>Table 9. FLEX 6000 Device Boundary-Scan Register Length</b>	
<b>Device</b>	<b>Boundary-Scan Register Length</b>
EPF6010A	522
EPF6016	621
EPF6016A	522
EPF6024A	666

FLEX 6000 devices include a weak pull-up on JTAG pins.

f See [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#) for more information.

[Figure 16](#) shows the timing requirements for the JTAG signals.

**Figure 16. JTAG Waveforms**



[Table 10](#) shows the JTAG timing parameters and values for FLEX 6000 devices.

## Operating Conditions

Tables 11 through 18 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V and 3.3-V FLEX 6000 devices.

**Table 11. FLEX 6000 5.0-V Device Absolute Maximum Ratings** *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply voltage	With respect to ground (2)	−2.0	7.0	V
$V_I$	DC input voltage		−2.0	7.0	V
$I_{OUT}$	DC output current, per pin		−25	25	mA
$T_{STG}$	Storage temperature	No bias	−65	150	°C
$T_{AMB}$	Ambient temperature	Under bias	−65	135	°C
$T_J$	Junction temperature	PQFP, TQFP, and BGA packages		135	°C

**Table 12. FLEX 6000 5.0-V Device Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
$V_{CCIO}$	Supply voltage for output buffers, 5.0-V operation	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
$V_I$	Input voltage		−0.5	$V_{CCINT} + 0.5$	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_J$	Operating temperature	For commercial use	0	85	°C
		For industrial use	−40	100	°C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns

**Table 13. FLEX 6000 5.0-V Device DC Operating Conditions** Notes (5), (6)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	High-level input voltage		2.0		$V_{CCINT} + 0.5$	V
$V_{IL}$	Low-level input voltage		-0.5		0.8	V
$V_{OH}$	5.0-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 4.75$ V (7)	2.4			V
	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (7)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (7)	$V_{CCIO} - 0.2$			V
$V_{OL}$	5.0-V low-level TTL output voltage	$I_{OL} = 8$ mA DC, $V_{CCIO} = 4.75$ V (8)			0.45	V
	3.3-V low-level TTL output voltage	$I_{OL} = 8$ mA DC, $V_{CCIO} = 3.00$ V (8)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (8)			0.2	V
$I_I$	Input pin leakage current	$V_I = V_{CC}$ or ground (8)	-10		10	$\mu$ A
$I_{OZ}$	Tri-stated I/O pin leakage current	$V_O = V_{CC}$ or ground (8)	-40		40	$\mu$ A
$I_{CC0}$	$V_{CC}$ supply current (standby)	$V_I =$ ground, no load		0.5	5	mA

**Table 14. FLEX 6000 5.0-V Device Capacitance** Note (9)

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance for I/O pin	$V_{IN} = 0$ V, $f = 1.0$ MHz		8	pF
$C_{INCLK}$	Input capacitance for dedicated input	$V_{IN} = 0$ V, $f = 1.0$ MHz		12	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		8	pF

**Notes to tables:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum  $V_{CC}$  rise time to 100 ms.  $V_{CC}$  must rise monotonically.
- (5) Typical values are for  $T_A = 25^\circ$  C and  $V_{CC} = 5.0$  V.
- (6) These values are specified under the FLEX 6000 Recommended Operating Conditions shown in Table 12 on page 31.
- (7) The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current.
- (8) The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (9) Capacitance is sample-tested only.

**Table 15. FLEX 6000 3.3-V Device Absolute Maximum Ratings** *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply voltage	With respect to ground (2)	−0.5	4.6	V
$V_I$	DC input voltage		−2.0	5.75	V
$I_{OUT}$	DC output current, per pin		−25	25	mA
$T_{STG}$	Storage temperature	No bias	−65	150	°C
$T_{AMB}$	Ambient temperature	Under bias	−65	135	°C
$T_J$	Junction temperature	PQFP, PLCC, and BGA packages		135	°C

**Table 16. FLEX 6000 3.3-V Device Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
$V_{CCIO}$	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.30 (2.30)	2.70 (2.70)	V
$V_I$	Input voltage		−0.5	5.75	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_J$	Operating temperature	For commercial use	0	85	°C
		For industrial use	−40	100	°C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns



<b>Table 17. FLEX 6000 3.3-V Device DC Operating Conditions</b> <i>Notes (5), (6)</i>						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	High-level input voltage		1.7		5.75	V
$V_{IL}$	Low-level input voltage		-0.5		0.8	V
$V_{OH}$	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (7)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (7)	$V_{CCIO} - 0.2$			V
	2.5-V high-level output voltage	$I_{OH} = -100$ $\mu$ A DC, $V_{CCIO} = 2.30$ V (7)	2.1			V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (7)	2.0			V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (7)	1.7			V
$V_{OL}$	3.3-V low-level TTL output voltage	$I_{OL} = 8$ mA DC, $V_{CCIO} = 3.00$ V (8)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (8)			0.2	V
	2.5-V low-level output voltage	$I_{OL} = 100$ $\mu$ A DC, $V_{CCIO} = 2.30$ V (8)			0.2	V
		$I_{OL} = 1$ mA DC, $V_{CCIO} = 2.30$ V (8)			0.4	V
		$I_{OL} = 2$ mA DC, $V_{CCIO} = 2.30$ V (8)			0.7	V
$I_I$	Input pin leakage current	$V_I = 5.3$ V to ground (8)	-10		10	$\mu$ A
$I_{OZ}$	Tri-stated I/O pin leakage current	$V_O = 5.3$ V to ground (8)	-10		10	$\mu$ A
$I_{CC0}$	$V_{CC}$ supply current (standby)	$V_I =$ ground, no load		0.5	5	mA

<b>Table 18. FLEX 6000 3.3-V Device Capacitance</b> <i>Note (9)</i>					
Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance for I/O pin	$V_{IN} = 0$ V, $f = 1.0$ MHz		8	pF
$C_{INCLK}$	Input capacitance for dedicated input	$V_{IN} = 0$ V, $f = 1.0$ MHz		12	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		8	pF

**Notes to tables:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) The minimum DC input voltage is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum  $V_{CC}$  rise time is 100 ms.  $V_{CC}$  must rise monotonically.
- (5) Typical values are for  $T_A = 25^\circ$  C and  $V_{CC} = 3.3$  V.
- (6) These values are specified under [Table 16 on page 33](#).
- (7) The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current.
- (8) The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (9) Capacitance is sample-tested only.

**Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 2 of 2)**

Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 2 of 2)							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{CO}$		0.3		0.4		0.4	ns
$t_{CLR}$		0.4		0.4		0.5	ns
$t_C$		1.8		2.1		2.6	ns
$t_{LD\_CLR}$		1.8		2.1		2.6	ns
$t_{CARRY\_TO\_CARRY}$		0.1		0.1		0.1	ns
$t_{REG\_TO\_CARRY}$		1.6		1.9		2.3	ns
$t_{DATA\_TO\_CARRY}$		2.1		2.5		3.0	ns
$t_{CARRY\_TO\_CASC}$		1.0		1.1		1.4	ns
$t_{CASC\_TO\_CASC}$		0.5		0.6		0.7	ns
$t_{REG\_TO\_CASC}$		1.4		1.7		2.1	ns
$t_{DATA\_TO\_CASC}$		1.1		1.2		1.5	ns
$t_{CH}$	2.5		3.0		3.5		ns
$t_{CL}$	2.5		3.0		3.5		ns

**Table 25. IOE Timing Microparameters for EPF6010A & EPF6016A Devices**

Table 25. IOE Timing Microparameters for EPF6010A & EPF6016A Devices							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{OD1}$		1.9		2.2		2.7	ns
$t_{OD2}$		4.1		4.8		5.8	ns
$t_{OD3}$		5.8		6.8		8.3	ns
$t_{XZ}$		1.4		1.7		2.1	ns
$t_{XZ1}$		1.4		1.7		2.1	ns
$t_{XZ2}$		3.6		4.3		5.2	ns
$t_{XZ3}$		5.3		6.3		7.7	ns
$t_{IOE}$		0.5		0.6		0.7	ns
$t_{IN}$		3.6		4.1		5.1	ns
$t_{IN\_DELAY}$		4.8		5.4		6.7	ns

Tables 29 through 33 show the timing information for EPF6016 devices.

Table 29. LE Timing Microparameters for EPF6016 Devices					
Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
$t_{REG\_TO\_REG}$		2.2		2.8	ns
$t_{CASC\_TO\_REG}$		0.9		1.2	ns
$t_{CARRY\_TO\_REG}$		1.6		2.1	ns
$t_{DATA\_TO\_REG}$		2.4		3.0	ns
$t_{CASC\_TO\_OUT}$		1.3		1.7	ns
$t_{CARRY\_TO\_OUT}$		2.4		3.0	ns
$t_{DATA\_TO\_OUT}$		2.7		3.4	ns
$t_{REG\_TO\_OUT}$		0.3		0.5	ns
$t_{SU}$	1.1		1.6		ns
$t_H$	1.8		2.3		ns
$t_{CO}$		0.3		0.4	ns
$t_{CLR}$		0.5		0.6	ns
$t_C$		1.2		1.5	ns
$t_{LD\_CLR}$		1.2		1.5	ns
$t_{CARRY\_TO\_CARRY}$		0.2		0.4	ns
$t_{REG\_TO\_CARRY}$		0.8		1.1	ns
$t_{DATA\_TO\_CARRY}$		1.7		2.2	ns
$t_{CARRY\_TO\_CASC}$		1.7		2.2	ns
$t_{CASC\_TO\_CASC}$		0.9		1.2	ns
$t_{REG\_TO\_CASC}$		1.6		2.0	ns
$t_{DATA\_TO\_CASC}$		1.7		2.1	ns
$t_{CH}$	4.0		4.0		ns
$t_{CL}$	4.0		4.0		ns

Table 30. IOE Timing Microparameters for EPF6016 Devices					
Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
$t_{OD1}$		2.3		2.8	ns
$t_{OD2}$		4.6		5.1	ns

**Table 33. External Timing Parameters for EPF6016 Devices**

Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
t <sub>INSU</sub>	3.2		4.1		ns
t <sub>INH</sub>	0.0		0.0		ns
t <sub>OUTCO</sub>	2.0	7.9	2.0	9.9	ns

Tables 34 through 38 show the timing information for EPF6024A devices.

**Table 34. LE Timing Microparameters for EPF6024A Devices**

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{REG\_TO\_REG}$		1.2		1.3		1.6	ns
$t_{CASC\_TO\_REG}$		0.7		0.8		1.0	ns
$t_{CARRY\_TO\_REG}$		1.6		1.8		2.2	ns
$t_{DATA\_TO\_REG}$		1.3		1.4		1.7	ns
$t_{CASC\_TO\_OUT}$		1.2		1.3		1.6	ns
$t_{CARRY\_TO\_OUT}$		2.0		2.2		2.6	ns
$t_{DATA\_TO\_OUT}$		1.8		2.1		2.6	ns
$t_{REG\_TO\_OUT}$		0.3		0.3		0.4	ns
$t_{SU}$	0.9		1.0		1.2		ns
$t_H$	1.3		1.4		1.7		ns
$t_{CO}$		0.2		0.3		0.3	ns
$t_{CLR}$		0.3		0.3		0.4	ns
$t_C$		1.9		2.1		2.5	ns
$t_{LD\_CLR}$		1.9		2.1		2.5	ns
$t_{CARRY\_TO\_CARRY}$		0.2		0.2		0.3	ns
$t_{REG\_TO\_CARRY}$		1.4		1.6		1.9	ns
$t_{DATA\_TO\_CARRY}$		1.3		1.4		1.7	ns
$t_{CARRY\_TO\_CASC}$		1.1		1.2		1.4	ns
$t_{CASC\_TO\_CASC}$		0.7		0.8		1.0	ns
$t_{REG\_TO\_CASC}$		1.4		1.6		1.9	ns
$t_{DATA\_TO\_CASC}$		1.0		1.1		1.3	ns
$t_{CH}$	2.5		3.0		3.5		ns
$t_{CL}$	2.5		3.0		3.5		ns

**Table 38. External Timing Parameters for EPF6024A Devices**

Table 38. External Timing Parameters for EPF6024A Devices							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	2.0 (1)		2.2 (1)		2.6 (1)		ns
t <sub>INH</sub>	0.2 (2)		0.2 (2)		0.3 (2)		ns
t <sub>OUTCO</sub>	2.0	7.4	2.0	8.2	2.0	9.9	ns

**Notes:**

- (1) Setup times are longer when the *Increase Input Delay* option is turned on. The setup time values are shown with the *Increase Input Delay* option turned off.
- (2) Hold time is zero when the *Increase Input Delay* option is turned on.

## Power Consumption

The supply power (P) for FLEX 6000 devices can be calculated with the following equations:

$$P = P_{\text{INT}} + P_{\text{IO}}$$

$$P = (I_{\text{CCSTANDBY}} + I_{\text{CCACTIVE}}) \times V_{\text{CC}} + P_{\text{IO}}$$

Typical  $I_{\text{CCSTANDBY}}$  values are shown as  $I_{\text{CC0}}$  in the “FLEX 6000 Device DC Operating Conditions” table on [pages 31 and 33](#) of this data sheet. The  $I_{\text{CCACTIVE}}$  value depends on the switching frequency and the application logic. This value is based on the amount of current that each LE typically consumes. The  $P_{\text{IO}}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#).

The  $I_{\text{CCACTIVE}}$  value can be calculated with the following equation:

$$I_{\text{CCACTIVE}} = K \times f_{\text{MAX}} \times N \times \text{tog}_{\text{LC}} \times \frac{\mu\text{A}}{\text{MHz} \times \text{LE}}$$

Where:

$f_{\text{MAX}}$  = Maximum operating frequency in MHz

$N$  = Total number of LEs used in a FLEX 6000 device

$\text{tog}_{\text{LC}}$  = Average percentage of LEs toggling at each clock (typically 12.5%)

$K$  = Constant, shown in [Table 39](#)

**Table 39. K Constant Values**

Device	K Value
EPF6010A	14
EPF6016	88
EPF6016A	14
EPF6024A	14