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### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### **Details**

Product Status	Active
Number of LABs/CLBs	132
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	81
Number of Gates	-
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-LBGA
Supplier Device Package	100-FBGA (11x11)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=epf6016afc100-2">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=epf6016afc100-2</a>

## ...and More Features

- Powerful I/O pins
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Fast path from register to I/O pin for fast clock-to-output time
- Flexible interconnect
  - FastTrack<sup>®</sup> Interconnect continuous routing structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Tri-state emulation that implements internal tri-state networks
  - Four low-skew global paths for clock, clear, preset, or logic signals
- Software design support and automatic place-and-route provided by Altera’s development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800
- Flexible package options
  - Available in a variety of packages with 100 to 256 pins, including the innovative FineLine BGA<sup>™</sup> packages (see [Table 2](#))
  - SameFrame<sup>™</sup> pin-compatibility (with other FLEX<sup>®</sup> 6000 devices) across device densities and pin counts
  - Thin quad flat pack (TQFP), plastic quad flat pack (PQFP), and ball-grid array (BGA) packages (see [Table 2](#))
  - Footprint- and pin-compatibility with other FLEX 6000 devices in the same package
- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, the library of parameterized modules (LPM), Verilog HDL, VHDL, DesignWare components, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Device	100-Pin TQFP	100-Pin FineLine BGA	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin BGA	256-pin FineLine BGA
EPF6010A	71		102				
EPF6016			117	171	199	204	
EPF6016A	81	81	117	171			171
EPF6024A			117	171	199	218	219

### *Carry Chain*

The carry chain provides a very fast (0.1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 6000 architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Altera software during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

Because the first LE of each LAB can generate control signals for that LAB, the first LE in each LAB is not included in carry chains. In addition, the inputs of the first LE in each LAB may be used to generate synchronous clear and load enable signals for counters implemented with carry chains.

Carry chains longer than nine LEs are implemented automatically by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from an even-numbered LAB to another even-numbered LAB, or from an odd-numbered LAB to another odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the second LE of the third LAB in the row. In addition, the carry chain does not cross the middle of the row. For instance, in the EPF6016 device, the carry chain stops at the 11th LAB in a row and a new carry chain begins at the 12th LAB.

Figure 5 shows how an  $n$ -bit full adder can be implemented in  $n + 1$  LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. Although the register can be bypassed for simple adders, it can be used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the FastTrack Interconnect.

### *Cascade Chain*

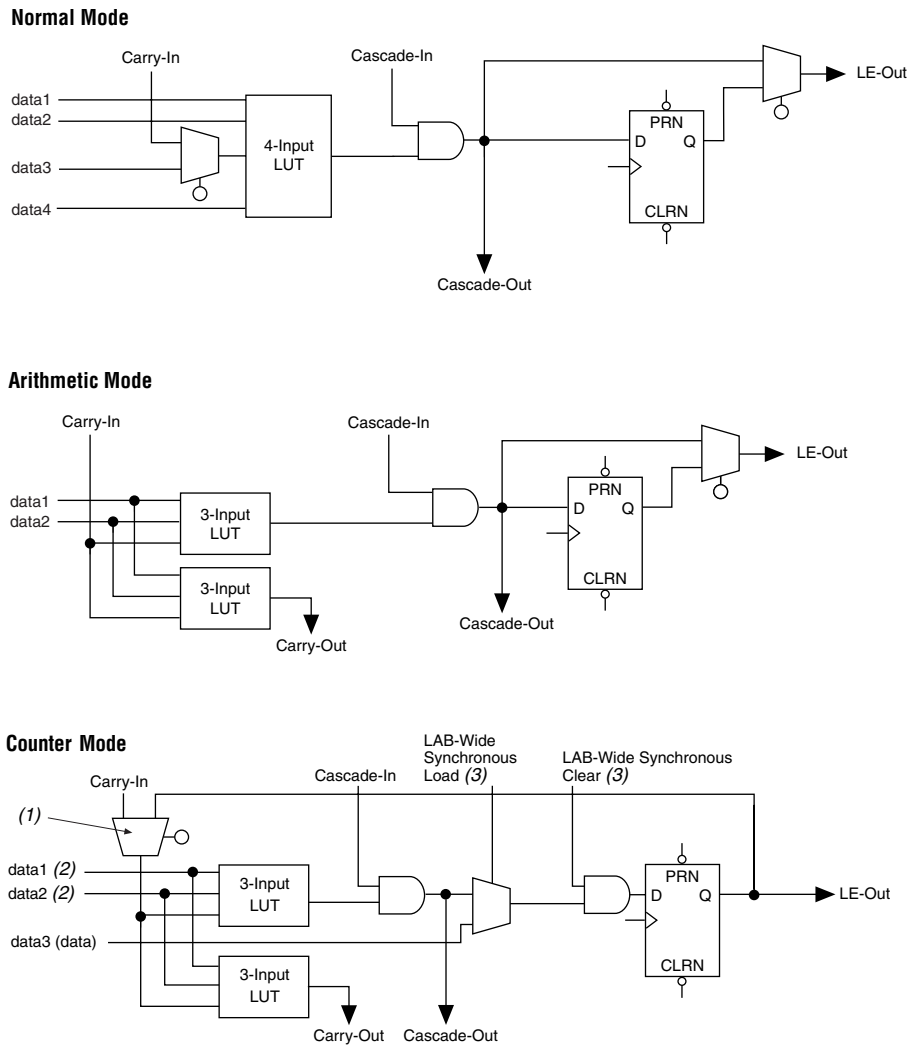
The cascade chain enables the FLEX 6000 architecture to implement very wide fan-in functions. Adjacent LUTs can be used to implement portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR gate (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 0.5 ns per LE. Cascade chain logic can be created automatically by the Altera software during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of cascade chains for the appropriate functions.

A cascade chain implementing an AND gate can use the register in the last LE; a cascade chain implementing an OR gate cannot use this register because of the inversion required to implement the OR gate.

Because the first LE of an LAB can generate control signals for that LAB, the first LE in each LAB is not included in cascade chains. Moreover, cascade chains longer than nine bits are automatically implemented by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from an even-numbered LAB to another even-numbered LAB, or from an odd-numbered LAB to another odd-numbered LAB. For example, the last LE of the first LAB in a row cascades to the second LE of the third LAB. The cascade chain does not cross the center of the row. For example, in an EPF6016 device, the cascade chain stops at the 11th LAB in a row and a new cascade chain begins at the 12th LAB.

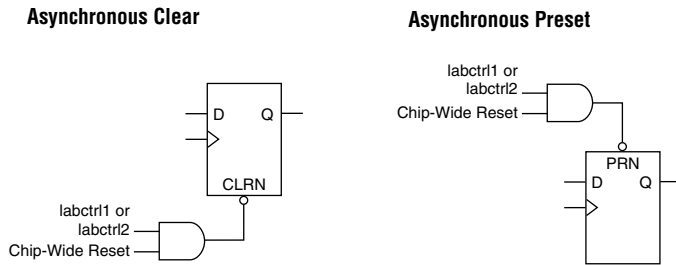
Figure 6 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. In this example, functions of  $4n$  variables are implemented with  $n$  LEs. The cascade chain requires 3.4 ns to decode a 16-bit address.

Figure 7. LE Operating Modes



**Notes:**

- (1) The register feedback multiplexer is available on LE 2 of each LAB.
- (2) The data1 and data2 input signals can supply a clock enable, up or down control, or register feedback signals for all LEs other than the second LE in an LAB.
- (3) The LAB-wide synchronous clear and LAB-wide synchronous load affect all registers in an LAB.

**Figure 8. LE Clear & Preset Modes****Asynchronous Clear**

The flipflop can be cleared by either LABCTRL1 or LABCTRL2.

**Asynchronous Preset**

An asynchronous preset is implemented with an asynchronous clear. The Altera software provides preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, this technique can be used when a register drives logic or drives a pin.

In addition to the two clear and preset modes, FLEX 6000 devices provide a chip-wide reset pin (DEV\_CLRn) that can reset all registers in the device. The option to use this pin is set in the Altera software before compilation. The chip-wide reset overrides all other control signals. Any register with an asynchronous preset will be preset when the chip-wide reset is asserted because of the inversion technique used to implement the asynchronous preset.

The Altera software can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses an additional three LEs per register.

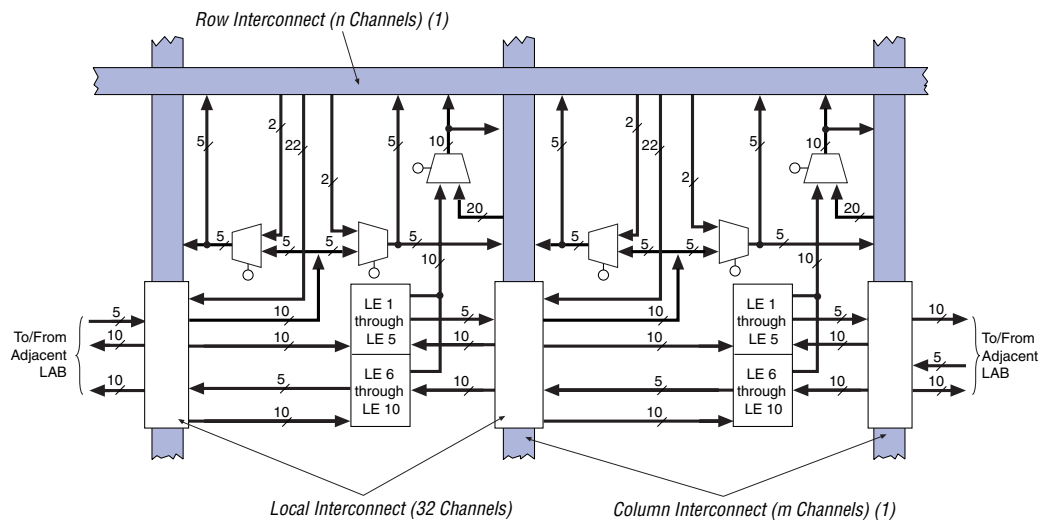
**FastTrack Interconnect**

In the FLEX 6000 OptiFLEX architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even for complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of column and row interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect, which routes signals between LABs in the same row, and also routes signals from I/O pins to LABs. Additionally, the local interconnect routes signals between LEs in the same LAB and in adjacent LABs. The column interconnect routes signals between rows and routes signals from I/O pins to rows.

LEs 1 through 5 of an LAB drive the local interconnect to the right, while LEs 6 through 10 drive the local interconnect to the left. The DATA1 and DATA3 inputs of each LE are driven by the local interconnect to the left; DATA2 and DATA4 are driven by the local interconnect to the right. The local interconnect also routes signals from LEs to I/O pins. Figure 9 shows an overview of the FLEX 6000 interconnect architecture. LEs in the first and last columns have drivers on both sides so that all LEs in the LAB can drive I/O pins via the local interconnect.

Figure 9. FastTrack Interconnect Architecture



Note:

- (1) For EPF6010A, EPF6016, and EPF6016A devices,  $n = 144$  channels and  $m = 20$  channels; for EPF6024A devices,  $n = 186$  channels and  $m = 30$  channels.

A row channel can be driven by an LE or by one of two column channels. These three signals feed a 3-to-1 multiplexer that connects to six specific row channels. Row channels drive into the local interconnect via multiplexers.

Each column of LABs is served by a dedicated column interconnect. The LEs in an LAB can drive the column interconnect. The LEs in an LAB, a column IOE, or a row interconnect can drive the column interconnect. The column interconnect can then drive another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect must be routed to the row interconnect before it can enter an LAB.

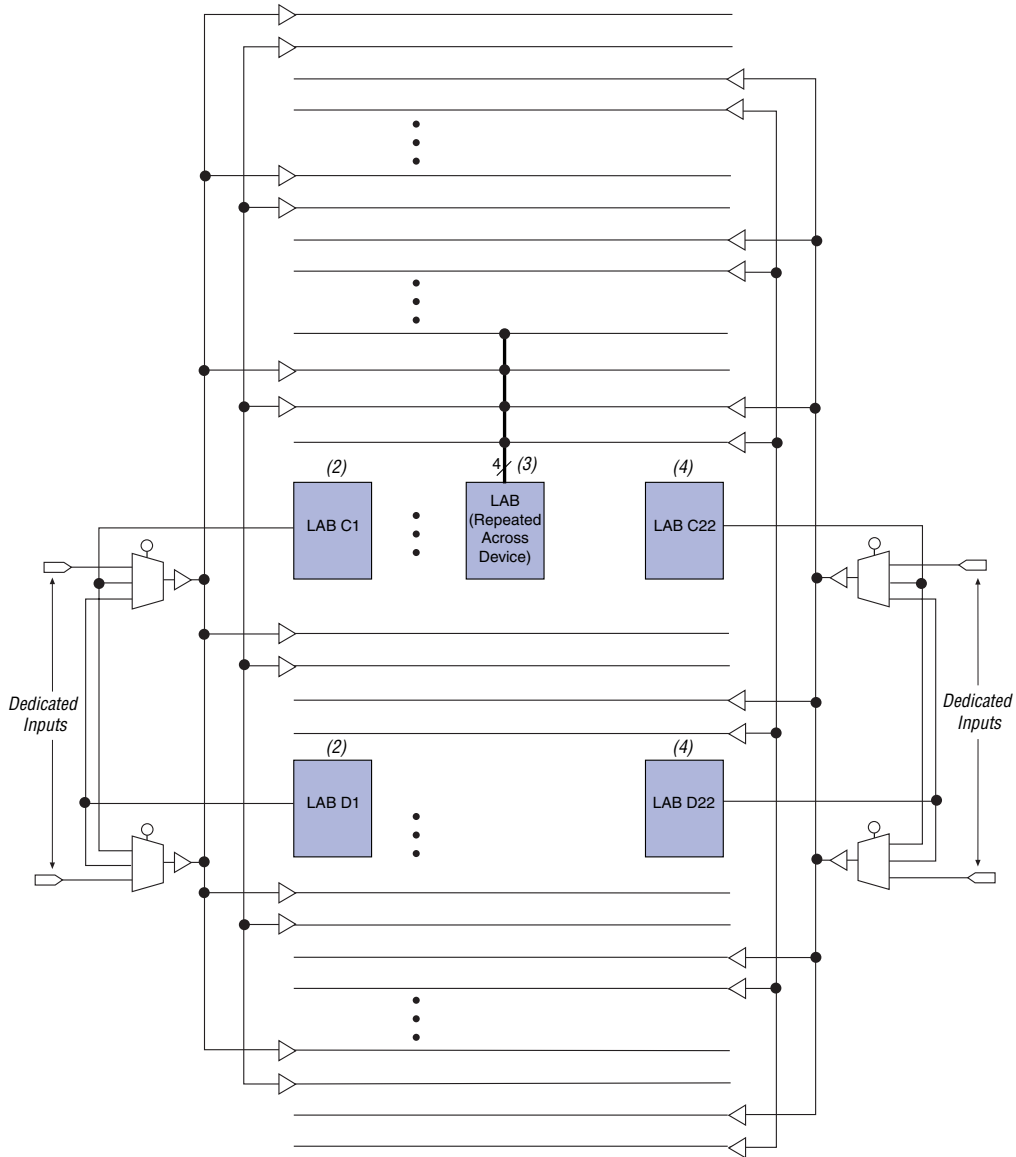
Each LE has a FastTrack Interconnect output and a local output. The FastTrack interconnect output can drive six row and two column lines directly; the local output drives the local interconnect. Each local interconnect channel driven by an LE can drive four row and two column channels. This feature provides additional flexibility, because each LE can drive any of ten row lines and four column lines.

In addition, LEs can drive global control signals. This feature is useful for distributing internally generated clock, asynchronous clear, and asynchronous preset signals. A pin-driven global signal can also drive data signals, which is useful for high-fan-out data signals.

Each LAB drives two groups of local interconnects, which allows an LE to drive two LABs, or 20 LEs, via the local interconnect. The row-to-local multiplexers are used more efficiently, because the multiplexers can now drive two LABs. [Figure 10](#) shows how an LAB connects to row and column interconnects.



Figure 11. Global Clock & Clear Distribution *Note (1)*



**Notes:**

- (1) The global clock and clear distribution signals are shown for EPF6016 and EPF6016A devices. In EPF6010A devices, LABs in rows B and C drive global signals. In EPF6024A devices, LABs in rows C and E drive global signals.
- (2) The local interconnect from LABs C1 and D1 can drive two global control signals on the left side.
- (3) Global signals drive into every LAB as clock, asynchronous clear, preset, and data signals.
- (4) The local interconnect from LABs C22 and D22 can drive two global control signals on the right side.

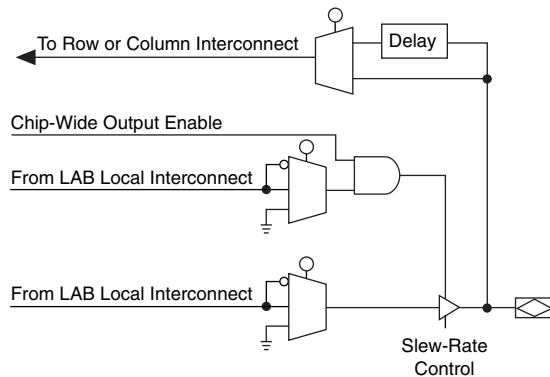
## I/O Elements

An IOE contains a bidirectional I/O buffer and a tri-state buffer. IOEs can be used as input, output, or bidirectional pins. An IOE receives its data signals from the adjacent local interconnect, which can be driven by a row or column interconnect (allowing any LE in the device to drive the IOE) or by an adjacent LE (allowing fast clock-to-output delays). A FastFLEX™ I/O pin is a row or column output pin that receives its data signals from the adjacent local interconnect driven by an adjacent LE. The IOE receives its output enable signal through the same path, allowing individual output enables for every pin and permitting emulation of open-drain buffers. The Altera Compiler uses programmable inversion to invert the data or output enable signals automatically where appropriate. Open-drain emulation is provided by driving the data input low and toggling the OE of each IOE. This emulation is possible because there is one OE per pin.

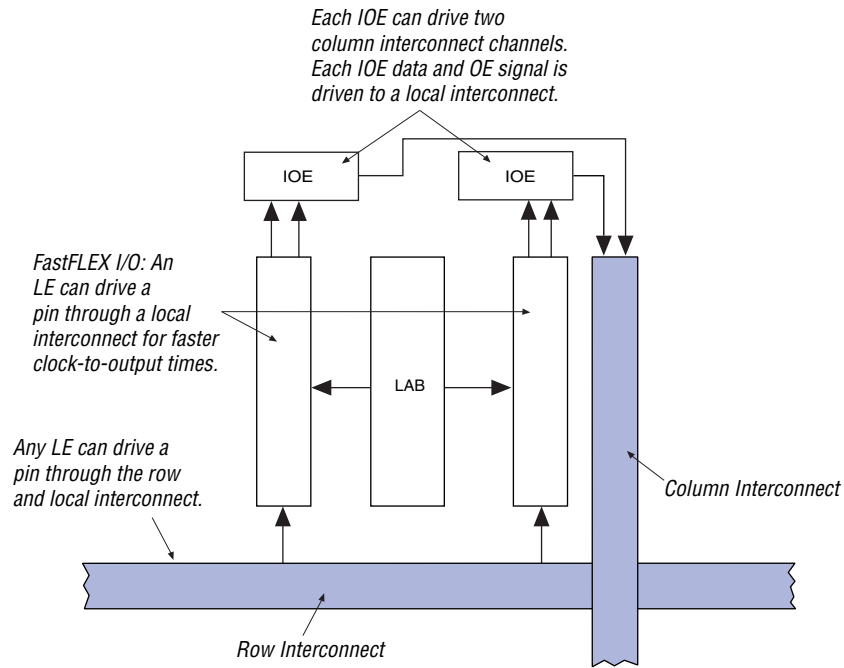
A chip-wide output enable feature allows the designer to disable all pins of the device by asserting one pin (DEV\_OE). This feature is useful during board debugging or testing.

Figure 12 shows the IOE block diagram.

**Figure 12. IOE Block Diagram**



**Figure 14. IOE Connection to Column Interconnect**



## SameFrame Pin-Outs

3.3-V FLEX 6000 devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support an EPF6016A device in a 100-pin FineLine BGA package or an EPF6024A device in a 256-pin FineLine BGA package.

The Altera software packages provide support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software packages generate pin-outs describing how to lay out a board to take advantage of this migration (see [Figure 15](#)).

**Figure 15. SameFrame Pin-Out Example**

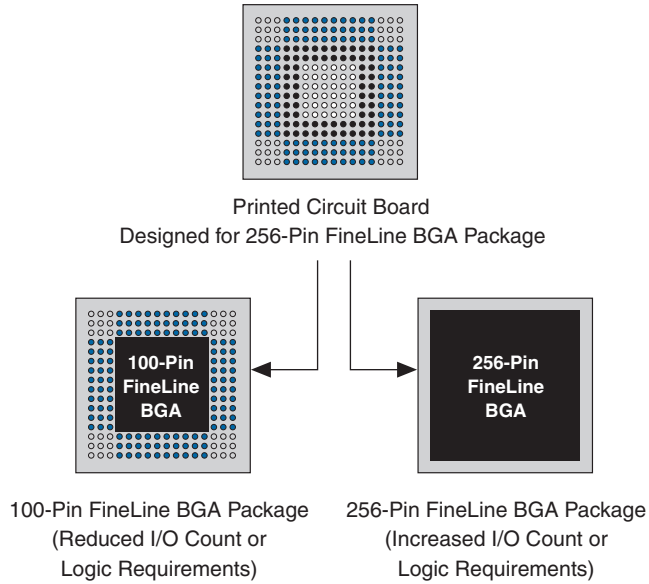


Table 6 lists the 3.3-V FLEX 6000 devices with the SameFrame pin-out feature.

<b>Table 6. 3.3-V FLEX 6000 Devices with SameFrame Pin-Outs</b>		
<b>Device</b>	<b>100-Pin FineLine BGA</b>	<b>256-Pin FineLine BGA</b>
EPF6016A	v	v
EPF6024A		v

## Output Configuration

This section discusses slew-rate control, the MultiVolt I/O interface, power sequencing, and hot-socketing for FLEX 6000 devices.

### Slew-Rate Control

The output buffer in each IOE has an adjustable output slew-rate that can be configured for low-noise or high-speed performance. A slower slew-rate reduces system noise and adds a maximum delay of 6.8 ns. The fast slew-rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew-rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a device-wide basis. The slew-rate setting affects only the falling edge of the output.

**Table 13. FLEX 6000 5.0-V Device DC Operating Conditions** Notes (5), (6)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	High-level input voltage		2.0		V <sub>CCINT</sub> + 0.5	V
V <sub>IL</sub>	Low-level input voltage		-0.5		0.8	V
V <sub>OH</sub>	5.0-V high-level TTL output voltage	I <sub>OH</sub> = -8 mA DC, V <sub>CCIO</sub> = 4.75 V (7)	2.4			V
	3.3-V high-level TTL output voltage	I <sub>OH</sub> = -8 mA DC, V <sub>CCIO</sub> = 3.00 V (7)	2.4			V
	3.3-V high-level CMOS output voltage	I <sub>OH</sub> = -0.1 mA DC, V <sub>CCIO</sub> = 3.00 V (7)	V <sub>CCIO</sub> - 0.2			V
V <sub>OL</sub>	5.0-V low-level TTL output voltage	I <sub>OL</sub> = 8 mA DC, V <sub>CCIO</sub> = 4.75 V (8)			0.45	V
	3.3-V low-level TTL output voltage	I <sub>OL</sub> = 8 mA DC, V <sub>CCIO</sub> = 3.00 V (8)			0.45	V
	3.3-V low-level CMOS output voltage	I <sub>OL</sub> = 0.1 mA DC, V <sub>CCIO</sub> = 3.00 V (8)			0.2	V
I <sub>I</sub>	Input pin leakage current	V <sub>I</sub> = V <sub>CC</sub> or ground (8)	-10		10	μA
I <sub>OZ</sub>	Tri-stated I/O pin leakage current	V <sub>O</sub> = V <sub>CC</sub> or ground (8)	-40		40	μA
I <sub>CC0</sub>	V <sub>CC</sub> supply current (standby)	V <sub>I</sub> = ground, no load		0.5	5	mA

**Table 14. FLEX 6000 5.0-V Device Capacitance** Note (9)

Symbol	Parameter	Conditions	Min	Max	Unit
C <sub>IN</sub>	Input capacitance for I/O pin	V <sub>IN</sub> = 0 V, f = 1.0 MHz		8	pF
C <sub>INCLK</sub>	Input capacitance for dedicated input	V <sub>IN</sub> = 0 V, f = 1.0 MHz		12	pF
C <sub>OUT</sub>	Output capacitance	V <sub>OUT</sub> = 0 V, f = 1.0 MHz		8	pF

**Notes to tables:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum V<sub>CC</sub> rise time to 100 ms. V<sub>CC</sub> must rise monotonically.
- (5) Typical values are for T<sub>A</sub> = 25° C and V<sub>CC</sub> = 5.0 V.
- (6) These values are specified under the FLEX 6000 Recommended Operating Conditions shown in Table 12 on page 31.
- (7) The I<sub>OH</sub> parameter refers to high-level TTL or CMOS output current.
- (8) The I<sub>OL</sub> parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (9) Capacitance is sample-tested only.

## Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row can be calculated by adding the following parameters:

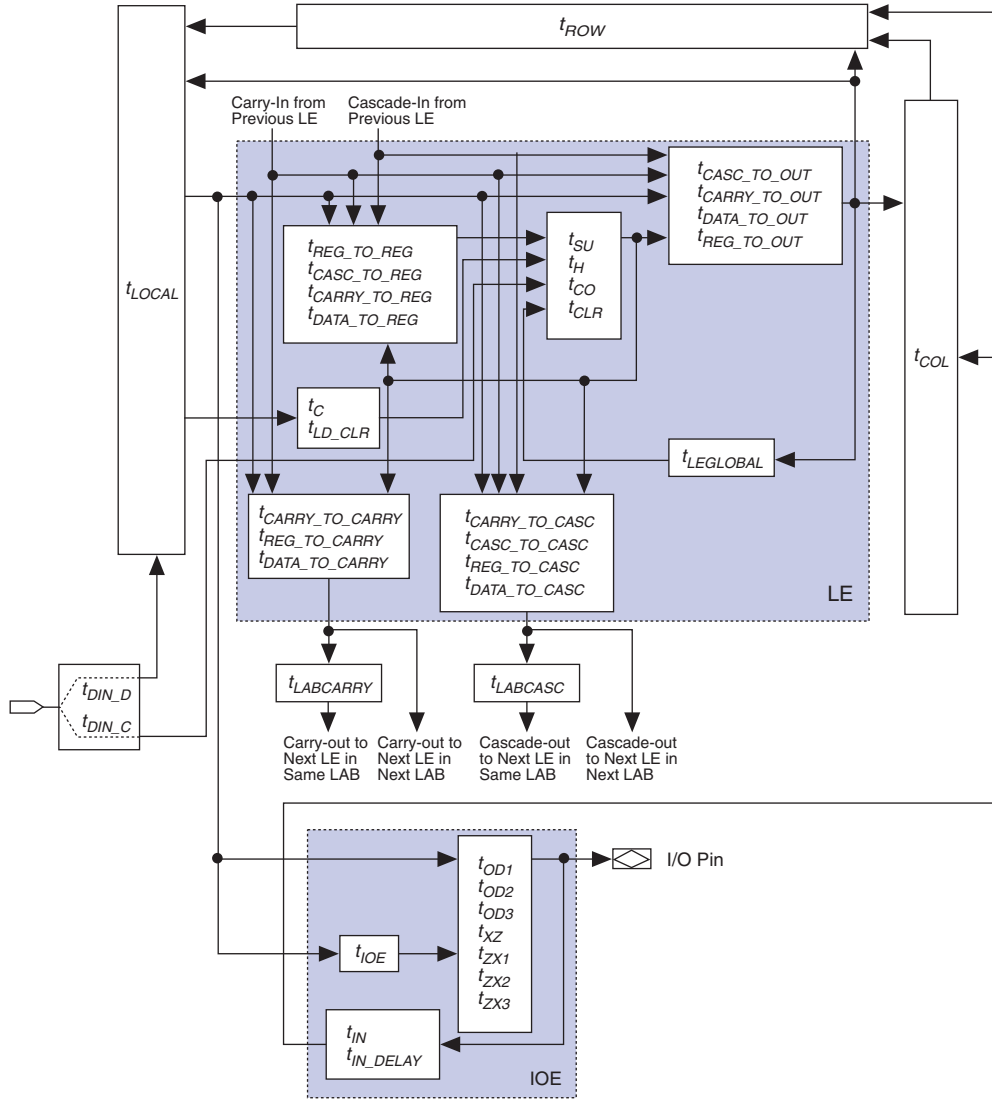
- LE register clock-to-output delay ( $t_{CO} + t_{REG\_TO\_OUT}$ )
- Routing delay ( $t_{ROW} + t_{LOCAL}$ )
- LE LUT delay ( $t_{DATA\_TO\_REG}$ )
- LE register setup time ( $t_{SU}$ )

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

Timing simulation and delay prediction are available with the Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 19 shows the overall timing model, which maps the possible routing paths to and from the various elements of the FLEX 6000 device.

Figure 19. FLEX 6000 Timing Model



<b>Table 20. IOE Timing Microparameters</b> <i>Note (1)</i>		
<b>Symbol</b>	<b>Parameter</b>	<b>Conditions</b>
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF (2)
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = \text{low voltage}$	C1 = 35 pF (3)
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF (4)
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF (2)
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off, $V_{CCIO} = \text{low voltage}$	C1 = 35 pF (3)
$t_{ZX3}$	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF (4)
$t_{IOE}$	Output enable control delay	
$t_{IN}$	Input pad and buffer to FastTrack Interconnect delay	
$t_{IN\_DELAY}$	Input pad and buffer to FastTrack Interconnect delay with additional delay turned on	

<b>Table 21. Interconnect Timing Microparameters</b> <i>Note (1)</i>		
<b>Symbol</b>	<b>Parameter</b>	<b>Conditions</b>
$t_{LOCAL}$	LAB local interconnect delay	
$t_{ROW}$	Row interconnect routing delay	(5)
$t_{COL}$	Column interconnect routing delay	(5)
$t_{DIN\_D}$	Dedicated input to LE data delay	(5)
$t_{DIN\_C}$	Dedicated input to LE control delay	
$t_{LEGLOBAL}$	LE output to LE control via internally-generated global signal delay	(5)
$t_{LABCARRY}$	Routing delay for the carry-out of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

<b>Table 22. External Reference Timing Parameters</b>		
<b>Symbol</b>	<b>Parameter</b>	<b>Conditions</b>
$t_1$	Register-to-register test pattern	(6)
$t_{DRR}$	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects	(7)



Tables 29 through 33 show the timing information for EPF6016 devices.

**Table 29. LE Timing Microparameters for EPF6016 Devices**

Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
$t_{REG\_TO\_REG}$		2.2		2.8	ns
$t_{CASC\_TO\_REG}$		0.9		1.2	ns
$t_{CARRY\_TO\_REG}$		1.6		2.1	ns
$t_{DATA\_TO\_REG}$		2.4		3.0	ns
$t_{CASC\_TO\_OUT}$		1.3		1.7	ns
$t_{CARRY\_TO\_OUT}$		2.4		3.0	ns
$t_{DATA\_TO\_OUT}$		2.7		3.4	ns
$t_{REG\_TO\_OUT}$		0.3		0.5	ns
$t_{SU}$	1.1		1.6		ns
$t_H$	1.8		2.3		ns
$t_{CO}$		0.3		0.4	ns
$t_{CLR}$		0.5		0.6	ns
$t_C$		1.2		1.5	ns
$t_{LD\_CLR}$		1.2		1.5	ns
$t_{CARRY\_TO\_CARRY}$		0.2		0.4	ns
$t_{REG\_TO\_CARRY}$		0.8		1.1	ns
$t_{DATA\_TO\_CARRY}$		1.7		2.2	ns
$t_{CARRY\_TO\_CASC}$		1.7		2.2	ns
$t_{CASC\_TO\_CASC}$		0.9		1.2	ns
$t_{REG\_TO\_CASC}$		1.6		2.0	ns
$t_{DATA\_TO\_CASC}$		1.7		2.1	ns
$t_{CH}$	4.0		4.0		ns
$t_{CL}$	4.0		4.0		ns

**Table 30. IOE Timing Microparameters for EPF6016 Devices**

Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
$t_{OD1}$		2.3		2.8	ns
$t_{OD2}$		4.6		5.1	ns

**Table 35. IOE Timing Microparameters for EPF6024A Devices**

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{OD1}$		1.9		2.1		2.5	ns
$t_{OD2}$		4.0		4.4		5.3	ns
$t_{OD3}$		7.0		7.8		9.3	ns
$t_{XZ}$		4.3		4.8		5.8	ns
$t_{XZ1}$		4.3		4.8		5.8	ns
$t_{XZ2}$		6.4		7.1		8.6	ns
$t_{XZ3}$		9.4		10.5		12.6	ns
$t_{IOE}$		0.5		0.6		0.7	ns
$t_{IN}$		3.3		3.7		4.4	ns
$t_{IN\_DELAY}$		5.3		5.9		7.0	ns

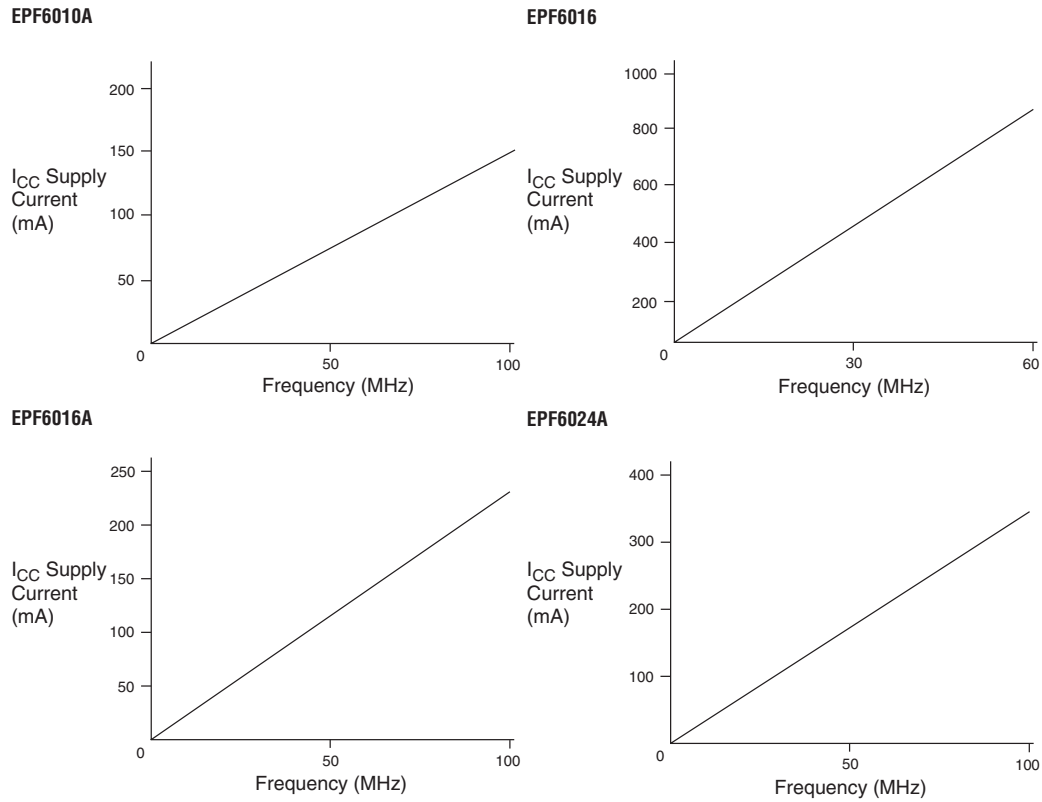
**Table 36. Interconnect Timing Microparameters for EPF6024A Devices**

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{LOCAL}$		0.8		0.8		1.1	ns
$t_{ROW}$		3.0		3.1		3.3	ns
$t_{COL}$		3.0		3.2		3.4	ns
$t_{DIN\_D}$		5.4		5.6		6.2	ns
$t_{DIN\_C}$		4.6		5.1		6.1	ns
$t_{LEGLOBAL}$		3.1		3.5		4.3	ns
$t_{LABCARRY}$		0.6		0.7		0.8	ns
$t_{LABCASC}$		0.3		0.3		0.4	ns

**Table 37. External Reference Timing Parameters for EPF6024A Devices**

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_1$		45.0		50.0		60.0	ns

Figure 20.  $I_{CCACTIVE}$  vs. Operating Frequency



## Device Configuration & Operation

The FLEX 6000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.

- f See [Application Note 116 \(Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices\)](#) for detailed information on configuring FLEX 6000 devices, including sample schematics, timing diagrams, configuration options, pins names, and timing parameters.

## Operating Modes

The FLEX 6000 architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. This process of physically loading the SRAM data into a FLEX 6000 device is known as configuration. During initialization—a process that occurs immediately after configuration—the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. The configuration and initialization processes of a device are referred to as *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 6000 devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and is used to dynamically reconfigure an entire system. Also, in-field system upgrades can be performed by distributing new configuration files.

## Configuration Schemes

The configuration data for a FLEX 6000 device can be loaded with one of three configuration schemes, which is chosen on the basis of the target application. An EPC1 or EPC1441 configuration device or intelligent controller can be used to control the configuration of a FLEX 6000 device, allowing automatic configuration on system power-up.

Multiple FLEX 6000 devices can be configured in any of the three configuration schemes by connecting the configuration enable input (nCE) and configuration enable output (nCEO) pins on each device.

Table 40 shows the data sources for each configuration scheme.

<b>Configuration Scheme</b>	<b>Data Source</b>
Configuration device	EPC1 or EPC1441 configuration device
Passive serial (PS)	BitBlaster™, ByteBlasterMV™, or MasterBlaster™ download cables, or serial data source
Passive serial asynchronous (PSA)	BitBlaster, ByteBlasterMV, or MasterBlaster download cables, or serial data source



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