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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

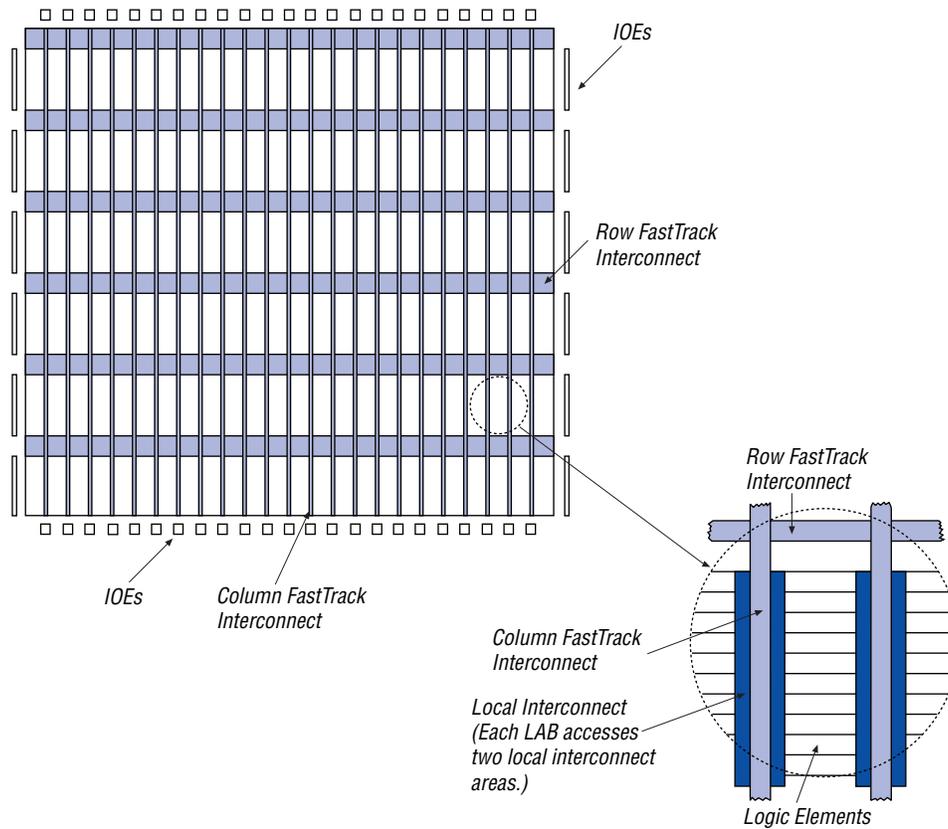
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	132
Number of Logic Elements/Cells	1320
Total RAM Bits	-
Number of I/O	81
Number of Gates	16000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-LBGA
Supplier Device Package	100-FBGA (11x11)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epf6016afc100-3

Figure 1. OptiFLEX Architecture Block Diagram



FLEX 6000 devices provide four dedicated, global inputs that drive the control inputs of the flipflops to ensure efficient distribution of high-speed, low-skew control signals. These inputs use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. These inputs can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device. The dedicated global routing structure is built into the device, eliminating the need to create a clock tree.

Logic Array Block

An LAB consists of ten LEs, their associated carry and cascade chains, the LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 6000 architecture, and facilitates efficient routing with optimum device utilization and high performance.

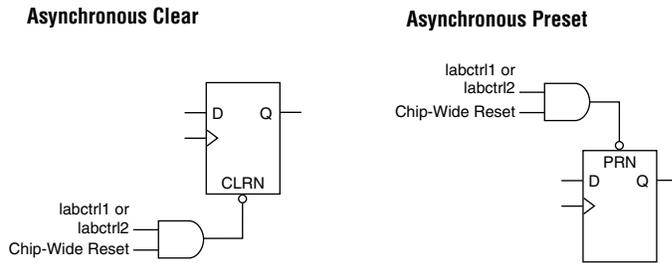
Cascade Chain

The cascade chain enables the FLEX 6000 architecture to implement very wide fan-in functions. Adjacent LUTs can be used to implement portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR gate (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 0.5 ns per LE. Cascade chain logic can be created automatically by the Altera software during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of cascade chains for the appropriate functions.

A cascade chain implementing an AND gate can use the register in the last LE; a cascade chain implementing an OR gate cannot use this register because of the inversion required to implement the OR gate.

Because the first LE of an LAB can generate control signals for that LAB, the first LE in each LAB is not included in cascade chains. Moreover, cascade chains longer than nine bits are automatically implemented by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from an even-numbered LAB to another even-numbered LAB, or from an odd-numbered LAB to another odd-numbered LAB. For example, the last LE of the first LAB in a row cascades to the second LE of the third LAB. The cascade chain does not cross the center of the row. For example, in an EPF6016 device, the cascade chain stops at the 11th LAB in a row and a new cascade chain begins at the 12th LAB.

Figure 6 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. In this example, functions of $4n$ variables are implemented with n LEs. The cascade chain requires 3.4 ns to decode a 16-bit address.

Figure 8. LE Clear & Preset Modes**Asynchronous Clear**

The flipflop can be cleared by either LABCTRL1 or LABCTRL2.

Asynchronous Preset

An asynchronous preset is implemented with an asynchronous clear. The Altera software provides preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, this technique can be used when a register drives logic or drives a pin.

In addition to the two clear and preset modes, FLEX 6000 devices provide a chip-wide reset pin (DEV_CLRn) that can reset all registers in the device. The option to use this pin is set in the Altera software before compilation. The chip-wide reset overrides all other control signals. Any register with an asynchronous preset will be preset when the chip-wide reset is asserted because of the inversion technique used to implement the asynchronous preset.

The Altera software can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses an additional three LEs per register.

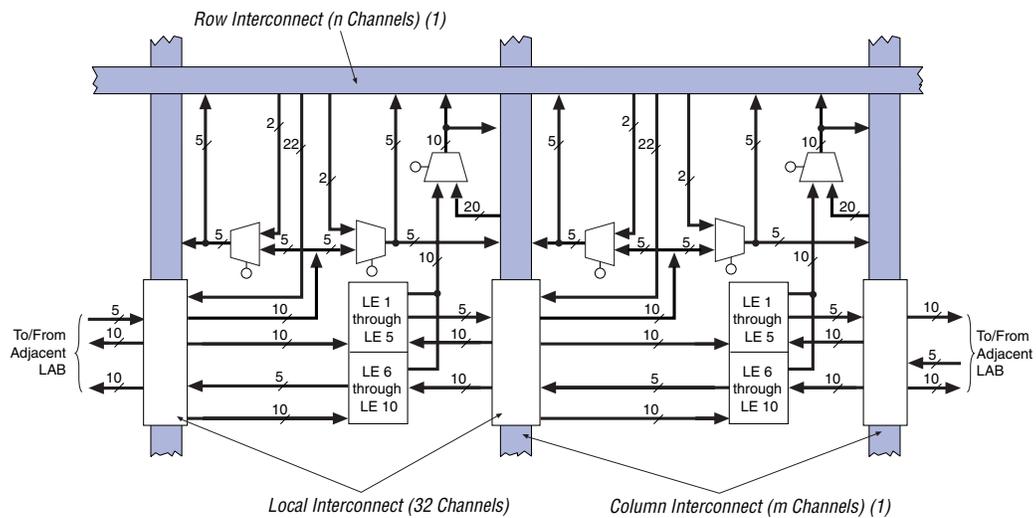
FastTrack Interconnect

In the FLEX 6000 OptiFLEX architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even for complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of column and row interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect, which routes signals between LABs in the same row, and also routes signals from I/O pins to LABs. Additionally, the local interconnect routes signals between LEs in the same LAB and in adjacent LABs. The column interconnect routes signals between rows and routes signals from I/O pins to rows.

LEs 1 through 5 of an LAB drive the local interconnect to the right, while LEs 6 through 10 drive the local interconnect to the left. The DATA1 and DATA3 inputs of each LE are driven by the local interconnect to the left; DATA2 and DATA4 are driven by the local interconnect to the right. The local interconnect also routes signals from LEs to I/O pins. Figure 9 shows an overview of the FLEX 6000 interconnect architecture. LEs in the first and last columns have drivers on both sides so that all LEs in the LAB can drive I/O pins via the local interconnect.

Figure 9. FastTrack Interconnect Architecture



Note:

- (1) For EPF6010A, EPF6016, and EPF6016A devices, $n = 144$ channels and $m = 20$ channels; for EPF6024A devices, $n = 186$ channels and $m = 30$ channels.

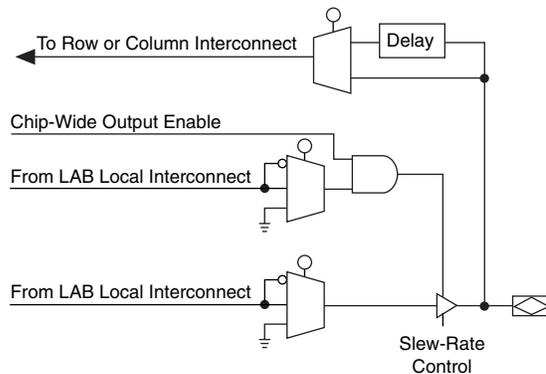
I/O Elements

An IOE contains a bidirectional I/O buffer and a tri-state buffer. IOEs can be used as input, output, or bidirectional pins. An IOE receives its data signals from the adjacent local interconnect, which can be driven by a row or column interconnect (allowing any LE in the device to drive the IOE) or by an adjacent LE (allowing fast clock-to-output delays). A FastFLEX™ I/O pin is a row or column output pin that receives its data signals from the adjacent local interconnect driven by an adjacent LE. The IOE receives its output enable signal through the same path, allowing individual output enables for every pin and permitting emulation of open-drain buffers. The Altera Compiler uses programmable inversion to invert the data or output enable signals automatically where appropriate. Open-drain emulation is provided by driving the data input low and toggling the OE of each IOE. This emulation is possible because there is one OE per pin.

A chip-wide output enable feature allows the designer to disable all pins of the device by asserting one pin (DEV_OE). This feature is useful during board debugging or testing.

Figure 12 shows the IOE block diagram.

Figure 12. IOE Block Diagram



Each IOE drives a row or column interconnect when used as an input or bidirectional pin. A row IOE can drive up to six row lines; a column IOE can drive up to two column lines. The input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time. Figure 13 shows how an IOE connects to a row interconnect, and Figure 14 shows how an IOE connects to a column interconnect.

Figure 13. IOE Connection to Row Interconnect

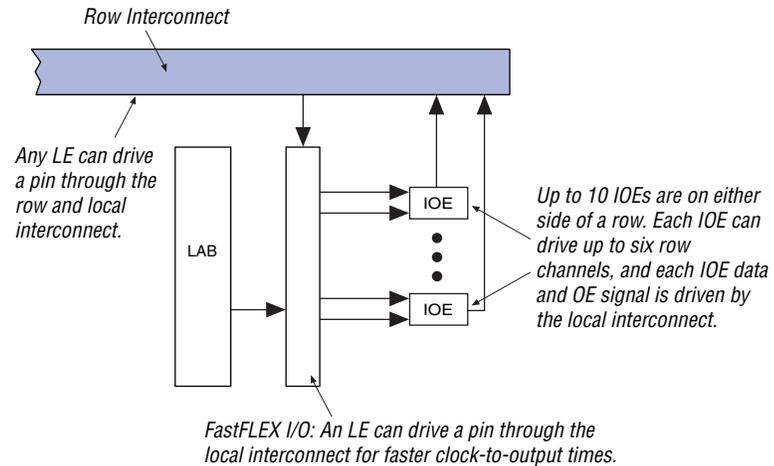
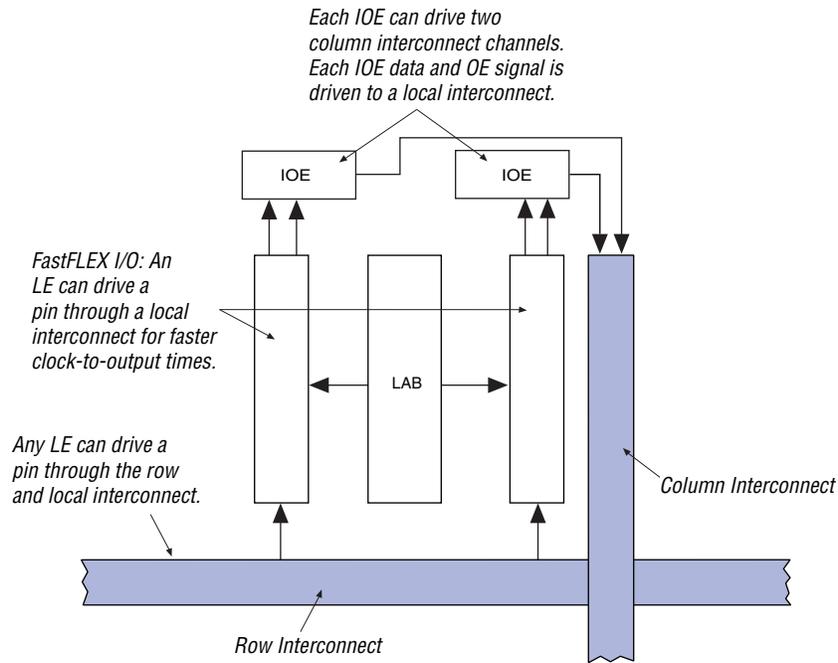


Figure 14. IOE Connection to Column Interconnect



SameFrame Pin-Outs

3.3-V FLEX 6000 devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support an EPF6016A device in a 100-pin FineLine BGA package or an EPF6024A device in a 256-pin FineLine BGA package.

The Altera software packages provide support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software packages generate pin-outs describing how to lay out a board to take advantage of this migration (see [Figure 15](#)).

Operating Conditions

Tables 11 through 18 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V and 3.3-V FLEX 6000 devices.

Table 11. FLEX 6000 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground (2)	-2.0	7.0	V
V_I	DC input voltage		-2.0	7.0	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	°C
T_{AMB}	Ambient temperature	Under bias	-65	135	°C
T_J	Junction temperature	PQFP, TQFP, and BGA packages		135	°C

Table 12. FLEX 6000 5.0-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output buffers, 5.0-V operation	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
V_I	Input voltage		-0.5	$V_{CCINT} + 0.5$	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating temperature	For commercial use	0	85	°C
		For industrial use	-40	100	°C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 15. FLEX 6000 3.3-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply voltage	With respect to ground (2)	-0.5	4.6	V
V _I	DC input voltage		-2.0	5.75	V
I _{OUT}	DC output current, per pin		-25	25	mA
T _{STG}	Storage temperature	No bias	-65	150	°C
T _{AMB}	Ambient temperature	Under bias	-65	135	°C
T _J	Junction temperature	PQFP, PLCC, and BGA packages		135	°C

Table 16. FLEX 6000 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
V _{CCIO}	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.30 (2.30)	2.70 (2.70)	V
V _I	Input voltage		-0.5	5.75	V
V _O	Output voltage		0	V _{CCIO}	V
T _J	Operating temperature	For commercial use	0	85	°C
		For industrial use	-40	100	°C
t _R	Input rise time			40	ns
t _F	Input fall time			40	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IH}	High-level input voltage		1.7		5.75	V
V _{IL}	Low-level input voltage		-0.5		0.8	V
V _{OH}	3.3-V high-level TTL output voltage	I _{OH} = -8 mA DC, V _{CCIO} = 3.00 V (7)	2.4			V
	3.3-V high-level CMOS output voltage	I _{OH} = -0.1 mA DC, V _{CCIO} = 3.00 V (7)	V _{CCIO} - 0.2			V
	2.5-V high-level output voltage	I _{OH} = -100 μA DC, V _{CCIO} = 2.30 V (7)	2.1			V
		I _{OH} = -1 mA DC, V _{CCIO} = 2.30 V (7)	2.0			V
		I _{OH} = -2 mA DC, V _{CCIO} = 2.30 V (7)	1.7			V
V _{OL}	3.3-V low-level TTL output voltage	I _{OL} = 8 mA DC, V _{CCIO} = 3.00 V (8)			0.45	V
	3.3-V low-level CMOS output voltage	I _{OL} = 0.1 mA DC, V _{CCIO} = 3.00 V (8)			0.2	V
	2.5-V low-level output voltage	I _{OL} = 100 μA DC, V _{CCIO} = 2.30 V (8)			0.2	V
		I _{OL} = 1 mA DC, V _{CCIO} = 2.30 V (8)			0.4	V
I _{OL} = 2 mA DC, V _{CCIO} = 2.30 V (8)				0.7	V	
I _I	Input pin leakage current	V _I = 5.3 V to ground (8)	-10		10	μA
I _{OZ}	Tri-stated I/O pin leakage current	V _O = 5.3 V to ground (8)	-10		10	μA
I _{CC0}	V _{CC} supply current (standby)	V _I = ground, no load		0.5	5	mA

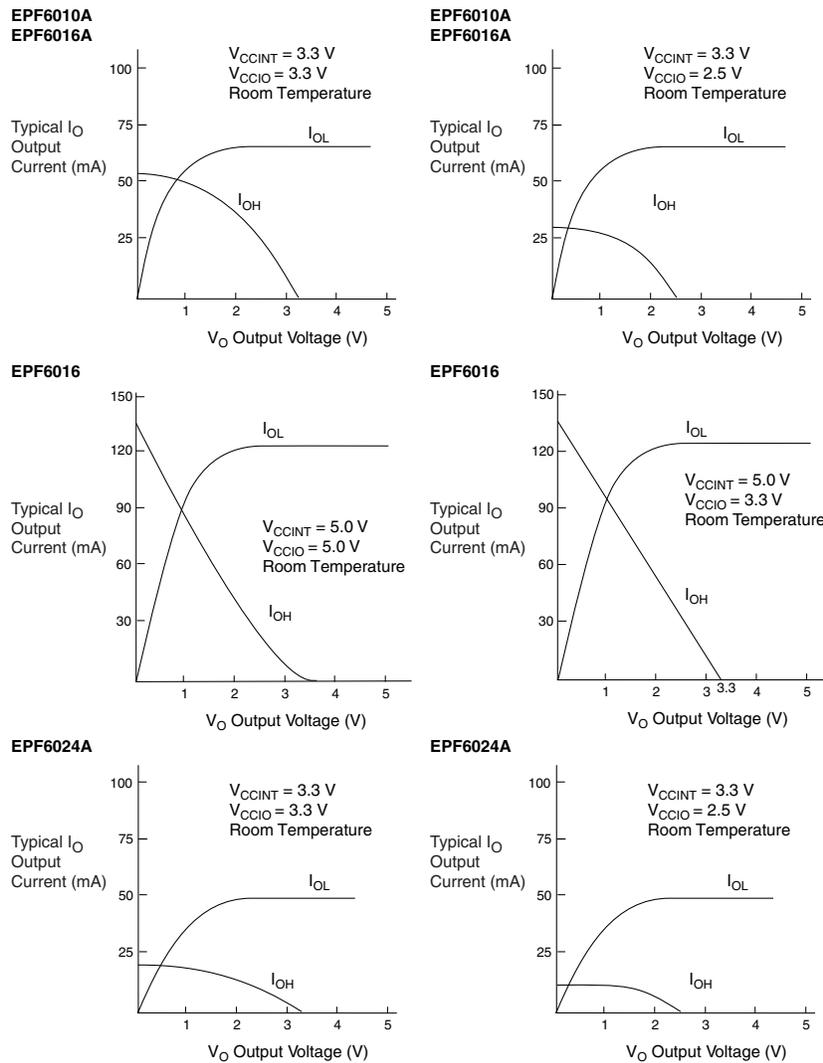
Symbol	Parameter	Conditions	Min	Max	Unit
C _{IN}	Input capacitance for I/O pin	V _{IN} = 0 V, f = 1.0 MHz		8	pF
C _{INCLK}	Input capacitance for dedicated input	V _{IN} = 0 V, f = 1.0 MHz		12	pF
C _{OUT}	Output capacitance	V _{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) The minimum DC input voltage is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
- (5) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.
- (6) These values are specified under [Table 16 on page 33](#).
- (7) The I_{OH} parameter refers to high-level TTL or CMOS output current.
- (8) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (9) Capacitance is sample-tested only.

Figure 18 shows the typical output drive characteristics of 5.0-V and 3.3-V FLEX 6000 devices with 5.0-V, 3.3-V, and 2.5-V V_{CCIO} . When $V_{CCIO} = 5.0$ V on EPF6016 devices, the output driver is compliant with the *PCI Local Bus Specification, Revision 2.2* for 5.0-V operation. When $V_{CCIO} = 3.3$ V on the EPF6010A and EPF6016A devices, the output driver is compliant with the *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation.

Figure 18. Output Drive Characteristics



Tables 19 through 21 describe the FLEX 6000 internal timing microparameters, which are expressed as worst-case values. Using hand calculations, these parameters can be used to estimate design performance. However, before committing designs to silicon, actual worst-case performance should be modeled using timing simulation and timing analysis. Tables 22 and 23 describe FLEX 6000 external timing parameters.

Symbol	Parameter	Conditions
$t_{REG_TO_REG}$	LUT delay for LE register feedback in carry chain	
$t_{CASC_TO_REG}$	Cascade-in to register delay	
$t_{CARRY_TO_REG}$	Carry-in to register delay	
$t_{DATA_TO_REG}$	LE input to register delay	
$t_{CASC_TO_OUT}$	Cascade-in to LE output delay	
$t_{CARRY_TO_OUT}$	Carry-in to LE output delay	
$t_{DATA_TO_OUT}$	LE input to LE output delay	
$t_{REG_TO_OUT}$	Register output to LE output delay	
t_{SU}	LE register setup time before clock; LE register recovery time after asynchronous clear	
t_H	LE register hold time after clock	
t_{CO}	LE register clock-to-output delay	
t_{CLR}	LE register clear delay	
t_C	LE register control signal delay	
t_{LD_CLR}	Synchronous load or clear delay in counter mode	
$t_{CARRY_TO_CARRY}$	Carry-in to carry-out delay	
$t_{REG_TO_CARRY}$	Register output to carry-out delay	
$t_{DATA_TO_CARRY}$	LE input to carry-out delay	
$t_{CARRY_TO_CASC}$	Carry-in to cascade-out delay	
$t_{CASC_TO_CASC}$	Cascade-in to cascade-out delay	
$t_{REG_TO_CASC}$	Register-out to cascade-out delay	
$t_{DATA_TO_CASC}$	LE input to cascade-out delay	
t_{CH}	LE register clock high time	
t_{CL}	LE register clock low time	

Symbol	Parameter	Conditions
t_{INSU}	Setup time with global clock at LE register	(8)
t_{INH}	Hold time with global clock at LE register	(8)
t_{OUTCO}	Clock-to-output delay with global clock with LE register using FastFLEX I/O pin	(8)

Notes to tables:

- (1) Microparameters are timing delays contributed by individual architectural elements and cannot be measured explicitly.
- (2) Operating conditions:
 $V_{CCIO} = 5.0\text{ V} \pm 5\%$ for commercial use in 5.0-V FLEX 6000 devices.
 $V_{CCIO} = 5.0\text{ V} \pm 10\%$ for industrial use in 5.0-V FLEX 6000 devices.
 $V_{CCIO} = 3.3\text{ V} \pm 10\%$ for commercial or industrial use in 3.3-V FLEX 6000 devices.
- (3) Operating conditions:
 $V_{CCIO} = 3.3\text{ V} \pm 10\%$ for commercial or industrial use in 5.0-V FLEX 6000 devices.
 $V_{CCIO} = 2.5\text{ V} \pm 0.2\text{ V}$ for commercial or industrial use in 3.3-V FLEX 6000 devices.
- (4) Operating conditions:
 $V_{CCIO} = 2.5\text{ V}, 3.3\text{ V}, \text{ or } 5.0\text{ V}.$
- (5) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
- (6) This timing parameter shows the delay of a register-to-register test pattern and is used to determine speed grades. There are 12 LEs, including source and destination registers. The row and column interconnects between the registers vary in length.
- (7) This timing parameter is shown for reference and is specified by characterization.
- (8) This timing parameter is specified by characterization.

Tables 24 through 28 show the timing information for EPF6010A and EPF6016A devices.

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{REG_TO_REG}$		1.2		1.3		1.7	ns
$t_{CASC_TO_REG}$		0.9		1.0		1.2	ns
$t_{CARRY_TO_REG}$		0.9		1.0		1.2	ns
$t_{DATA_TO_REG}$		1.1		1.2		1.5	ns
$t_{CASC_TO_OUT}$		1.3		1.4		1.8	ns
$t_{CARRY_TO_OUT}$		1.6		1.8		2.3	ns
$t_{DATA_TO_OUT}$		1.7		2.0		2.5	ns
$t_{REG_TO_OUT}$		0.4		0.4		0.5	ns
t_{SU}	0.9		1.0		1.3		ns
t_{H}	1.4		1.7		2.1		ns

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{CO}		0.3		0.4		0.4	ns
t_{CLR}		0.4		0.4		0.5	ns
t_C		1.8		2.1		2.6	ns
t_{LD_CLR}		1.8		2.1		2.6	ns
$t_{CARRY_TO_CARRY}$		0.1		0.1		0.1	ns
$t_{REG_TO_CARRY}$		1.6		1.9		2.3	ns
$t_{DATA_TO_CARRY}$		2.1		2.5		3.0	ns
$t_{CARRY_TO_CASC}$		1.0		1.1		1.4	ns
$t_{CASC_TO_CASC}$		0.5		0.6		0.7	ns
$t_{REG_TO_CASC}$		1.4		1.7		2.1	ns
$t_{DATA_TO_CASC}$		1.1		1.2		1.5	ns
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{OD1}		1.9		2.2		2.7	ns
t_{OD2}		4.1		4.8		5.8	ns
t_{OD3}		5.8		6.8		8.3	ns
t_{XZ}		1.4		1.7		2.1	ns
t_{XZ1}		1.4		1.7		2.1	ns
t_{XZ2}		3.6		4.3		5.2	ns
t_{XZ3}		5.3		6.3		7.7	ns
t_{IOE}		0.5		0.6		0.7	ns
t_{IN}		3.6		4.1		5.1	ns
t_{IN_DELAY}		4.8		5.4		6.7	ns

Table 26. Interconnect Timing Microparameters for EPF6010A & EPF6016A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LOCAL}		0.7		0.7		1.0	ns
t_{ROW}		2.9		3.2		3.2	ns
t_{COL}		1.2		1.3		1.4	ns
t_{DIN_D}		5.4		5.7		6.4	ns
t_{DIN_C}		4.3		5.0		6.1	ns
$t_{LEGLOBAL}$		2.6		3.0		3.7	ns
$t_{LABCARRY}$		0.7		0.8		0.9	ns
$t_{LABCASC}$		1.3		1.4		1.8	ns

Table 27. External Reference Timing Parameters for EPF6010A & EPF6016A Devices

Parameter	Device	Speed Grade						Unit
		-1		-2		-3		
		Min	Max	Min	Max	Min	Max	
t_1	EPF6010A		37.6		43.6		53.7	ns
	EPF6016A		38.0		44.0		54.1	ns

Table 28. External Timing Parameters for EPF6010A & EPF6016A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.1 (1)		2.4 (1)		3.3 (1)		ns
t_{INH}	0.2 (2)		0.3 (2)		0.1 (2)		ns
t_{OUTCO}	2.0	7.1	2.0	8.2	2.0	10.1	ns

Notes:

- (1) Setup times are longer when the *Increase Input Delay* option is turned on. The setup time values are shown with the *Increase Input Delay* option turned off.
- (2) Hold time is zero when the *Increase Input Delay* option is turned on.

Table 33. External Timing Parameters for EPF6016 Devices

Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
t_{INSU}	3.2		4.1		ns
t_{INH}	0.0		0.0		ns
t_{OUTCO}	2.0	7.9	2.0	9.9	ns

Tables 34 through 38 show the timing information for EPF6024A devices.

Table 34. LE Timing Microparameters for EPF6024A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{REG_TO_REG}$		1.2		1.3		1.6	ns
$t_{CASC_TO_REG}$		0.7		0.8		1.0	ns
$t_{CARRY_TO_REG}$		1.6		1.8		2.2	ns
$t_{DATA_TO_REG}$		1.3		1.4		1.7	ns
$t_{CASC_TO_OUT}$		1.2		1.3		1.6	ns
$t_{CARRY_TO_OUT}$		2.0		2.2		2.6	ns
$t_{DATA_TO_OUT}$		1.8		2.1		2.6	ns
$t_{REG_TO_OUT}$		0.3		0.3		0.4	ns
t_{SU}	0.9		1.0		1.2		ns
t_{H}	1.3		1.4		1.7		ns
t_{CO}		0.2		0.3		0.3	ns
t_{CLR}		0.3		0.3		0.4	ns
t_{C}		1.9		2.1		2.5	ns
t_{LD_CLR}		1.9		2.1		2.5	ns
$t_{CARRY_TO_CARRY}$		0.2		0.2		0.3	ns
$t_{REG_TO_CARRY}$		1.4		1.6		1.9	ns
$t_{DATA_TO_CARRY}$		1.3		1.4		1.7	ns
$t_{CARRY_TO_CASC}$		1.1		1.2		1.4	ns
$t_{CASC_TO_CASC}$		0.7		0.8		1.0	ns
$t_{REG_TO_CASC}$		1.4		1.6		1.9	ns
$t_{DATA_TO_CASC}$		1.0		1.1		1.3	ns
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

Table 35. IOE Timing Microparameters for EPF6024A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{OD1}		1.9		2.1		2.5	ns
t_{OD2}		4.0		4.4		5.3	ns
t_{OD3}		7.0		7.8		9.3	ns
t_{XZ}		4.3		4.8		5.8	ns
t_{XZ1}		4.3		4.8		5.8	ns
t_{XZ2}		6.4		7.1		8.6	ns
t_{XZ3}		9.4		10.5		12.6	ns
t_{IOE}		0.5		0.6		0.7	ns
t_{IN}		3.3		3.7		4.4	ns
t_{IN_DELAY}		5.3		5.9		7.0	ns

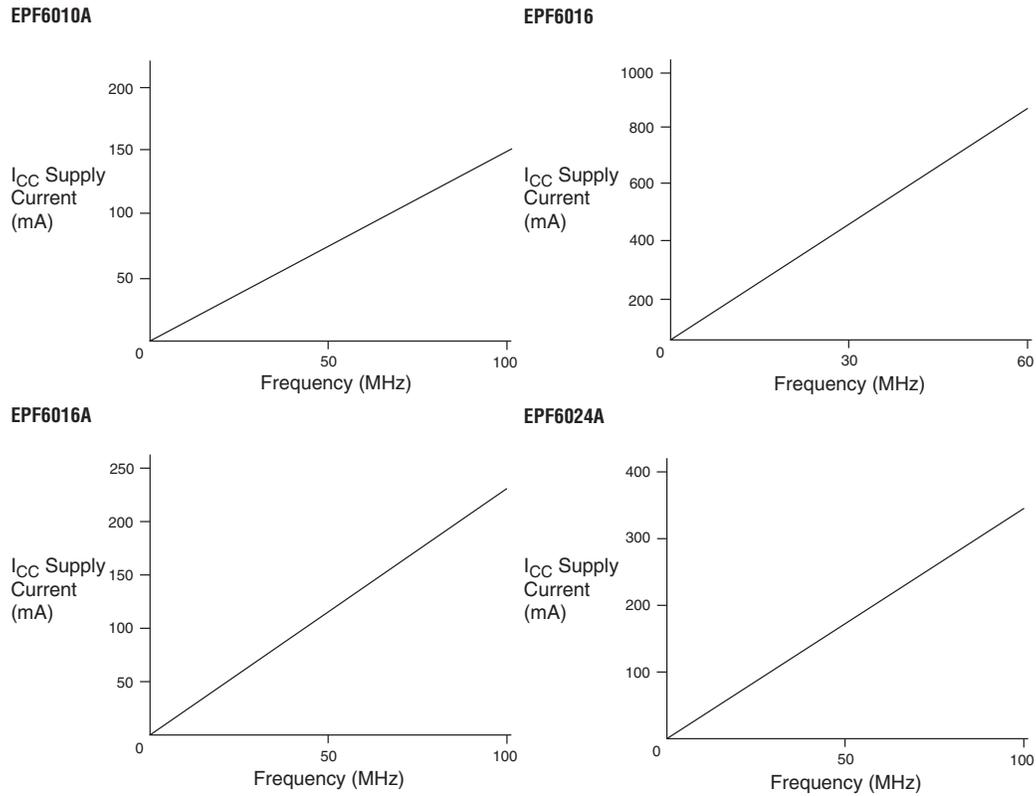
Table 36. Interconnect Timing Microparameters for EPF6024A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LOCAL}		0.8		0.8		1.1	ns
t_{ROW}		3.0		3.1		3.3	ns
t_{COL}		3.0		3.2		3.4	ns
t_{DIN_D}		5.4		5.6		6.2	ns
t_{DIN_C}		4.6		5.1		6.1	ns
$t_{LEGLOBAL}$		3.1		3.5		4.3	ns
$t_{LABCARRY}$		0.6		0.7		0.8	ns
$t_{LABCASC}$		0.3		0.3		0.4	ns

Table 37. External Reference Timing Parameters for EPF6024A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_1		45.0		50.0		60.0	ns

Figure 20. $I_{CCACTIVE}$ vs. Operating Frequency



Device Configuration & Operation

The FLEX 6000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.

- f See [Application Note 116 \(Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices\)](#) for detailed information on configuring FLEX 6000 devices, including sample schematics, timing diagrams, configuration options, pins names, and timing parameters.

Operating Modes

The FLEX 6000 architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. This process of physically loading the SRAM data into a FLEX 6000 device is known as configuration. During initialization—a process that occurs immediately after configuration—the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. The configuration and initialization processes of a device are referred to as *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 6000 devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and is used to dynamically reconfigure an entire system. Also, in-field system upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for a FLEX 6000 device can be loaded with one of three configuration schemes, which is chosen on the basis of the target application. An EPC1 or EPC1441 configuration device or intelligent controller can be used to control the configuration of a FLEX 6000 device, allowing automatic configuration on system power-up.

Multiple FLEX 6000 devices can be configured in any of the three configuration schemes by connecting the configuration enable input (nCE) and configuration enable output (nCEO) pins on each device.

Table 40 shows the data sources for each configuration scheme.

Configuration Scheme	Data Source
Configuration device	EPC1 or EPC1441 configuration device
Passive serial (PS)	BitBlaster™, ByteBlasterMV™, or MasterBlaster™ download cables, or serial data source
Passive serial asynchronous (PSA)	BitBlaster, ByteBlasterMV, or MasterBlaster download cables, or serial data source



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