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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	132
Number of Logic Elements/Cells	1320
Total RAM Bits	-
Number of I/O	171
Number of Gates	16000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf6016aqc208-2n">https://www.e-xfl.com/product-detail/intel/epf6016aqc208-2n</a>

## ...and More Features

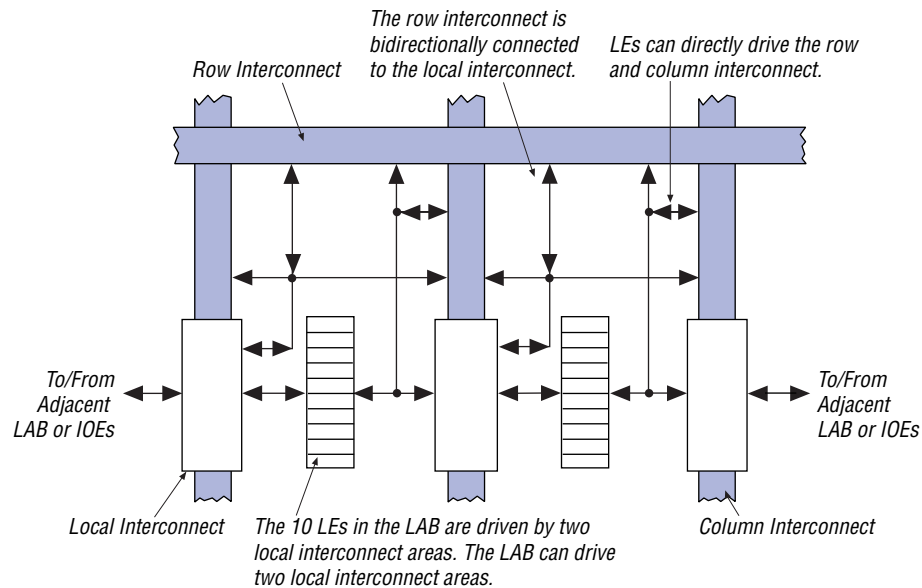
- Powerful I/O pins
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Fast path from register to I/O pin for fast clock-to-output time
- Flexible interconnect
  - FastTrack® Interconnect continuous routing structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Tri-state emulation that implements internal tri-state networks
  - Four low-skew global paths for clock, clear, preset, or logic signals
- Software design support and automatic place-and-route provided by Altera's development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800
- Flexible package options
  - Available in a variety of packages with 100 to 256 pins, including the innovative FineLine BGA™ packages (see [Table 2](#))
  - SameFrame™ pin-compatibility (with other FLEX® 6000 devices) across device densities and pin counts
  - Thin quad flat pack (TQFP), plastic quad flat pack (PQFP), and ball-grid array (BGA) packages (see [Table 2](#))
  - Footprint- and pin-compatibility with other FLEX 6000 devices in the same package
- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, the library of parameterized modules (LPM), Verilog HDL, VHDL, DesignWare components, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

**Table 2. FLEX 6000 Package Options & I/O Pin Count**

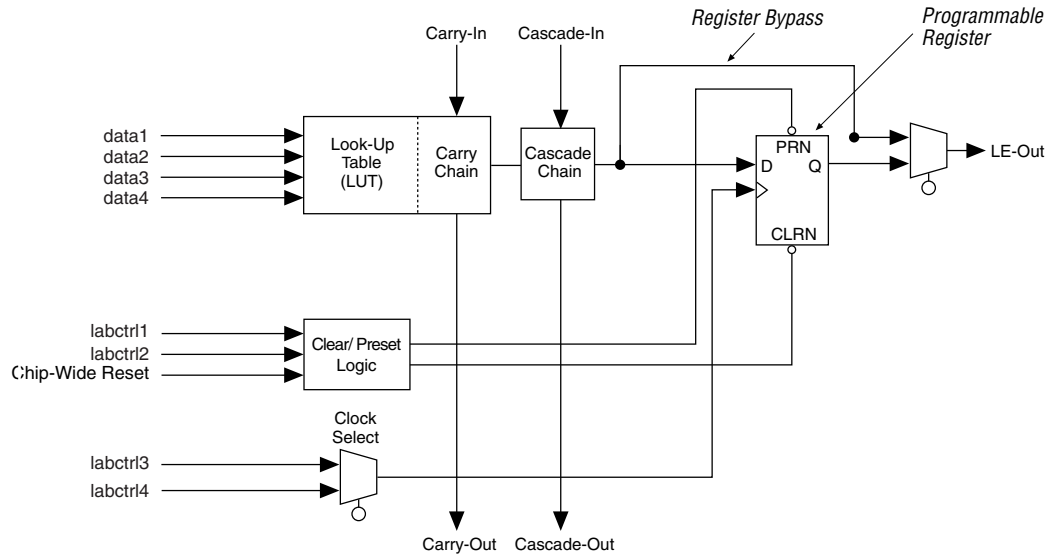
Device	100-Pin TQFP	100-Pin FineLine BGA	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin BGA	256-pin FineLine BGA
EPF6010A	71		102				
EPF6016			117	171	199	204	
EPF6016A	81	81	117	171			171
EPF6024A			117	171	199	218	219

The interleaved LAB structure—an innovative feature of the FLEX 6000 architecture—allows each LAB to drive two local interconnects. This feature minimizes the use of the FastTrack Interconnect, providing higher performance. An LAB can drive 20 LEs in adjacent LABs via the local interconnect, which maximizes fitting flexibility while minimizing die size. See [Figure 2](#).

**Figure 2. Logic Array Block**



In most designs, the registers only use global clock and clear signals. However, in some cases, other clock or asynchronous clear signals are needed. In addition, counters may also have synchronous clear or load signals. In a design that uses non-global clock and clear signals, inputs from the first LE in an LAB are re-routed to drive the control signals for that LAB. See [Figure 3](#).

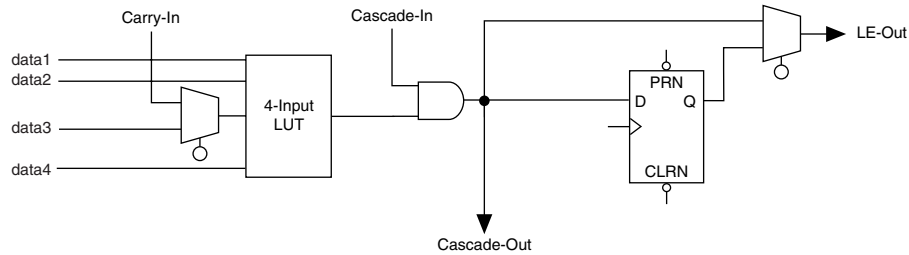
**Figure 4. Logic Element**

The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock and clear control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the flipflop is bypassed and the output of the LUT drives the outputs of the LE. The LE output can drive both the local interconnect and the FastTrack Interconnect.

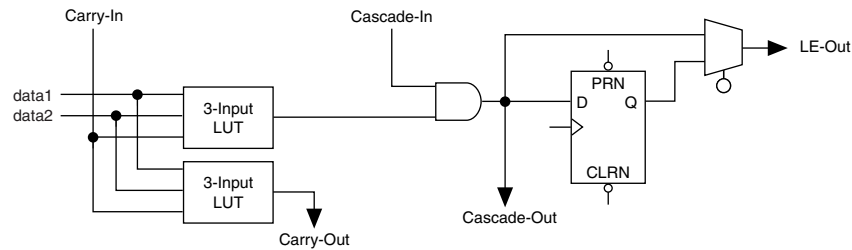
The FLEX 6000 architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equivalent comparators with minimum delay. Carry and cascade chains connect LEs 2 through 10 in an LAB and all LABs in the same half of the row. Because extensive use of carry and cascade chains can reduce routing flexibility, these chains should be limited to speed-critical portions of a design.

**Figure 7. LE Operating Modes**

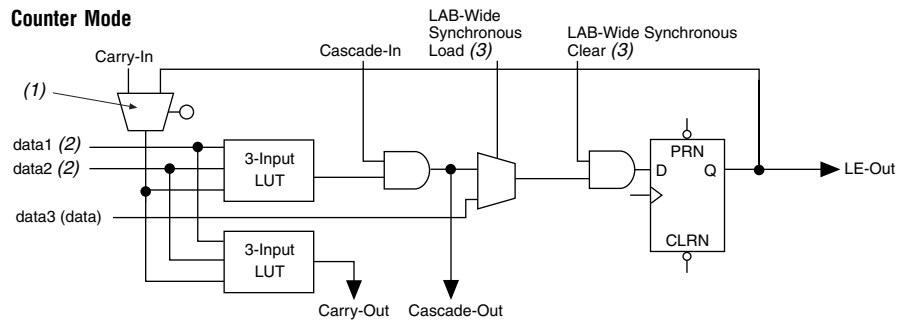
**Normal Mode**



**Arithmetic Mode**



**Counter Mode**



**Notes:**

- (1) The register feedback multiplexer is available on LE 2 of each LAB.
- (2) The data1 and data2 input signals can supply a clock enable, up or down control, or register feedback signals for all LEs other than the second LE in an LAB.
- (3) The LAB-wide synchronous clear and LAB-wide synchronous load affect all registers in an LAB.

Either the counter enable or the up/down control may be used for a given counter. Moreover, the synchronous load can be used as a count enable by routing the register output into the data input automatically when requested by the designer.

The second LE of each LAB has a special function for counter mode; the carry-in of the LE can be driven by a fast feedback path from the register. This function gives a faster counter speed for counter carry chains starting in the second LE of an LAB.

The Altera software implements functions to use the counter mode automatically where appropriate. The designer does not have to decide how the carry chain will be used.

### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

### *Clear & Preset Logic Control*

Logic for the programmable register's clear and preset functions is controlled by the LAB-wide signals LABCTRL1 and LABCTRL2. The LE register has an asynchronous clear that can implement an asynchronous preset. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear or preset. Because the clear and preset functions are active-low, the Altera software automatically assigns a logic high to an unused clear or preset signal. The clear and preset logic is implemented in either the asynchronous clear or asynchronous preset mode, which is chosen during design entry (see [Figure 8](#)).

A row channel can be driven by an LE or by one of two column channels. These three signals feed a 3-to-1 multiplexer that connects to six specific row channels. Row channels drive into the local interconnect via multiplexers.

Each column of LABs is served by a dedicated column interconnect. The LEs in an LAB can drive the column interconnect. The LEs in an LAB, a column IOE, or a row interconnect can drive the column interconnect. The column interconnect can then drive another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect must be routed to the row interconnect before it can enter an LAB.

Each LE has a FastTrack Interconnect output and a local output. The FastTrack interconnect output can drive six row and two column lines directly; the local output drives the local interconnect. Each local interconnect channel driven by an LE can drive four row and two column channels. This feature provides additional flexibility, because each LE can drive any of ten row lines and four column lines.

In addition, LEs can drive global control signals. This feature is useful for distributing internally generated clock, asynchronous clear, and asynchronous preset signals. A pin-driven global signal can also drive data signals, which is useful for high-fan-out data signals.

Each LAB drives two groups of local interconnects, which allows an LE to drive two LABs, or 20 LEs, via the local interconnect. The row-to-local multiplexers are used more efficiently, because the multiplexers can now drive two LABs. [Figure 10](#) shows how an LAB connects to row and column interconnects.

Table 5 summarizes the FastTrack Interconnect resources available in each FLEX 6000 device.

<b>Table 5. FLEX 6000 FastTrack Interconnect Resources</b>				
<b>Device</b>	<b>Rows</b>	<b>Channels per Row</b>	<b>Columns</b>	<b>Channels per Column</b>
EPF6010A	4	144	22	20
EPF6016 EPF6016A	6	144	22	20
EPF6024A	7	186	28	30

In addition to general-purpose I/O pins, FLEX 6000 devices have four dedicated input pins that provide low-skew signal distribution across the device. These four inputs can be used for global clock and asynchronous clear control signals. These signals are available as control signals for all LEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device. Using dedicated inputs to route data signals provides a fast path for high fan-out signals.

The local interconnect from LABs located at either end of two rows can drive a global control signal. For instance, in an EPF6016 device, LABs C1, D1, C22, and D22 can all drive global control signals. When an LE drives a global control signal, the dedicated input pin that drives that signal cannot be used. Any LE in the device can drive a global control signal by driving the FastTrack Interconnect into the appropriate LAB. To minimize delay, however, the Altera software places the driving LE in the appropriate LAB. The LE-driving-global signal feature is optimized for speed for control signals; regular data signals are better routed on the FastTrack Interconnect and do not receive any advantage from being routed on global signals. This LE-driving-global control signal feature is controlled by the designer and is not used automatically by the Altera software. See Figure 11.



**Table 10. JTAG Timing Parameters & Values**

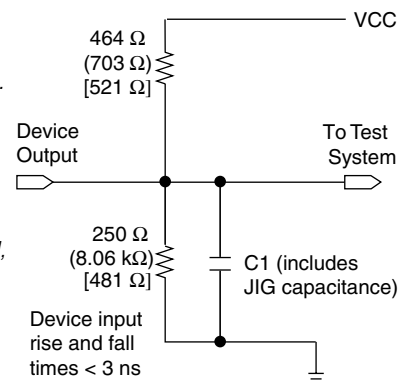
Symbol	Parameter	Min	Max	Unit
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock-to-output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock-to-output		35	ns
$t_{JSZX}$	Update register high impedance to valid output		35	ns
$t_{JSXZ}$	Update register valid output to high impedance		35	ns

## Generic Testing

Each FLEX 6000 device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 6000 devices are made under conditions equivalent to those shown in [Figure 17](#). Multiple test patterns can be used to configure devices during all stages of the production flow.

**Figure 17. AC Test Conditions**

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers without parentheses are for 5.0-V devices or outputs. Numbers in parentheses are for 3.3-V devices or outputs. Numbers in brackets are for 2.5-V devices or outputs.



## Operating Conditions

Tables 11 through 18 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V and 3.3-V FLEX 6000 devices.

**Table 11. FLEX 6000 5.0-V Device Absolute Maximum Ratings** *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply voltage	With respect to ground (2)	−2.0	7.0	V
$V_I$	DC input voltage		−2.0	7.0	V
$I_{OUT}$	DC output current, per pin		−25	25	mA
$T_{STG}$	Storage temperature	No bias	−65	150	°C
$T_{AMB}$	Ambient temperature	Under bias	−65	135	°C
$T_J$	Junction temperature	PQFP, TQFP, and BGA packages		135	°C

**Table 12. FLEX 6000 5.0-V Device Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
$V_{CCIO}$	Supply voltage for output buffers, 5.0-V operation	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
$V_I$	Input voltage		−0.5	$V_{CCINT} + 0.5$	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_J$	Operating temperature	For commercial use	0	85	°C
		For industrial use	−40	100	°C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns

**Table 13. FLEX 6000 5.0-V Device DC Operating Conditions** *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	High-level input voltage		2.0		$V_{CCINT} + 0.5$	V
$V_{IL}$	Low-level input voltage		-0.5		0.8	V
$V_{OH}$	5.0-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 4.75$ V (7)	2.4			V
	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (7)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (7)	$V_{CCIO} - 0.2$			V
$V_{OL}$	5.0-V low-level TTL output voltage	$I_{OL} = 8$ mA DC, $V_{CCIO} = 4.75$ V (8)			0.45	V
	3.3-V low-level TTL output voltage	$I_{OL} = 8$ mA DC, $V_{CCIO} = 3.00$ V (8)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (8)			0.2	V
$I_I$	Input pin leakage current	$V_I = V_{CC}$ or ground (8)	-10		10	$\mu$ A
$I_{OZ}$	Tri-stated I/O pin leakage current	$V_O = V_{CC}$ or ground (8)	-40		40	$\mu$ A
$I_{CC0}$	$V_{CC}$ supply current (standby)	$V_I =$ ground, no load		0.5	5	mA

**Table 14. FLEX 6000 5.0-V Device Capacitance** *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance for I/O pin	$V_{IN} = 0$ V, $f = 1.0$ MHz		8	pF
$C_{INCLK}$	Input capacitance for dedicated input	$V_{IN} = 0$ V, $f = 1.0$ MHz		12	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		8	pF

**Notes to tables:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum  $V_{CC}$  rise time to 100 ms.  $V_{CC}$  must rise monotonically.
- (5) Typical values are for  $T_A = 25^\circ$  C and  $V_{CC} = 5.0$  V.
- (6) These values are specified under the FLEX 6000 Recommended Operating Conditions shown in Table 12 on page 31.
- (7) The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current.
- (8) The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (9) Capacitance is sample-tested only.

**Table 15. FLEX 6000 3.3-V Device Absolute Maximum Ratings** *Note (1)*

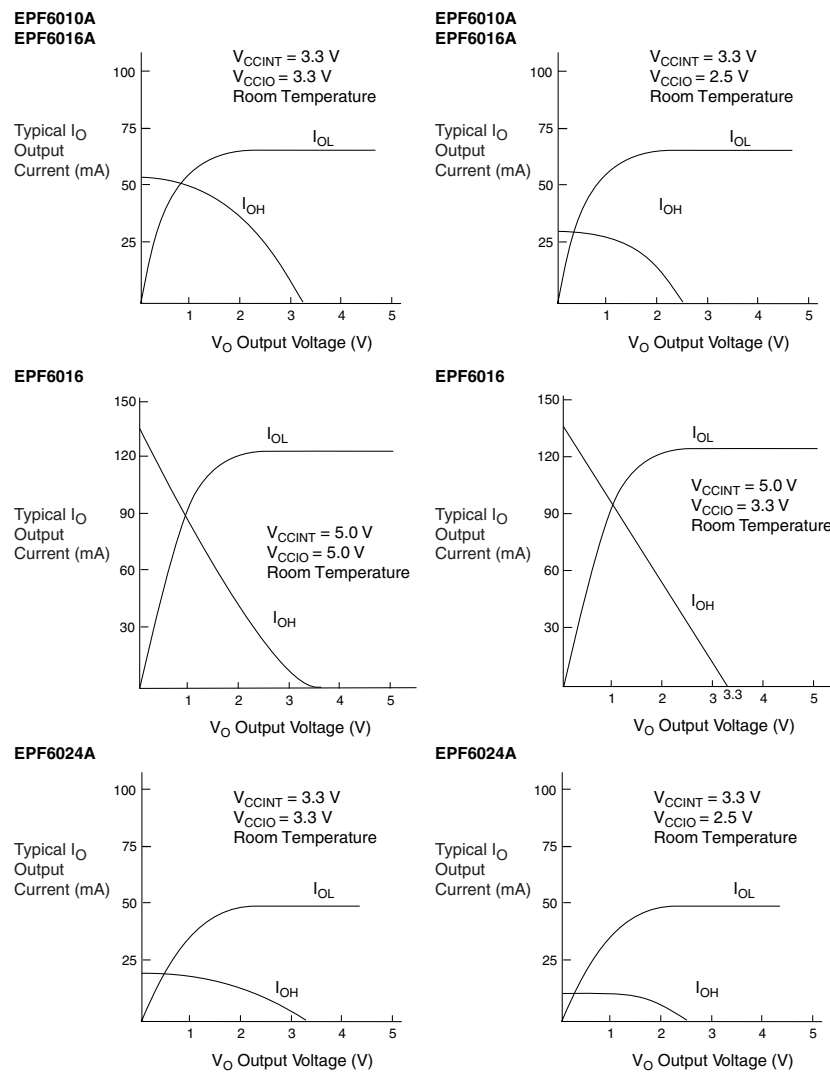
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	Supply voltage	With respect to ground (2)	−0.5	4.6	V
V <sub>I</sub>	DC input voltage		−2.0	5.75	V
I <sub>OUT</sub>	DC output current, per pin		−25	25	mA
T <sub>STG</sub>	Storage temperature	No bias	−65	150	°C
T <sub>AMB</sub>	Ambient temperature	Under bias	−65	135	°C
T <sub>J</sub>	Junction temperature	PQFP, PLCC, and BGA packages		135	°C

**Table 16. FLEX 6000 3.3-V Device Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CCINT</sub>	Supply voltage for internal logic and input buffers	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
V <sub>CCIO</sub>	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.30 (2.30)	2.70 (2.70)	V
V <sub>I</sub>	Input voltage		−0.5	5.75	V
V <sub>O</sub>	Output voltage		0	V <sub>CCIO</sub>	V
T <sub>J</sub>	Operating temperature	For commercial use	0	85	°C
		For industrial use	−40	100	°C
t <sub>R</sub>	Input rise time			40	ns
t <sub>F</sub>	Input fall time			40	ns

Figure 18 shows the typical output drive characteristics of 5.0-V and 3.3-V FLEX 6000 devices with 5.0-V, 3.3-V, and 2.5-V  $V_{CCIO}$ . When  $V_{CCIO} = 5.0$  V on EPF6016 devices, the output driver is compliant with the *PCI Local Bus Specification, Revision 2.2* for 5.0-V operation. When  $V_{CCIO} = 3.3$  V on the EPF6010A and EPF6016A devices, the output driver is compliant with the *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation.

Figure 18. Output Drive Characteristics



**Table 20. IOE Timing Microparameters** *Note (1)*

Symbol	Parameter	Conditions
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF (2)
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off, $V_{CCIO}$ = low voltage	C1 = 35 pF (3)
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF (4)
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF (2)
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off, $V_{CCIO}$ = low voltage	C1 = 35 pF (3)
$t_{ZX3}$	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF (4)
$t_{IOE}$	Output enable control delay	
$t_{IN}$	Input pad and buffer to FastTrack Interconnect delay	
$t_{IN\_DELAY}$	Input pad and buffer to FastTrack Interconnect delay with additional delay turned on	

**Table 21. Interconnect Timing Microparameters** *Note (1)*

Symbol	Parameter	Conditions
$t_{LOCAL}$	LAB local interconnect delay	
$t_{ROW}$	Row interconnect routing delay	(5)
$t_{COL}$	Column interconnect routing delay	(5)
$t_{DIN\_D}$	Dedicated input to LE data delay	(5)
$t_{DIN\_C}$	Dedicated input to LE control delay	
$t_{LEGLOBAL}$	LE output to LE control via internally-generated global signal delay	(5)
$t_{LABCARRY}$	Routing delay for the carry-out of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

**Table 22. External Reference Timing Parameters**

Symbol	Parameter	Conditions
$t_1$	Register-to-register test pattern	(6)
$t_{DRR}$	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects	(7)

<b>Table 23. External Timing Parameters</b>		
<b>Symbol</b>	<b>Parameter</b>	<b>Conditions</b>
$t_{\text{INSU}}$	Setup time with global clock at LE register	(8)
$t_{\text{INH}}$	Hold time with global clock at LE register	(8)
$t_{\text{OUTCO}}$	Clock-to-output delay with global clock with LE register using FastFLEX I/O pin	(8)

**Notes to tables:**

- (1) Microparameters are timing delays contributed by individual architectural elements and cannot be measured explicitly.
- (2) Operating conditions:  
 $V_{\text{CCIO}} = 5.0 \text{ V} \pm 5\%$  for commercial use in 5.0-V FLEX 6000 devices.  
 $V_{\text{CCIO}} = 5.0 \text{ V} \pm 10\%$  for industrial use in 5.0-V FLEX 6000 devices.  
 $V_{\text{CCIO}} = 3.3 \text{ V} \pm 10\%$  for commercial or industrial use in 3.3-V FLEX 6000 devices.
- (3) Operating conditions:  
 $V_{\text{CCIO}} = 3.3 \text{ V} \pm 10\%$  for commercial or industrial use in 5.0-V FLEX 6000 devices.  
 $V_{\text{CCIO}} = 2.5 \text{ V} \pm 0.2 \text{ V}$  for commercial or industrial use in 3.3-V FLEX 6000 devices.
- (4) Operating conditions:  
 $V_{\text{CCIO}} = 2.5 \text{ V}, 3.3 \text{ V}, \text{ or } 5.0 \text{ V}.$
- (5) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
- (6) This timing parameter shows the delay of a register-to-register test pattern and is used to determine speed grades. There are 12 LEs, including source and destination registers. The row and column interconnects between the registers vary in length.
- (7) This timing parameter is shown for reference and is specified by characterization.
- (8) This timing parameter is specified by characterization.

Tables 24 through 28 show the timing information for EPF6010A and EPF6016A devices.

Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 1 of 2)							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{REG\_TO\_REG}$		1.2		1.3		1.7	ns
$t_{CASC\_TO\_REG}$		0.9		1.0		1.2	ns
$t_{CARRY\_TO\_REG}$		0.9		1.0		1.2	ns
$t_{DATA\_TO\_REG}$		1.1		1.2		1.5	ns
$t_{CASC\_TO\_OUT}$		1.3		1.4		1.8	ns
$t_{CARRY\_TO\_OUT}$		1.6		1.8		2.3	ns
$t_{DATA\_TO\_OUT}$		1.7		2.0		2.5	ns
$t_{REG\_TO\_OUT}$		0.4		0.4		0.5	ns
$t_{SU}$	0.9		1.0		1.3		ns
$t_H$	1.4		1.7		2.1		ns

**Table 26. Interconnect Timing Microparameters for EPF6010A & EPF6016A Devices**

Table 26. Interconnect Timing Microparameters for EPF6010A & EPF6016A Devices							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{LOCAL}$		0.7		0.7		1.0	ns
$t_{ROW}$		2.9		3.2		3.2	ns
$t_{COL}$		1.2		1.3		1.4	ns
$t_{DIN\_D}$		5.4		5.7		6.4	ns
$t_{DIN\_C}$		4.3		5.0		6.1	ns
$t_{LEGLOBAL}$		2.6		3.0		3.7	ns
$t_{LABCARRY}$		0.7		0.8		0.9	ns
$t_{LABCASC}$		1.3		1.4		1.8	ns

**Table 27. External Reference Timing Parameters for EPF6010A & EPF6016A Devices**

Table 27. External Reference Timing Parameters for EPF6010A & EPF6016A Devices								
Parameter	Device	Speed Grade						Unit
		-1		-2		-3		
		Min	Max	Min	Max	Min	Max	
t <sub>1</sub>	EPF6010A		37.6		43.6		53.7	ns
	EPF6016A		38.0		44.0		54.1	ns

**Table 28. External Timing Parameters for EPF6010A & EPF6016A Devices**

Table 28. External Timing Parameters for EPF6010A & EPF6016A Devices							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	2.1 (1)		2.4 (1)		3.3 (1)		ns
t <sub>INH</sub>	0.2 (2)		0.3 (2)		0.1 (2)		ns
t <sub>OUTCO</sub>	2.0	7.1	2.0	8.2	2.0	10.1	ns

**Notes:**

- (1) Setup times are longer when the *Increase Input Delay* option is turned on. The setup time values are shown with the *Increase Input Delay* option turned off.
- (2) Hold time is zero when the *Increase Input Delay* option is turned on.



Tables 29 through 33 show the timing information for EPF6016 devices.

Table 29. LE Timing Microparameters for EPF6016 Devices					
Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
$t_{REG\_TO\_REG}$		2.2		2.8	ns
$t_{CASC\_TO\_REG}$		0.9		1.2	ns
$t_{CARRY\_TO\_REG}$		1.6		2.1	ns
$t_{DATA\_TO\_REG}$		2.4		3.0	ns
$t_{CASC\_TO\_OUT}$		1.3		1.7	ns
$t_{CARRY\_TO\_OUT}$		2.4		3.0	ns
$t_{DATA\_TO\_OUT}$		2.7		3.4	ns
$t_{REG\_TO\_OUT}$		0.3		0.5	ns
$t_{SU}$	1.1		1.6		ns
$t_H$	1.8		2.3		ns
$t_{CO}$		0.3		0.4	ns
$t_{CLR}$		0.5		0.6	ns
$t_C$		1.2		1.5	ns
$t_{LD\_CLR}$		1.2		1.5	ns
$t_{CARRY\_TO\_CARRY}$		0.2		0.4	ns
$t_{REG\_TO\_CARRY}$		0.8		1.1	ns
$t_{DATA\_TO\_CARRY}$		1.7		2.2	ns
$t_{CARRY\_TO\_CASC}$		1.7		2.2	ns
$t_{CASC\_TO\_CASC}$		0.9		1.2	ns
$t_{REG\_TO\_CASC}$		1.6		2.0	ns
$t_{DATA\_TO\_CASC}$		1.7		2.1	ns
$t_{CH}$	4.0		4.0		ns
$t_{CL}$	4.0		4.0		ns

Table 30. IOE Timing Microparameters for EPF6016 Devices					
Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
$t_{OD1}$		2.3		2.8	ns
$t_{OD2}$		4.6		5.1	ns

**Table 33. External Timing Parameters for EPF6016 Devices**

Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
t <sub>INSU</sub>	3.2		4.1		ns
t <sub>INH</sub>	0.0		0.0		ns
t <sub>OUTCO</sub>	2.0	7.9	2.0	9.9	ns

Tables 34 through 38 show the timing information for EPF6024A devices.

**Table 34. LE Timing Microparameters for EPF6024A Devices**

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{REG\_TO\_REG}$		1.2		1.3		1.6	ns
$t_{CASC\_TO\_REG}$		0.7		0.8		1.0	ns
$t_{CARRY\_TO\_REG}$		1.6		1.8		2.2	ns
$t_{DATA\_TO\_REG}$		1.3		1.4		1.7	ns
$t_{CASC\_TO\_OUT}$		1.2		1.3		1.6	ns
$t_{CARRY\_TO\_OUT}$		2.0		2.2		2.6	ns
$t_{DATA\_TO\_OUT}$		1.8		2.1		2.6	ns
$t_{REG\_TO\_OUT}$		0.3		0.3		0.4	ns
$t_{SU}$	0.9		1.0		1.2		ns
$t_H$	1.3		1.4		1.7		ns
$t_{CO}$		0.2		0.3		0.3	ns
$t_{CLR}$		0.3		0.3		0.4	ns
$t_C$		1.9		2.1		2.5	ns
$t_{LD\_CLR}$		1.9		2.1		2.5	ns
$t_{CARRY\_TO\_CARRY}$		0.2		0.2		0.3	ns
$t_{REG\_TO\_CARRY}$		1.4		1.6		1.9	ns
$t_{DATA\_TO\_CARRY}$		1.3		1.4		1.7	ns
$t_{CARRY\_TO\_CASC}$		1.1		1.2		1.4	ns
$t_{CASC\_TO\_CASC}$		0.7		0.8		1.0	ns
$t_{REG\_TO\_CASC}$		1.4		1.6		1.9	ns
$t_{DATA\_TO\_CASC}$		1.0		1.1		1.3	ns
$t_{CH}$	2.5		3.0		3.5		ns
$t_{CL}$	2.5		3.0		3.5		ns

**Table 38. External Timing Parameters for EPF6024A Devices**

Table 38. External Timing Parameters for EPF6024A Devices							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	2.0 (1)		2.2 (1)		2.6 (1)		ns
t <sub>INH</sub>	0.2 (2)		0.2 (2)		0.3 (2)		ns
t <sub>OUTCO</sub>	2.0	7.4	2.0	8.2	2.0	9.9	ns

**Notes:**

- (1) Setup times are longer when the *Increase Input Delay* option is turned on. The setup time values are shown with the *Increase Input Delay* option turned off.
- (2) Hold time is zero when the *Increase Input Delay* option is turned on.

## Power Consumption

The supply power (P) for FLEX 6000 devices can be calculated with the following equations:

$$P = P_{\text{INT}} + P_{\text{IO}}$$

$$P = (I_{\text{CCSTANDBY}} + I_{\text{CCACTIVE}}) \times V_{\text{CC}} + P_{\text{IO}}$$

Typical  $I_{\text{CCSTANDBY}}$  values are shown as  $I_{\text{CC0}}$  in the “FLEX 6000 Device DC Operating Conditions” table on [pages 31 and 33](#) of this data sheet. The  $I_{\text{CCACTIVE}}$  value depends on the switching frequency and the application logic. This value is based on the amount of current that each LE typically consumes. The  $P_{\text{IO}}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#).

The  $I_{\text{CCACTIVE}}$  value can be calculated with the following equation:

$$I_{\text{CCACTIVE}} = K \times f_{\text{MAX}} \times N \times \text{tog}_{\text{LC}} \times \frac{\mu\text{A}}{\text{MHz} \times \text{LE}}$$

Where:

$f_{\text{MAX}}$  = Maximum operating frequency in MHz

$N$  = Total number of LEs used in a FLEX 6000 device

$\text{tog}_{\text{LC}}$  = Average percentage of LEs toggling at each clock (typically 12.5%)

$K$  = Constant, shown in [Table 39](#)

**Table 39. K Constant Values**

Device	K Value
EPF6010A	14
EPF6016	88
EPF6016A	14
EPF6024A	14

## Operating Modes

The FLEX 6000 architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. This process of physically loading the SRAM data into a FLEX 6000 device is known as configuration. During initialization—a process that occurs immediately after configuration—the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. The configuration and initialization processes of a device are referred to as *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 6000 devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and is used to dynamically reconfigure an entire system. Also, in-field system upgrades can be performed by distributing new configuration files.

## Configuration Schemes

The configuration data for a FLEX 6000 device can be loaded with one of three configuration schemes, which is chosen on the basis of the target application. An EPC1 or EPC1441 configuration device or intelligent controller can be used to control the configuration of a FLEX 6000 device, allowing automatic configuration on system power-up.

Multiple FLEX 6000 devices can be configured in any of the three configuration schemes by connecting the configuration enable input (nCE) and configuration enable output (nCEO) pins on each device.

Table 40 shows the data sources for each configuration scheme.

<b>Table 40. Configuration Schemes</b>	
<b>Configuration Scheme</b>	<b>Data Source</b>
Configuration device	EPC1 or EPC1441 configuration device
Passive serial (PS)	BitBlaster™, ByteBlasterMV™, or MasterBlaster™ download cables, or serial data source
Passive serial asynchronous (PSA)	BitBlaster, ByteBlasterMV, or MasterBlaster download cables, or serial data source

## Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.