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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 132 |
| Number of Logic Elements/Cells | 1320 |
| Total RAM Bits | - |
| Number of I/O | 171 |
| Number of Gates | 16000 |
| Voltage - Supply | 3V ~ 3.6V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf6016aqi208-2 |

Table 4 shows FLEX 6000 performance for more complex designs.

*Table 4. FLEX 6000 Device Performance for Complex Designs* *Note (1)*

| Application | LEs Used | Performance | | | Units |
|---|---|---|---|---|---|
| | | -1 Speed Grade | -2 Speed Grade | -3 Speed Grade | |
| 8-bit, 16-tap parallel finite impulse response (FIR) filter | 599 | 94 | 80 | 72 | MSPS |
| 8-bit, 512-point fast Fourier transform (FFT) function | 1,182 | 75<br>63 | 89<br>53 | 109<br>43 | µS<br>MHz |
| a16450 universal asynchronous receiver/transmitter (UART) | 487 | 36 | 30 | 25 | MHz |
| PCI bus target with zero wait states | 609 | 56 | 49 | 42 | MHz |

*Note:*
(1) The applications in this table were created using Altera MegaCore™ functions.

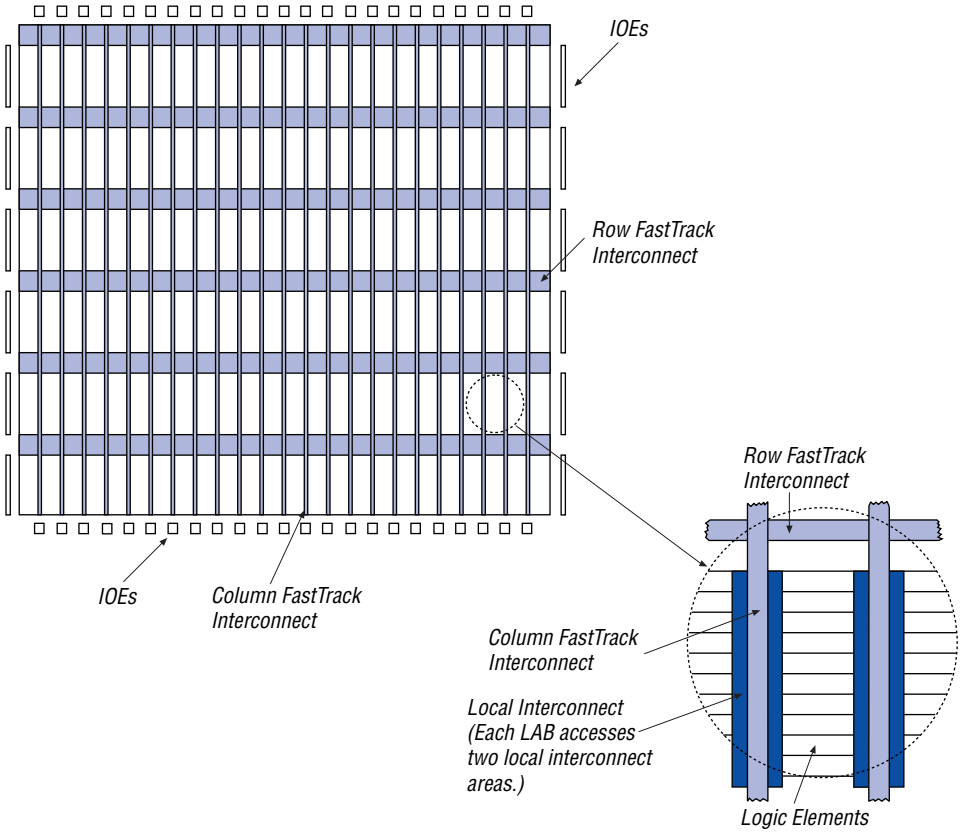
FLEX 6000 devices are supported by Altera development systems; a single, integrated package that offers schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development systems include DesignWare functions that are optimized for the FLEX 6000 architecture.

The Altera development system runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800.

f See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet* for more information.

*Figure 1. OptiFLEX Architecture Block Diagram*



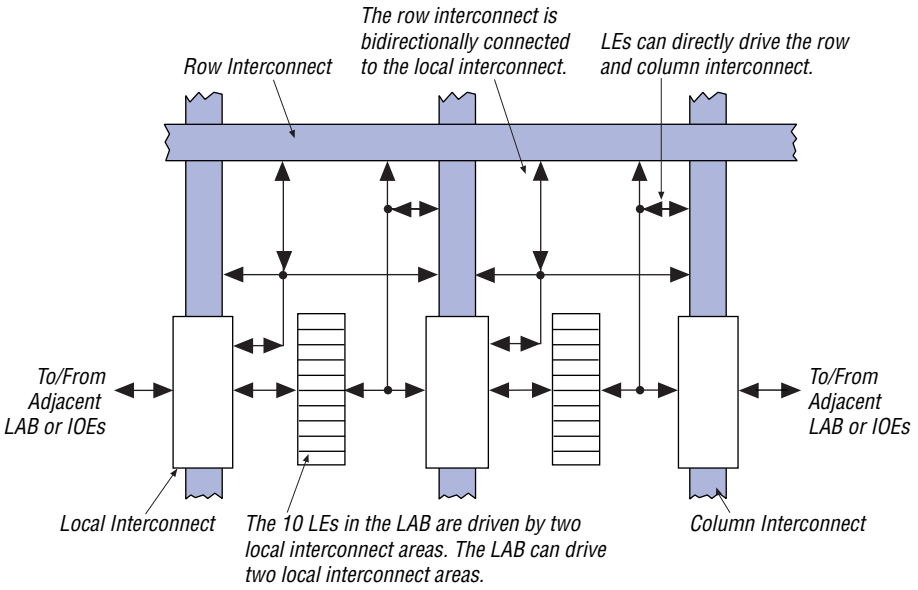

FLEX 6000 devices provide four dedicated, global inputs that drive the control inputs of the flipflops to ensure efficient distribution of high-speed, low-skew control signals. These inputs use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. These inputs can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device. The dedicated global routing structure is built into the device, eliminating the need to create a clock tree.

## Logic Array Block

An LAB consists of ten LEs, their associated carry and cascade chains, the LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 6000 architecture, and facilitates efficient routing with optimum device utilization and high performance.

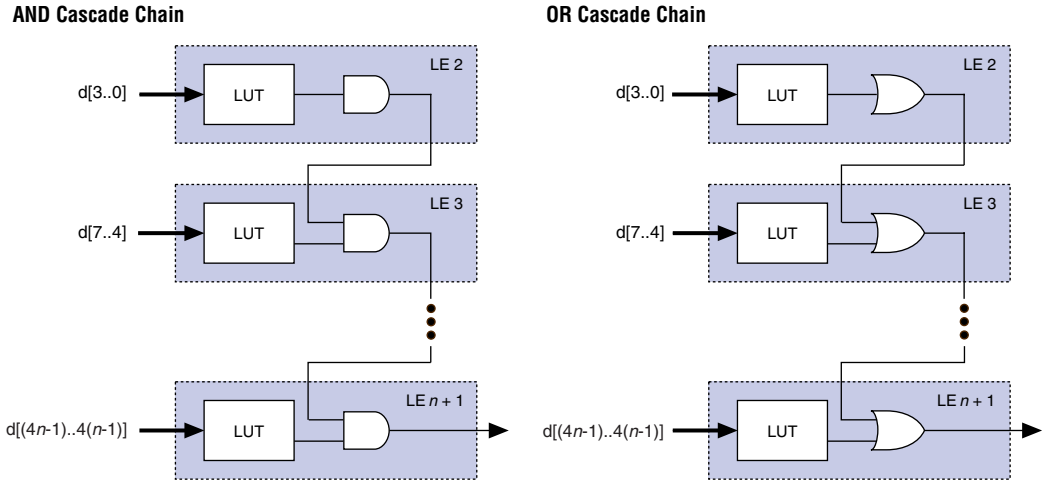
The interleaved LAB structure—an innovative feature of the FLEX 6000 architecture—allows each LAB to drive two local interconnects. This feature minimizes the use of the FastTrack Interconnect, providing higher performance. An LAB can drive 20 LEs in adjacent LABs via the local interconnect, which maximizes fitting flexibility while minimizing die size. See Figure 2.

*Figure 2. Logic Array Block*




In most designs, the registers only use global clock and clear signals. However, in some cases, other clock or asynchronous clear signals are needed. In addition, counters may also have synchronous clear or load signals. In a design that uses non-global clock and clear signals, inputs from the first LE in an LAB are re-routed to drive the control signals for that LAB. See Figure 3.

*Figure 6. Cascade Chain Operation*




## LE Operating Modes

The FLEX 6000 LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

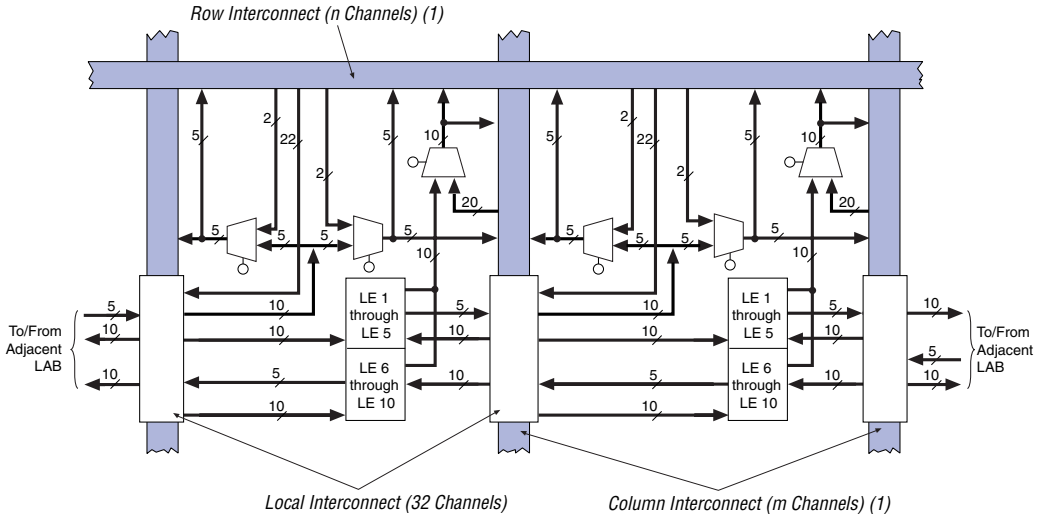
Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, synchronous clear, and synchronous load control for the register. The Altera software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions to use an LE operating mode for optimal performance.

Figure 7 shows the LE operating modes.

The FastTrack Interconnect consists of column and row interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect, which routes signals between LABs in the same row, and also routes signals from I/O pins to LABs. Additionally, the local interconnect routes signals between LEs in the same LAB and in adjacent LABs. The column interconnect routes signals between rows and routes signals from I/O pins to rows.

LEs 1 through 5 of an LAB drive the local interconnect to the right, while LEs 6 through 10 drive the local interconnect to the left. The `DATA1` and `DATA3` inputs of each LE are driven by the local interconnect to the left; `DATA2` and `DATA4` are driven by the local interconnect to the right. The local interconnect also routes signals from LEs to I/O pins. Figure 9 shows an overview of the FLEX 6000 interconnect architecture. LEs in the first and last columns have drivers on both sides so that all LEs in the LAB can drive I/O pins via the local interconnect.

***Figure 9. FastTrack Interconnect Architecture***




*Note:*

(1) For EPF6010A, EPF6016, and EPF6016A devices, $n$ = 144 channels and $m$ = 20 channels; for EPF6024A devices, $n$ = 186 channels and $m$ = 30 channels.

A row channel can be driven by an LE or by one of two column channels. These three signals feed a 3-to-1 multiplexer that connects to six specific row channels. Row channels drive into the local interconnect via multiplexers.

Each column of LABs is served by a dedicated column interconnect. The LEs in an LAB can drive the column interconnect. The LEs in an LAB, a column IOE, or a row interconnect can drive the column interconnect. The column interconnect can then drive another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect must be routed to the row interconnect before it can enter an LAB.

Each LE has a FastTrack Interconnect output and a local output. The FastTrack interconnect output can drive six row and two column lines directly; the local output drives the local interconnect. Each local interconnect channel driven by an LE can drive four row and two column channels. This feature provides additional flexibility, because each LE can drive any of ten row lines and four column lines.

In addition, LEs can drive global control signals. This feature is useful for distributing internally generated clock, asynchronous clear, and asynchronous preset signals. A pin-driven global signal can also drive data signals, which is useful for high-fan-out data signals.

Each LAB drives two groups of local interconnects, which allows an LE to drive two LABs, or 20 LEs, via the local interconnect. The row-to-local multiplexers are used more efficiently, because the multiplexers can now drive two LABs. Figure 10 shows how an LAB connects to row and column interconnects.

Table 5 summarizes the FastTrack Interconnect resources available in each FLEX 6000 device.

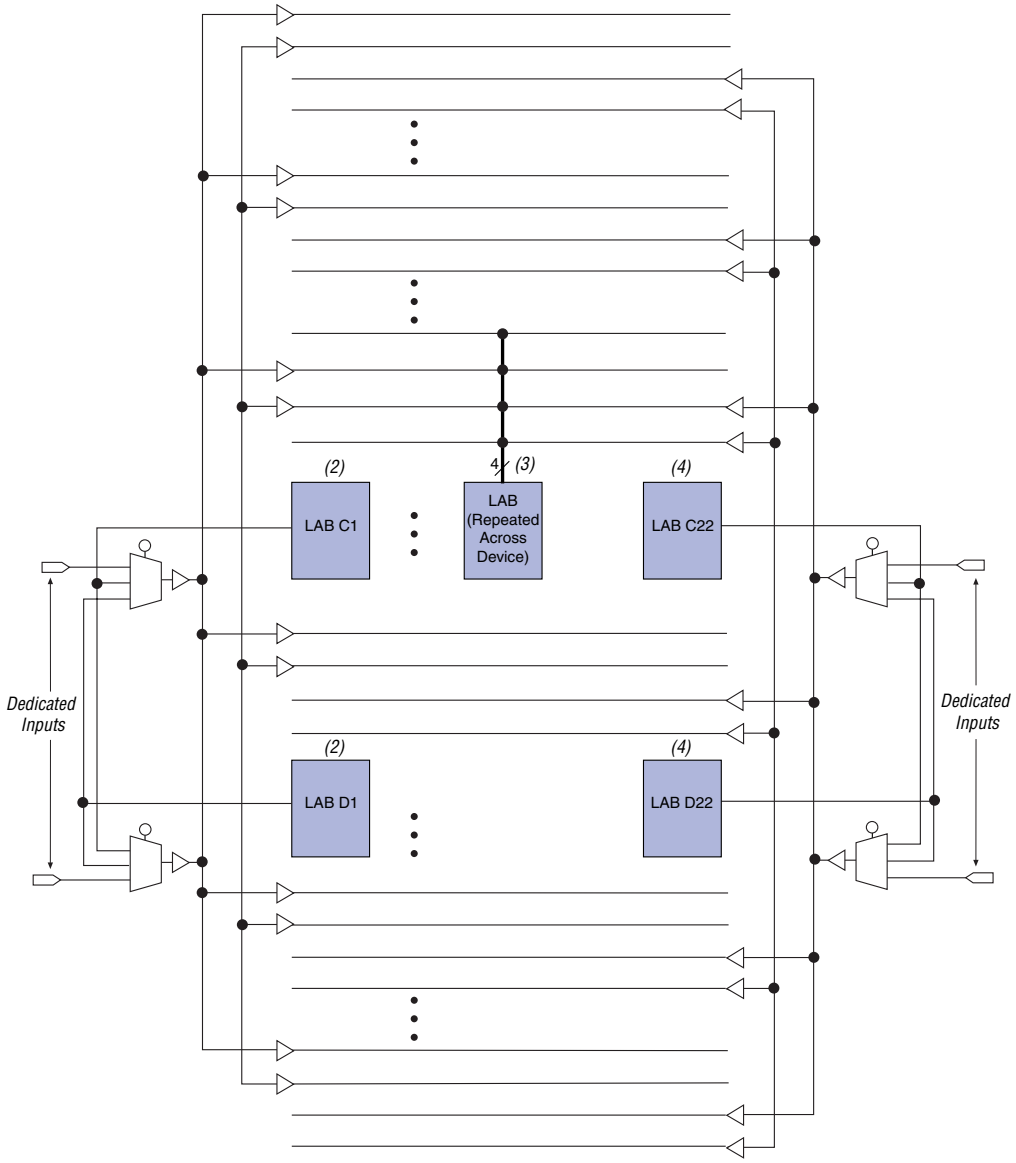
*Table 5. FLEX 6000 FastTrack Interconnect Resources*

| Device | Rows | Channels per Row | Columns | Channels per Column |
|---|---|---|---|---|
| EPF6010A | 4 | 144 | 22 | 20 |
| EPF6016<br>EPF6016A | 6 | 144 | 22 | 20 |
| EPF6024A | 7 | 186 | 28 | 30 |

In addition to general-purpose I/O pins, FLEX 6000 devices have four dedicated input pins that provide low-skew signal distribution across the device. These four inputs can be used for global clock and asynchronous clear control signals. These signals are available as control signals for all LEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device. Using dedicated inputs to route data signals provides a fast path for high fan-out signals.

The local interconnect from LABs located at either end of two rows can drive a global control signal. For instance, in an EPF6016 device, LABs C1, D1, C22, and D22 can all drive global control signals. When an LE drives a global control signal, the dedicated input pin that drives that signal cannot be used. Any LE in the device can drive a global control signal by driving the FastTrack Interconnect into the appropriate LAB. To minimize delay, however, the Altera software places the driving LE in the appropriate LAB. The LE-driving-global signal feature is optimized for speed for control signals; regular data signals are better routed on the FastTrack Interconnect and do not receive any advantage from being routed on global signals. This LE-driving-global control signal feature is controlled by the designer and is not used automatically by the Altera software. See Figure 11.

***Figure 11. Global Clock & Clear Distribution*** *Note (1)*




*Notes:*

(1) The global clock and clear distribution signals are shown for EPF6016 and EPF6016A devices. In EPF6010A devices, LABs in rows B and C drive global signals. In EPF6024A devices, LABs in rows C and E drive global signals.
(2) The local interconnect from LABs C1 and D1 can drive two global control signals on the left side.
(3) Global signals drive into every LAB as clock, asynchronous clear, preset, and data signals.
(4) The local interconnect from LABs C22 and D22 can drive two global control signals on the right side.

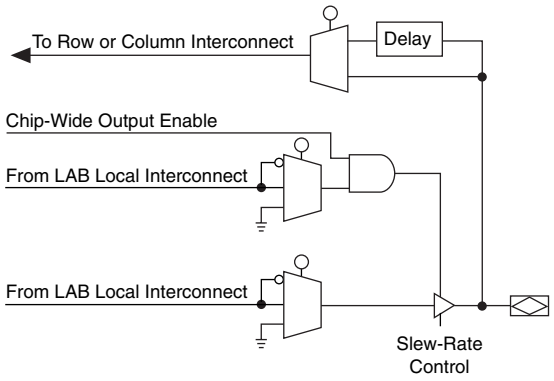
## I/O Elements

An IOE contains a bidirectional I/O buffer and a tri-state buffer. IOEs can be used as input, output, or bidirectional pins. An IOE receives its data signals from the adjacent local interconnect, which can be driven by a row or column interconnect (allowing any LE in the device to drive the IOE) or by an adjacent LE (allowing fast clock-to-output delays). A FastFLEX™ I/O pin is a row or column output pin that receives its data signals from the adjacent local interconnect driven by an adjacent LE. The IOE receives its output enable signal through the same path, allowing individual output enables for every pin and permitting emulation of open-drain buffers. The Altera Compiler uses programmable inversion to invert the data or output enable signals automatically where appropriate. Open-drain emulation is provided by driving the data input low and toggling the OE of each IOE. This emulation is possible because there is one OE per pin.

A chip-wide output enable feature allows the designer to disable all pins of the device by asserting one pin (DEV_OE). This feature is useful during board debugging or testing.

Figure 12 shows the IOE block diagram.

*Figure 12. IOE Block Diagram*



Each IOE drives a row or column interconnect when used as an input or bidirectional pin. A row IOE can drive up to six row lines; a column IOE can drive up to two column lines. The input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time. Figure 13 shows how an IOE connects to a row interconnect, and Figure 14 shows how an IOE connects to a column interconnect.

***Figure 13. IOE Connection to Row Interconnect***

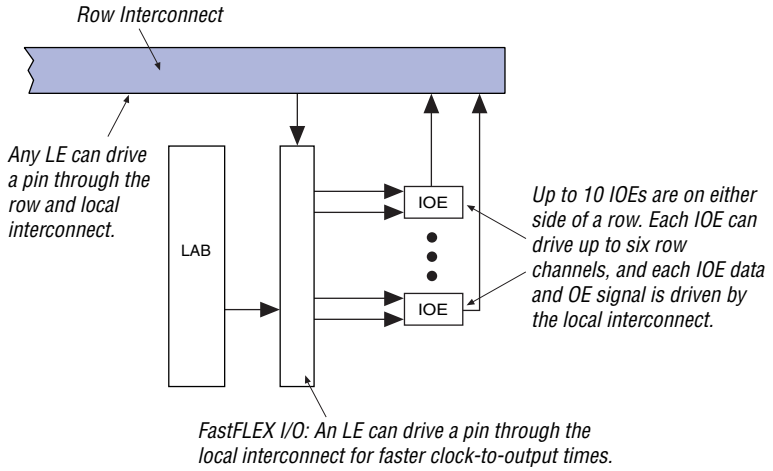
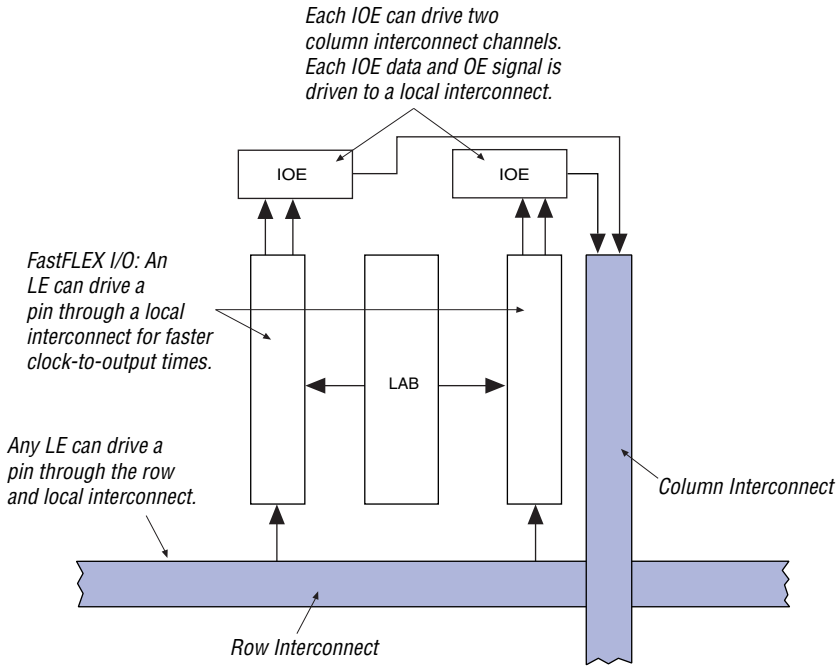


*Figure 14. IOE Connection to Column Interconnect*




## SameFrame Pin-Outs

3.3-V FLEX 6000 devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support an EPF6016A device in a 100-pin FineLine BGA package or an EPF6024A device in a 256-pin FineLine BGA package.

The Altera software packages provide support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software packages generate pin-outs describing how to lay out a board to take advantage of this migration (see Figure 15).

*Table 10. JTAG Timing Parameters & Values*

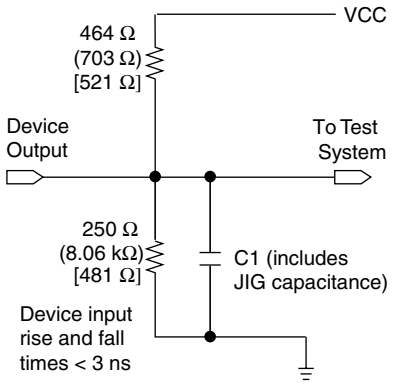
| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock-to-output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock-to-output | | 35 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 35 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 35 | ns |

## Generic Testing

Each FLEX 6000 device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 6000 devices are made under conditions equivalent to those shown in Figure 17. Multiple test patterns can be used to configure devices during all stages of the production flow.

*Figure 17. AC Test Conditions*

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers without parentheses are for 5.0-V devices or outputs. Numbers in parentheses are for 3.3-V devices or outputs. Numbers in brackets are for 2.5-V devices or outputs.*



## Operating Conditions

Tables 11 through 18 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V and 3.3-V FLEX 6000 devices.

*Table 11. FLEX 6000 5.0-V Device Absolute Maximum Ratings* *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to ground *(2)* | –2.0 | 7.0 | V |
| $V_I$ | DC input voltage | | –2.0 | 7.0 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, TQFP, and BGA packages | | 135 | ° C |

*Table 12. FLEX 6000 5.0-V Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 5.0-V operation | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| $V_I$ | Input voltage | | –0.5 | $V_{CCINT}$ + 0.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_J$ | Operating temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Figure 19. FLEX 6000 Timing Model*

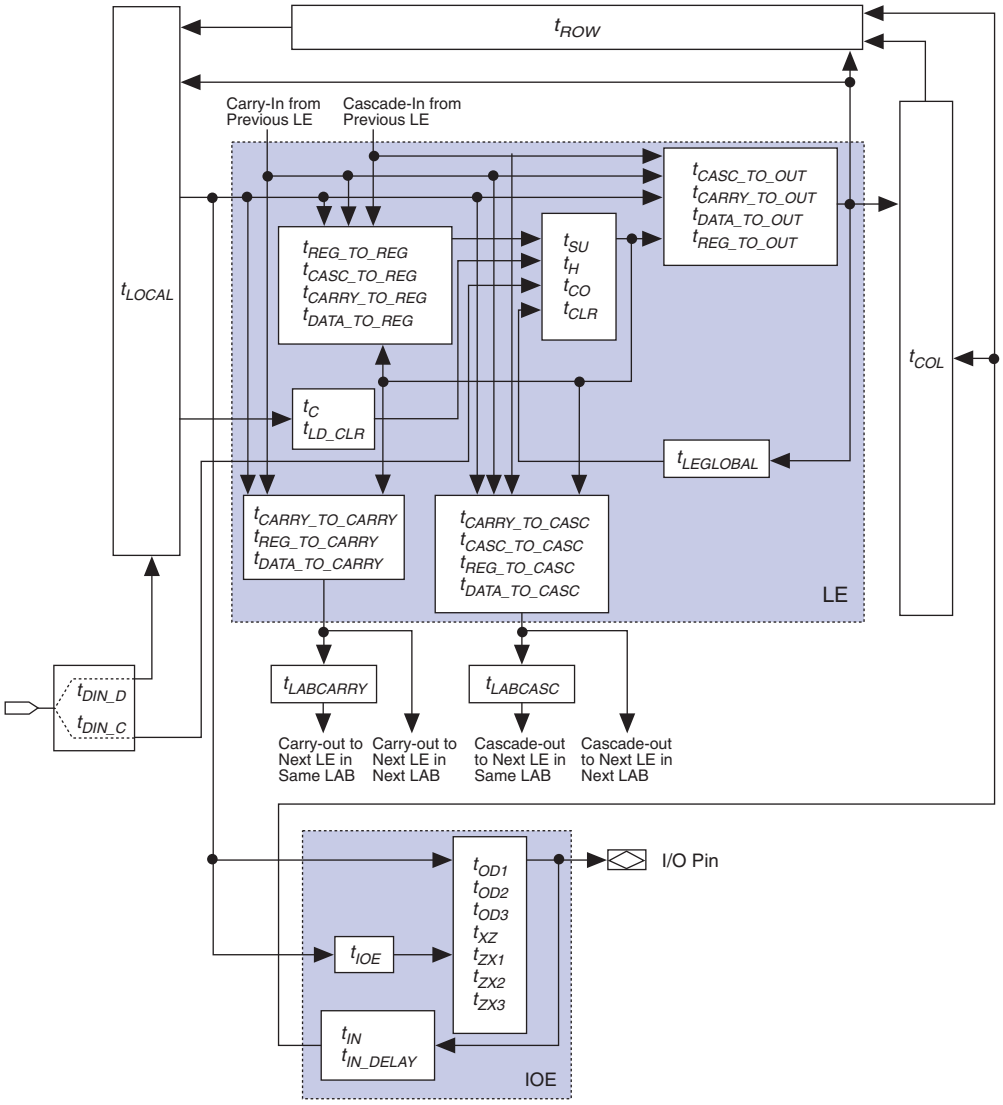


*Table 20. IOE Timing Microparameters* *Note (1)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$ | C1 = 35 pF *(2)* |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off, $V_{CCIO}$ = low voltage | C1 = 35 pF *(3)* |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on | C1 = 35 pF *(4)* |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$ | C1 = 35 pF *(2)* |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off, $V_{CCIO}$ = low voltage | C1 = 35 pF *(3)* |
| $t_{ZX3}$ | IOE output buffer enable delay, slow slew rate = on | C1 = 35 pF *(4)* |
| $t_{IOE}$ | Output enable control delay | |
| $t_{IN}$ | Input pad and buffer to FastTrack Interconnect delay | |
| $t_{IN\_DELAY}$ | Input pad and buffer to FastTrack Interconnect delay with additional delay turned on | |

*Table 21. Interconnect Timing Microparameters* *Note (1)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{LOCAL}$ | LAB local interconnect delay | |
| $t_{ROW}$ | Row interconnect routing delay | *(5)* |
| $t_{COL}$ | Column interconnect routing delay | *(5)* |
| $t_{DIN\_D}$ | Dedicated input to LE data delay | *(5)* |
| $t_{DIN\_C}$ | Dedicated input to LE control delay | |
| $t_{LEGLOBAL}$ | LE output to LE control via internally-generated global signal delay | *(5)* |
| $t_{LABCARRY}$ | Routing delay for the carry-out of an LE driving the carry-in signal of a different LE in a different LAB | |
| $t_{LABCASC}$ | Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB | |

*Table 22. External Reference Timing Parameters*

| Symbol | Parameter | Conditions |
|---|---|---|
| $\mathbf{t_1}$ | Register-to-register test pattern | *(6)* |
| $\mathbf{t_{DRR}}$ | Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects | *(7)* |

| Table 23. External Timing Parameters | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{INSU}$ | Setup time with global clock at LE register | *(8)* |
| $t_{INH}$ | Hold time with global clock at LE register | *(8)* |
| $t_{OUTCO}$ | Clock-to-output delay with global clock with LE register using FastFLEX I/O pin | *(8)* |

*Notes to tables:*

(1) Microparameters are timing delays contributed by individual architectural elements and cannot be measured explicitly.
(2) Operating conditions:
$V_{CCIO}$ = 5.0 V ±5% for commercial use in 5.0-V FLEX 6000 devices.
$V_{CCIO}$ = 5.0 V ±10% for industrial use in 5.0-V FLEX 6000 devices.
$V_{CCIO}$ = 3.3 V ±10% for commercial or industrial use in 3.3-V FLEX 6000 devices.
(3) Operating conditions:
$V_{CCIO}$ = 3.3 V ±10% for commercial or industrial use in 5.0-V FLEX 6000 devices.
$V_{CCIO}$ = 2.5 V ±0.2 V for commercial or industrial use in 3.3-V FLEX 6000 devices.
(4) Operating conditions:
$V_{CCIO}$ = 2.5 V, 3.3 V, or 5.0 V.
(5) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
(6) This timing parameter shows the delay of a register-to-register test pattern and is used to determine speed grades. There are 12 LEs, including source and destination registers. The row and column interconnects between the registers vary in length.
(7) This timing parameter is shown for reference and is specified by characterization.
(8) This timing parameter is specified by characterization.

Tables 24 through 28 show the timing information for EPF6010A and EPF6016A devices.

| Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 1 of 2) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Speed Grade** | | | | | | **Unit** |
| | **-1** | | **-2** | | **-3** | | |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{REG\_TO\_REG}$ | | 1.2 | | 1.3 | | 1.7 | ns |
| $t_{CASC\_TO\_REG}$ | | 0.9 | | 1.0 | | 1.2 | ns |
| $t_{CARRY\_TO\_REG}$ | | 0.9 | | 1.0 | | 1.2 | ns |
| $t_{DATA\_TO\_REG}$ | | 1.1 | | 1.2 | | 1.5 | ns |
| $t_{CASC\_TO\_OUT}$ | | 1.3 | | 1.4 | | 1.8 | ns |
| $t_{CARRY\_TO\_OUT}$ | | 1.6 | | 1.8 | | 2.3 | ns |
| $t_{DATA\_TO\_OUT}$ | | 1.7 | | 2.0 | | 2.5 | ns |
| $t_{REG\_TO\_OUT}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{SU}$ | 0.9 | | 1.0 | | 1.3 | | ns |
| $t_{H}$ | 1.4 | | 1.7 | | 2.1 | | ns |

*Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 2 of 2)*

| Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{CO}$ | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{CLR}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{C}$ | | 1.8 | | 2.1 | | 2.6 | ns |
| $t_{LD\_CLR}$ | | 1.8 | | 2.1 | | 2.6 | ns |
| $t_{CARRY\_TO\_CARRY}$ | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{REG\_TO\_CARRY}$ | | 1.6 | | 1.9 | | 2.3 | ns |
| $t_{DATA\_TO\_CARRY}$ | | 2.1 | | 2.5 | | 3.0 | ns |
| $t_{CARRY\_TO\_CASC}$ | | 1.0 | | 1.1 | | 1.4 | ns |
| $t_{CASC\_TO\_CASC}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{REG\_TO\_CASC}$ | | 1.4 | | 1.7 | | 2.1 | ns |
| $t_{DATA\_TO\_CASC}$ | | 1.1 | | 1.2 | | 1.5 | ns |
| $t_{CH}$ | 2.5 | | 3.0 | | 3.5 | | ns |
| $t_{CL}$ | 2.5 | | 3.0 | | 3.5 | | ns |

*Table 25. IOE Timing Microparameters for EPF6010A & EPF6016A Devices*

| Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{OD1}$ | | 1.9 | | 2.2 | | 2.7 | ns |
| $t_{OD2}$ | | 4.1 | | 4.8 | | 5.8 | ns |
| $t_{OD3}$ | | 5.8 | | 6.8 | | 8.3 | ns |
| $t_{XZ}$ | | 1.4 | | 1.7 | | 2.1 | ns |
| $t_{XZ1}$ | | 1.4 | | 1.7 | | 2.1 | ns |
| $t_{XZ2}$ | | 3.6 | | 4.3 | | 5.2 | ns |
| $t_{XZ3}$ | | 5.3 | | 6.3 | | 7.7 | ns |
| $t_{IOE}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{IN}$ | | 3.6 | | 4.1 | | 5.1 | ns |
| $t_{IN\_DELAY}$ | | 4.8 | | 5.4 | | 6.7 | ns |

*Table 26. Interconnect Timing Microparameters for EPF6010A & EPF6016A Devices*

| Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LOCAL}$ | | 0.7 | | 0.7 | | 1.0 | ns |
| $t_{ROW}$ | | 2.9 | | 3.2 | | 3.2 | ns |
| $t_{COL}$ | | 1.2 | | 1.3 | | 1.4 | ns |
| $t_{DIN\_D}$ | | 5.4 | | 5.7 | | 6.4 | ns |
| $t_{DIN\_C}$ | | 4.3 | | 5.0 | | 6.1 | ns |
| $t_{LEGLOBAL}$ | | 2.6 | | 3.0 | | 3.7 | ns |
| $t_{LABCARRY}$ | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{LABCASC}$ | | 1.3 | | 1.4 | | 1.8 | ns |

*Table 27. External Reference Timing Parameters for EPF6010A & EPF6016A Devices*

| Parameter | Device | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -1 | | -2 | | -3 | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_1$ | EPF6010A | | 37.6 | | 43.6 | | 53.7 | ns |
| | EPF6016A | | 38.0 | | 44.0 | | 54.1 | ns |

*Table 28. External Timing Parameters for EPF6010A & EPF6016A Devices*

| Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.1 *(1)* | | 2.4 *(1)* | | 3.3 *(1)* | | ns |
| $t_{INH}$ | 0.2 *(2)* | | 0.3 *(2)* | | 0.1 *(2)* | | ns |
| $t_{OUTCO}$ | 2.0 | 7.1 | 2.0 | 8.2 | 2.0 | 10.1 | ns |

*Notes:*
(1) Setup times are longer when the *Increase Input Delay* option is turned on. The setup time values are shown with the *Increase Input Delay* option turned off.
(2) Hold time is zero when the *Increase Input Delay* option is turned on.

*Table 30. IOE Timing Microparameters for EPF6016 Devices*

| Parameter | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | -2 | | -3 | | |
| | Min | Max | Min | Max | |
| $t_{OD3}$ | | 4.7 | | 5.2 | ns |
| $t_{XZ}$ | | 2.3 | | 2.8 | ns |
| $t_{ZX1}$ | | 2.3 | | 2.8 | ns |
| $t_{ZX2}$ | | 4.6 | | 5.1 | ns |
| $t_{ZX3}$ | | 4.7 | | 5.2 | ns |
| $t_{IOE}$ | | 0.5 | | 0.6 | ns |
| $t_{IN}$ | | 3.3 | | 4.0 | ns |
| $t_{IN\_DELAY}$ | | 4.6 | | 5.6 | ns |

*Table 31. Interconnect Timing Microparameters for EPF6016 Devices*

| Parameter | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | -2 | | -3 | | |
| | Min | Max | Min | Max | |
| $t_{LOCAL}$ | | 0.8 | | 1.0 | ns |
| $t_{ROW}$ | | 2.9 | | 3.3 | ns |
| $t_{COL}$ | | 2.3 | | 2.5 | ns |
| $t_{DIN\_D}$ | | 4.9 | | 6.0 | ns |
| $t_{DIN\_C}$ | | 4.8 | | 6.0 | ns |
| $t_{LEGLOBAL}$ | | 3.1 | | 3.9 | ns |
| $t_{LABCARRY}$ | | 0.4 | | 0.5 | ns |
| $t_{LABCASC}$ | | 0.8 | | 1.0 | ns |

*Table 32. External Reference Timing Parameters for EPF6016 Devices*

| Parameter | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | -2 | | -3 | | |
| | Min | Max | Min | Max | |
| $t_1$ | | 53.0 | | 65.0 | ns |
| $t_{DRR}$ | | 16.0 | | 20.0 | ns |

*Table 33. External Timing Parameters for EPF6016 Devices*

| Parameter | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | -2 | | -3 | | |
| | Min | Max | Min | Max | |
| $t_{INSU}$ | 3.2 | | 4.1 | | ns |
| $t_{INH}$ | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ | 2.0 | 7.9 | 2.0 | 9.9 | ns |

Tables 34 through 38 show the timing information for EPF6024A devices.

*Table 34. LE Timing Microparameters for EPF6024A Devices*

| Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{REG\_TO\_REG}$ | | 1.2 | | 1.3 | | 1.6 | ns |
| $t_{CASC\_TO\_REG}$ | | 0.7 | | 0.8 | | 1.0 | ns |
| $t_{CARRY\_TO\_REG}$ | | 1.6 | | 1.8 | | 2.2 | ns |
| $t_{DATA\_TO\_REG}$ | | 1.3 | | 1.4 | | 1.7 | ns |
| $t_{CASC\_TO\_OUT}$ | | 1.2 | | 1.3 | | 1.6 | ns |
| $t_{CARRY\_TO\_OUT}$ | | 2.0 | | 2.2 | | 2.6 | ns |
| $t_{DATA\_TO\_OUT}$ | | 1.8 | | 2.1 | | 2.6 | ns |
| $t_{REG\_TO\_OUT}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{SU}$ | 0.9 | | 1.0 | | 1.2 | | ns |
| $t_{H}$ | 1.3 | | 1.4 | | 1.7 | | ns |
| $t_{CO}$ | | 0.2 | | 0.3 | | 0.3 | ns |
| $t_{CLR}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{C}$ | | 1.9 | | 2.1 | | 2.5 | ns |
| $t_{LD\_CLR}$ | | 1.9 | | 2.1 | | 2.5 | ns |
| $t_{CARRY\_TO\_CARRY}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{REG\_TO\_CARRY}$ | | 1.4 | | 1.6 | | 1.9 | ns |
| $t_{DATA\_TO\_CARRY}$ | | 1.3 | | 1.4 | | 1.7 | ns |
| $t_{CARRY\_TO\_CASC}$ | | 1.1 | | 1.2 | | 1.4 | ns |
| $t_{CASC\_TO\_CASC}$ | | 0.7 | | 0.8 | | 1.0 | ns |
| $t_{REG\_TO\_CASC}$ | | 1.4 | | 1.6 | | 1.9 | ns |
| $t_{DATA\_TO\_CASC}$ | | 1.0 | | 1.1 | | 1.3 | ns |
| $t_{CH}$ | 2.5 | | 3.0 | | 3.5 | | ns |
| $t_{CL}$ | 2.5 | | 3.0 | | 3.5 | | ns |