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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

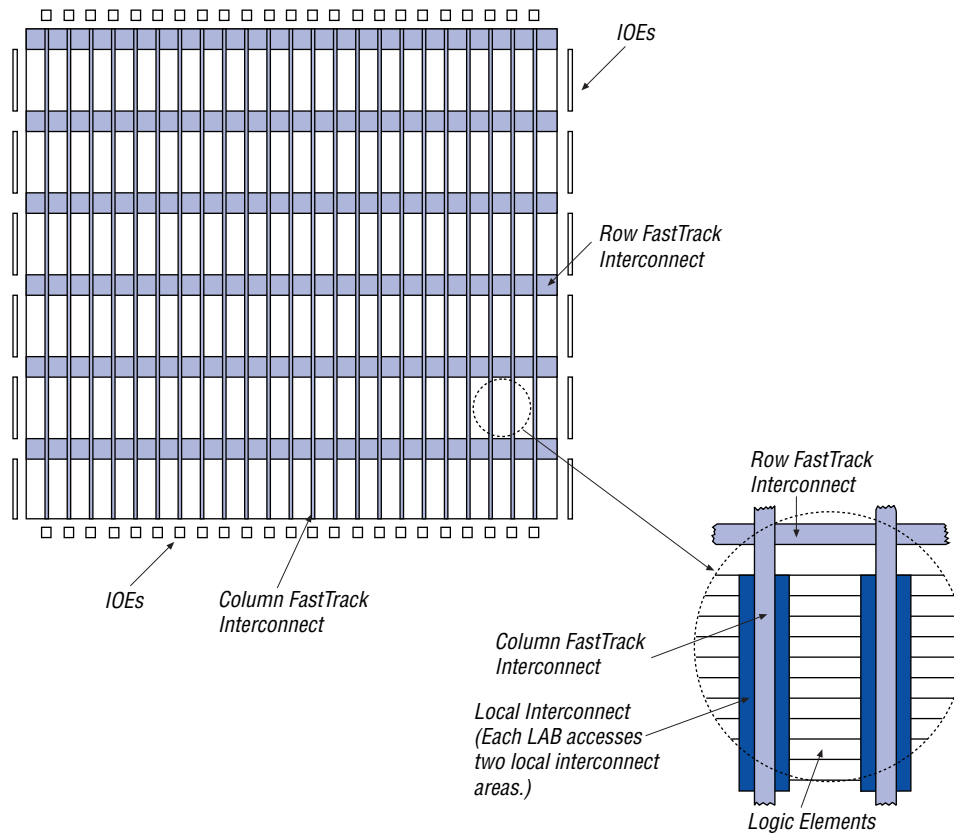
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

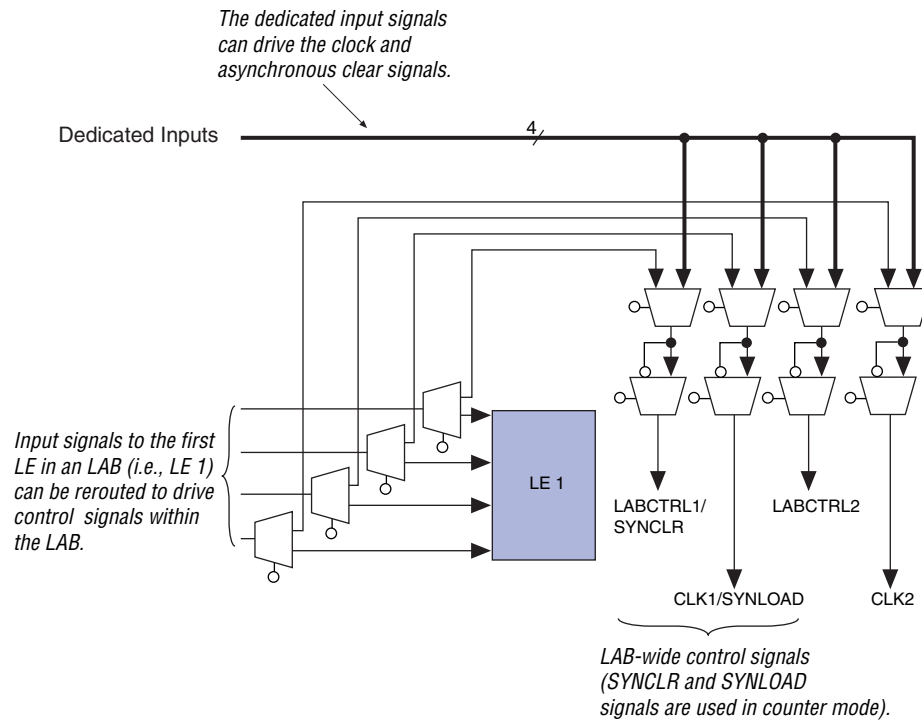
Product Status	Obsolete
Number of LABs/CLBs	132
Number of Logic Elements/Cells	1320
Total RAM Bits	-
Number of I/O	117
Number of Gates	16000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf6016atc144-1">https://www.e-xfl.com/product-detail/intel/epf6016atc144-1</a>

**Figure 1. OptiFLEX Architecture Block Diagram**

FLEX 6000 devices provide four dedicated, global inputs that drive the control inputs of the flipflops to ensure efficient distribution of high-speed, low-skew control signals. These inputs use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. These inputs can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device. The dedicated global routing structure is built into the device, eliminating the need to create a clock tree.

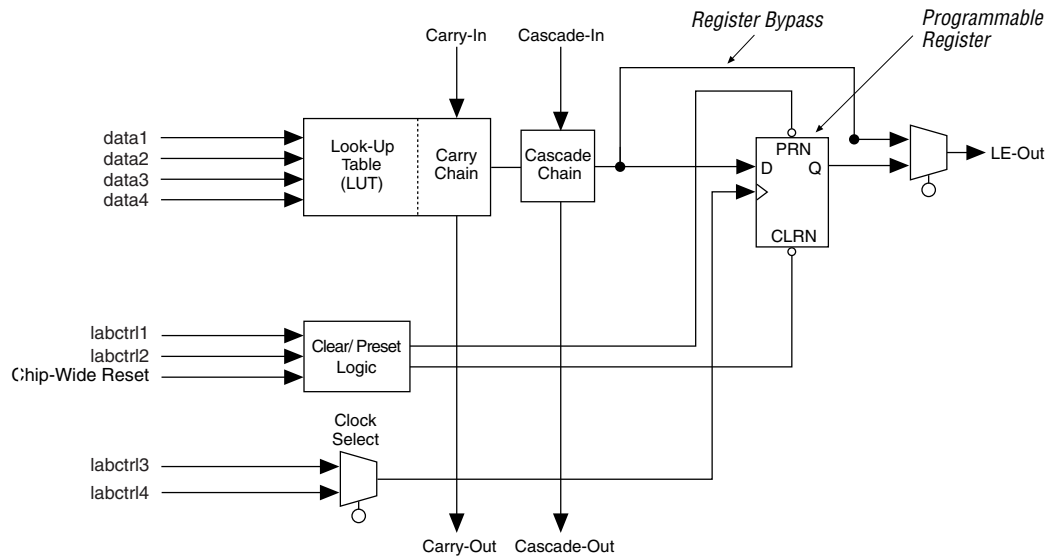
### Logic Array Block

An LAB consists of ten LEs, their associated carry and cascade chains, the LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 6000 architecture, and facilitates efficient routing with optimum device utilization and high performance.

**Figure 3. LAB Control Signals**

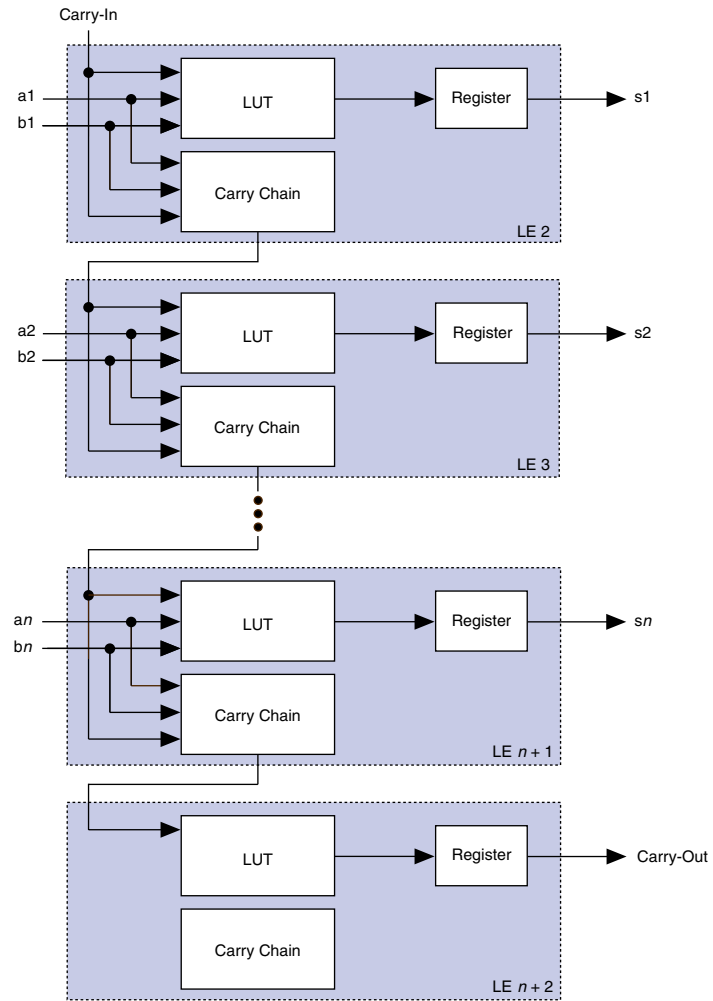
## Logic Element

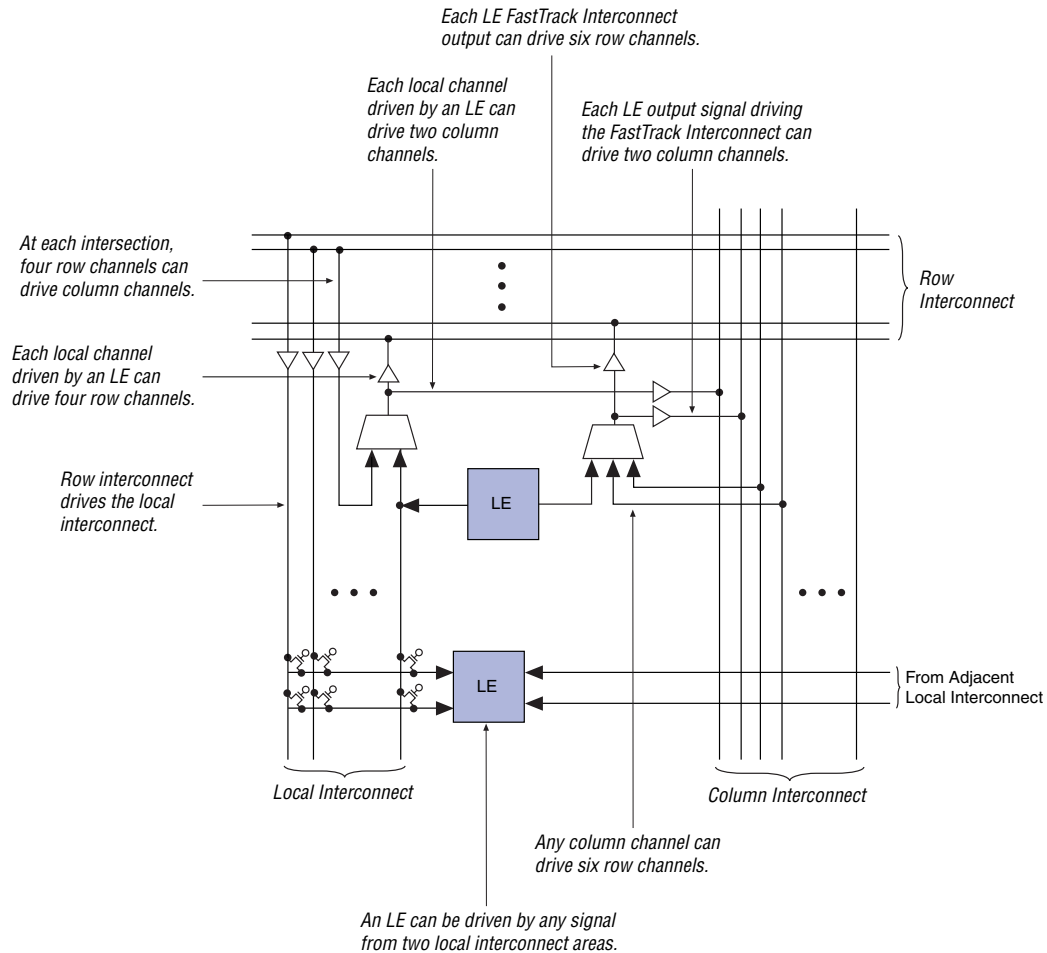
An LE, the smallest unit of logic in the FLEX 6000 architecture, has a compact size that provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. An LE contains a programmable flipflop, carry and cascade chains. Additionally, each LE drives both the local and the FastTrack Interconnect. See [Figure 4](#).

**Figure 4. Logic Element**

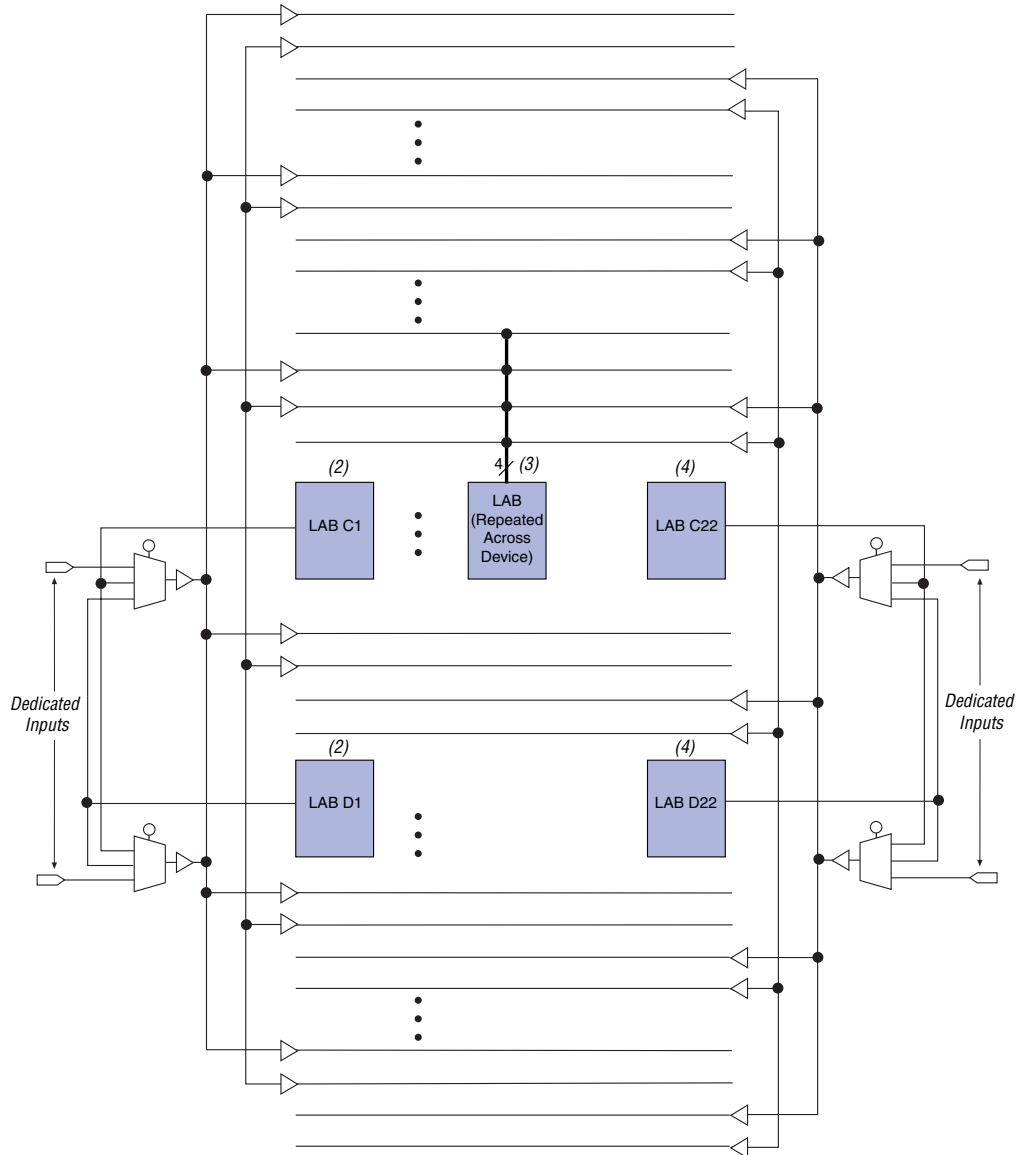
The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock and clear control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the flipflop is bypassed and the output of the LUT drives the outputs of the LE. The LE output can drive both the local interconnect and the FastTrack Interconnect.

The FLEX 6000 architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equivalent comparators with minimum delay. Carry and cascade chains connect LEs 2 through 10 in an LAB and all LABs in the same half of the row. Because extensive use of carry and cascade chains can reduce routing flexibility, these chains should be limited to speed-critical portions of a design.

**Figure 5. Carry Chain Operation**

**Figure 10. LAB Connections to Row & Column Interconnects**

For improved routability, the row interconnect consists of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-length channel, which saves the other half of the channel for the other half of the row. One-third of the row channels are half-length channels.

**Figure 11. Global Clock & Clear Distribution** *Note (1)***Notes:**

- (1) The global clock and clear distribution signals are shown for EPF6016 and EPF6016A devices. In EPF6010A devices, LABs in rows B and C drive global signals. In EPF6024A devices, LABs in rows C and E drive global signals.
- (2) The local interconnect from LABs C1 and D1 can drive two global control signals on the left side.
- (3) Global signals drive into every LAB as clock, asynchronous clear, preset, and data signals.
- (4) The local interconnect from LABs C22 and D22 can drive two global control signals on the right side.

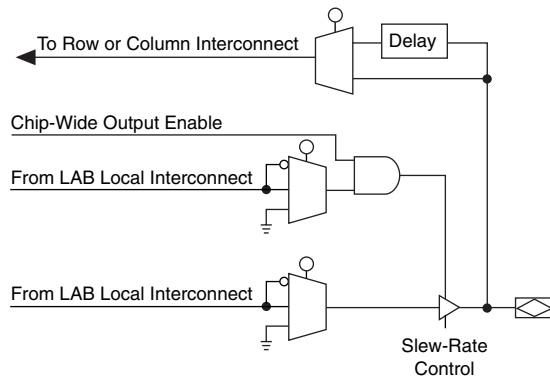
## I/O Elements

An IOE contains a bidirectional I/O buffer and a tri-state buffer. IOEs can be used as input, output, or bidirectional pins. An IOE receives its data signals from the adjacent local interconnect, which can be driven by a row or column interconnect (allowing any LE in the device to drive the IOE) or by an adjacent LE (allowing fast clock-to-output delays). A FastFLEX™ I/O pin is a row or column output pin that receives its data signals from the adjacent local interconnect driven by an adjacent LE. The IOE receives its output enable signal through the same path, allowing individual output enables for every pin and permitting emulation of open-drain buffers. The Altera Compiler uses programmable inversion to invert the data or output enable signals automatically where appropriate. Open-drain emulation is provided by driving the data input low and toggling the OE of each IOE. This emulation is possible because there is one OE per pin.

A chip-wide output enable feature allows the designer to disable all pins of the device by asserting one pin (DEV\_OE). This feature is useful during board debugging or testing.

Figure 12 shows the IOE block diagram.

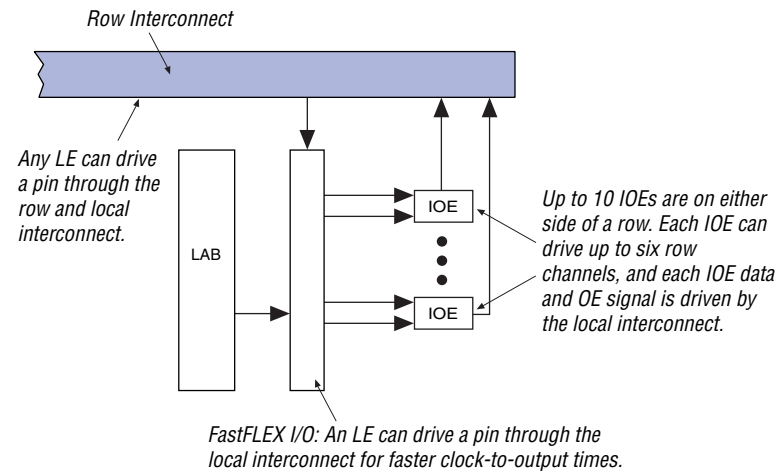
**Figure 12. IOE Block Diagram**





Each IOE drives a row or column interconnect when used as an input or bidirectional pin. A row IOE can drive up to six row lines; a column IOE can drive up to two column lines. The input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time. Figure 13 shows how an IOE connects to a row interconnect, and Figure 14 shows how an IOE connects to a column interconnect.

**Figure 13. IOE Connection to Row Interconnect**



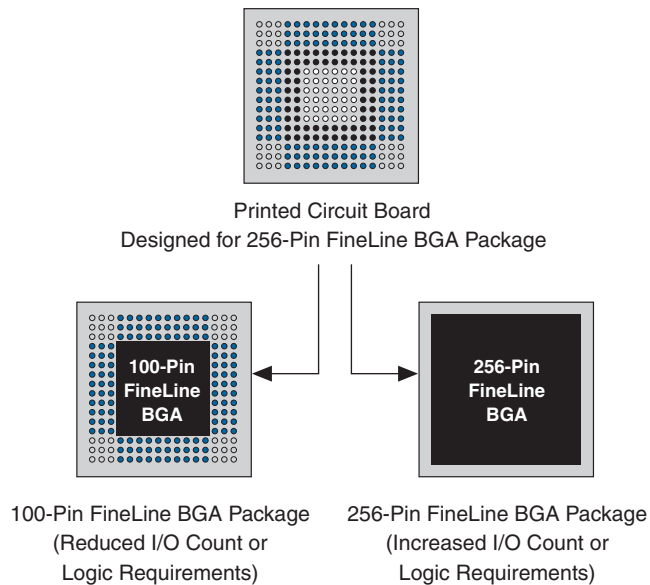
**Figure 15. SameFrame Pin-Out Example**

Table 6 lists the 3.3-V FLEX 6000 devices with the SameFrame pin-out feature.

**Table 6. 3.3-V FLEX 6000 Devices with SameFrame Pin-Outs**

Device	100-Pin FineLine BGA	256-Pin FineLine BGA
EPF6016A	V	V
EPF6024A		V

## Output Configuration

This section discusses slew-rate control, the MultiVolt I/O interface, power sequencing, and hot-socketing for FLEX 6000 devices.

### Slew-Rate Control

The output buffer in each IOE has an adjustable output slew-rate that can be configured for low-noise or high-speed performance. A slower slew-rate reduces system noise and adds a maximum delay of 6.8 ns. The fast slew-rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew-rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a device-wide basis. The slew-rate setting affects only the falling edge of the output.

## MultiVolt I/O Interface

The FLEX 6000 device architecture supports the MultiVolt I/O interface feature, which allows FLEX 6000 devices to interface with systems of differing supply voltages. The EPF6016 device can be set for 3.3-V or 5.0-V I/O pin operation. This device has one set of  $V_{CC}$  pins for internal operation and input buffers ( $V_{CCINT}$ ), and another set for output drivers ( $V_{CCIO}$ ).

The  $V_{CCINT}$  pins on 5.0-V FLEX 6000 devices must always be connected to a 5.0-V power supply. With a 5.0-V  $V_{CCINT}$  level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The  $V_{CCIO}$  pins on 5.0-V FLEX 6000 devices can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the  $V_{CCIO}$  pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the  $V_{CCIO}$  pins are connected to a 3.3-V power supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with  $V_{CCIO}$  levels lower than 4.75 V incur a nominally greater timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ .

On 3.3-V FLEX 6000 devices, the  $V_{CCINT}$  pins must be connected to a 3.3-V power supply. Additionally, 3.3-V FLEX 6000A devices can interface with 2.5-V, 3.3-V, or 5.0-V systems when the  $V_{CCIO}$  pins are tied to 2.5 V. The output can drive 2.5-V systems, and the inputs can be driven by 2.5-V, 3.3-V, or 5.0-V systems. When the  $V_{CCIO}$  pins are tied to 3.3 V, the output can drive 3.3-V or 5.0-V systems. MultiVolt I/Os are not supported on 100-pin TQFP or 100-pin FineLine BGA packages.

Table 7 describes FLEX 6000 MultiVolt I/O support.

<b>Table 7. FLEX 6000 MultiVolt I/O Support</b>							
<b><math>V_{CCINT}</math> (V)</b>	<b><math>V_{CCIO}</math> (V)</b>	<b>Input Signal (V)</b>			<b>Output Signal (V)</b>		
		<b>2.5</b>	<b>3.3</b>	<b>5.0</b>	<b>2.5</b>	<b>3.3</b>	<b>5.0</b>
3.3	2.5	v	v	v	v		
3.3	3.3	v	v	v	v (1)	v	v
5.0	3.3		v	v		v	v
5.0	5.0		v	v			v

**Note:**

- (1) When  $V_{CCIO} = 3.3$  V, a FLEX 6000 device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V or 3.3-V FLEX 6000 devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a  $V_{IH}$  of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The  $I_{OL}$  current specification should be considered when selecting a pull-up resistor.

Output pins on 5.0-V FLEX 6000 devices with  $V_{CCIO} = 3.3$  V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

### Power Sequencing & Hot-Socketing

Because FLEX 6000 family devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The  $V_{CCIO}$  and  $V_{CCINT}$  power planes can be powered in any order.

Signals can be driven into 3.3-V FLEX 6000 devices before and during power up without damaging the device. Additionally, FLEX 6000 devices do not drive out during power up. Once operating conditions are reached, FLEX 6000 devices operate as specified by the user.

### IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 6000 devices provide JTAG BST circuitry that comply with the IEEE Std. 1149.1-1990 specification. [Table 8](#) shows JTAG instructions for FLEX 6000 devices. JTAG BST can be performed before or after configuration, but not during configuration (except when you disable JTAG support in user mode).

- 1 See [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#) for more information on JTAG BST circuitry.

**Table 8. FLEX 6000 JTAG Instructions**

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test result at the input pins.
BYPASS	Places the 1-bit bypass register between the $TDI$ and $TDO$ pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.

**Table 10. JTAG Timing Parameters & Values**

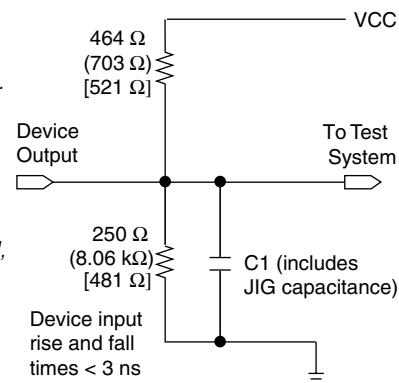
Symbol	Parameter	Min	Max	Unit
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock-to-output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock-to-output		35	ns
$t_{JSZX}$	Update register high impedance to valid output		35	ns
$t_{JSXZ}$	Update register valid output to high impedance		35	ns

## Generic Testing

Each FLEX 6000 device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 6000 devices are made under conditions equivalent to those shown in [Figure 17](#). Multiple test patterns can be used to configure devices during all stages of the production flow.

**Figure 17. AC Test Conditions**

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers without parentheses are for 5.0-V devices or outputs. Numbers in parentheses are for 3.3-V devices or outputs. Numbers in brackets are for 2.5-V devices or outputs.



## Operating Conditions

Tables 11 through 18 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V and 3.3-V FLEX 6000 devices.

**Table 11. FLEX 6000 5.0-V Device Absolute Maximum Ratings** *Note (1)*

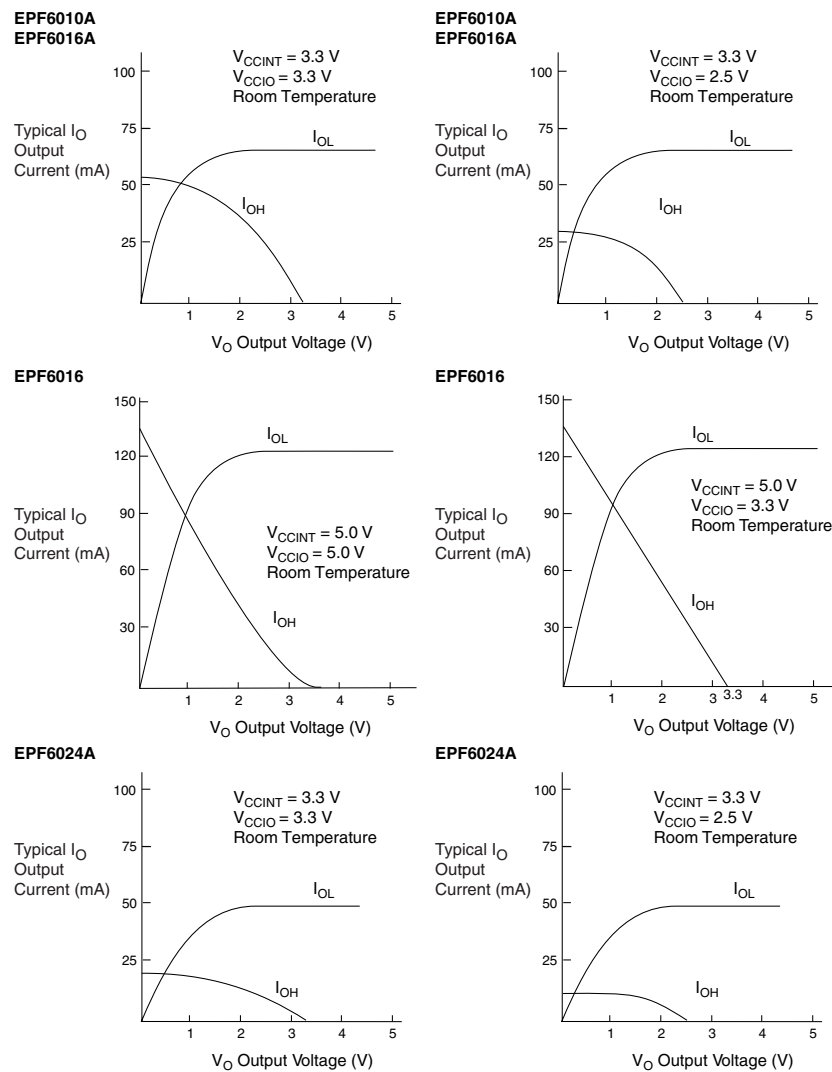
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply voltage	With respect to ground (2)	–2.0	7.0	V
$V_I$	DC input voltage		–2.0	7.0	V
$I_{OUT}$	DC output current, per pin		–25	25	mA
$T_{STG}$	Storage temperature	No bias	–65	150	°C
$T_{AMB}$	Ambient temperature	Under bias	–65	135	°C
$T_J$	Junction temperature	PQFP, TQFP, and BGA packages		135	°C

**Table 12. FLEX 6000 5.0-V Device Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
$V_{CCIO}$	Supply voltage for output buffers, 5.0-V operation	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
$V_I$	Input voltage		–0.5	$V_{CCINT} + 0.5$	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_J$	Operating temperature	For commercial use	0	85	°C
		For industrial use	–40	100	°C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns

Figure 18 shows the typical output drive characteristics of 5.0-V and 3.3-V FLEX 6000 devices with 5.0-V, 3.3-V, and 2.5-V  $V_{CCIO}$ . When  $V_{CCIO} = 5.0$  V on EPF6016 devices, the output driver is compliant with the *PCI Local Bus Specification, Revision 2.2* for 5.0-V operation. When  $V_{CCIO} = 3.3$  V on the EPF6010A and EPF6016A devices, the output driver is compliant with the *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation.

Figure 18. Output Drive Characteristics



## Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row can be calculated by adding the following parameters:

- LE register clock-to-output delay ( $t_{CO} + t_{REG\_TO\_OUT}$ )
- Routing delay ( $t_{ROW} + t_{LOCAL}$ )
- LE LUT delay ( $t_{DATA\_TO\_REG}$ )
- LE register setup time ( $t_{SU}$ )

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

Timing simulation and delay prediction are available with the Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 19 shows the overall timing model, which maps the possible routing paths to and from the various elements of the FLEX 6000 device.



**Table 20. IOE Timing Microparameters** *Note (1)*

Symbol	Parameter	Conditions
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF (2)
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off, $V_{CCIO}$ = low voltage	C1 = 35 pF (3)
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF (4)
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF (2)
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off, $V_{CCIO}$ = low voltage	C1 = 35 pF (3)
$t_{ZX3}$	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF (4)
$t_{IOE}$	Output enable control delay	
$t_{IN}$	Input pad and buffer to FastTrack Interconnect delay	
$t_{IN\_DELAY}$	Input pad and buffer to FastTrack Interconnect delay with additional delay turned on	

**Table 21. Interconnect Timing Microparameters** *Note (1)*

Symbol	Parameter	Conditions
$t_{LOCAL}$	LAB local interconnect delay	
$t_{ROW}$	Row interconnect routing delay	(5)
$t_{COL}$	Column interconnect routing delay	(5)
$t_{DIN\_D}$	Dedicated input to LE data delay	(5)
$t_{DIN\_C}$	Dedicated input to LE control delay	
$t_{LEGLOBAL}$	LE output to LE control via internally-generated global signal delay	(5)
$t_{LABCARRY}$	Routing delay for the carry-out of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

**Table 22. External Reference Timing Parameters**

Symbol	Parameter	Conditions
$t_1$	Register-to-register test pattern	(6)
$t_{DRR}$	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects	(7)

<b>Table 23. External Timing Parameters</b>		
<b>Symbol</b>	<b>Parameter</b>	<b>Conditions</b>
$t_{\text{INSU}}$	Setup time with global clock at LE register	(8)
$t_{\text{INH}}$	Hold time with global clock at LE register	(8)
$t_{\text{OUTCO}}$	Clock-to-output delay with global clock with LE register using FastFLEX I/O pin	(8)

**Notes to tables:**

- (1) Microparameters are timing delays contributed by individual architectural elements and cannot be measured explicitly.
- (2) Operating conditions:  
 $V_{\text{CCIO}} = 5.0 \text{ V} \pm 5\%$  for commercial use in 5.0-V FLEX 6000 devices.  
 $V_{\text{CCIO}} = 5.0 \text{ V} \pm 10\%$  for industrial use in 5.0-V FLEX 6000 devices.  
 $V_{\text{CCIO}} = 3.3 \text{ V} \pm 10\%$  for commercial or industrial use in 3.3-V FLEX 6000 devices.
- (3) Operating conditions:  
 $V_{\text{CCIO}} = 3.3 \text{ V} \pm 10\%$  for commercial or industrial use in 5.0-V FLEX 6000 devices.  
 $V_{\text{CCIO}} = 2.5 \text{ V} \pm 0.2 \text{ V}$  for commercial or industrial use in 3.3-V FLEX 6000 devices.
- (4) Operating conditions:  
 $V_{\text{CCIO}} = 2.5 \text{ V}, 3.3 \text{ V}, \text{ or } 5.0 \text{ V}.$
- (5) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
- (6) This timing parameter shows the delay of a register-to-register test pattern and is used to determine speed grades. There are 12 LEs, including source and destination registers. The row and column interconnects between the registers vary in length.
- (7) This timing parameter is shown for reference and is specified by characterization.
- (8) This timing parameter is specified by characterization.

Tables 24 through 28 show the timing information for EPF6010A and EPF6016A devices.

Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 1 of 2)							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{REG\_TO\_REG}$		1.2		1.3		1.7	ns
$t_{CASC\_TO\_REG}$		0.9		1.0		1.2	ns
$t_{CARRY\_TO\_REG}$		0.9		1.0		1.2	ns
$t_{DATA\_TO\_REG}$		1.1		1.2		1.5	ns
$t_{CASC\_TO\_OUT}$		1.3		1.4		1.8	ns
$t_{CARRY\_TO\_OUT}$		1.6		1.8		2.3	ns
$t_{DATA\_TO\_OUT}$		1.7		2.0		2.5	ns
$t_{REG\_TO\_OUT}$		0.4		0.4		0.5	ns
$t_{SU}$	0.9		1.0		1.3		ns
$t_H$	1.4		1.7		2.1		ns

**Table 30. IOE Timing Microparameters for EPF6016 Devices**

Table 30. IOE Timing Microparameters for EPF6016 Devices					
Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
$t_{OD3}$		4.7		5.2	ns
$t_{XZ}$		2.3		2.8	ns
$t_{ZX1}$		2.3		2.8	ns
$t_{ZX2}$		4.6		5.1	ns
$t_{ZX3}$		4.7		5.2	ns
$t_{IOE}$		0.5		0.6	ns
$t_{IN}$		3.3		4.0	ns
$t_{IN\_DELAY}$		4.6		5.6	ns

**Table 31. Interconnect Timing Microparameters for EPF6016 Devices**

Table 31. Interconnect Timing Microparameters for EPF6016 Devices					
Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
$t_{LOCAL}$		0.8		1.0	ns
$t_{ROW}$		2.9		3.3	ns
$t_{COL}$		2.3		2.5	ns
$t_{DIN\_D}$		4.9		6.0	ns
$t_{DIN\_C}$		4.8		6.0	ns
$t_{LEGLOBAL}$		3.1		3.9	ns
$t_{LABCARRY}$		0.4		0.5	ns
$t_{LABCASC}$		0.8		1.0	ns

**Table 32. External Reference Timing Parameters for EPF6016 Devices**

Table 32. External Reference Timing Parameters for EPF6016 Devices					
Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
t <sub>1</sub>		53.0		65.0	ns
t <sub>DDR</sub>		16.0		20.0	ns

This calculation provides an  $I_{CC}$  estimate based on typical conditions with no output load. The actual  $I_{CC}$  should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

To better reflect actual designs, the power model (and the constant K in the power calculation equations shown above) for continuous interconnect FLEX devices assumes that LEs drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all LEs drive only one short interconnect segment. This assumption may lead to inaccurate results, compared to measured power consumption for an actual design in a segmented interconnect FPGA.

Figure 20 shows the relationship between the current and operating frequency for EPF6010A, EPF6016, EPF6016A, and EPF6024A devices.



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