Intel - EPF6016ATC144-2 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	132
Number of Logic Elements/Cells	1320
Total RAM Bits	-
Number of I/O	117
Number of Gates	16000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf6016atc144-2

Carry Chain

The carry chain provides a very fast (0.1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 6000 architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Altera software during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

Because the first LE of each LAB can generate control signals for that LAB, the first LE in each LAB is not included in carry chains. In addition, the inputs of the first LE in each LAB may be used to generate synchronous clear and load enable signals for counters implemented with carry chains.

Carry chains longer than nine LEs are implemented automatically by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from an even-numbered LAB to another even-numbered LAB, or from an odd-numbered LAB to another odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the second LE of the third LAB in the row. In addition, the carry chain does not cross the middle of the row. For instance, in the EPF6016 device, the carry chain stops at the 11th LAB in a row and a new carry chain begins at the 12th LAB.

Figure 5 shows how an n-bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. Although the register can be bypassed for simple adders, it can be used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the FastTrack Interconnect.

Figure 5. Carry Chain Operation

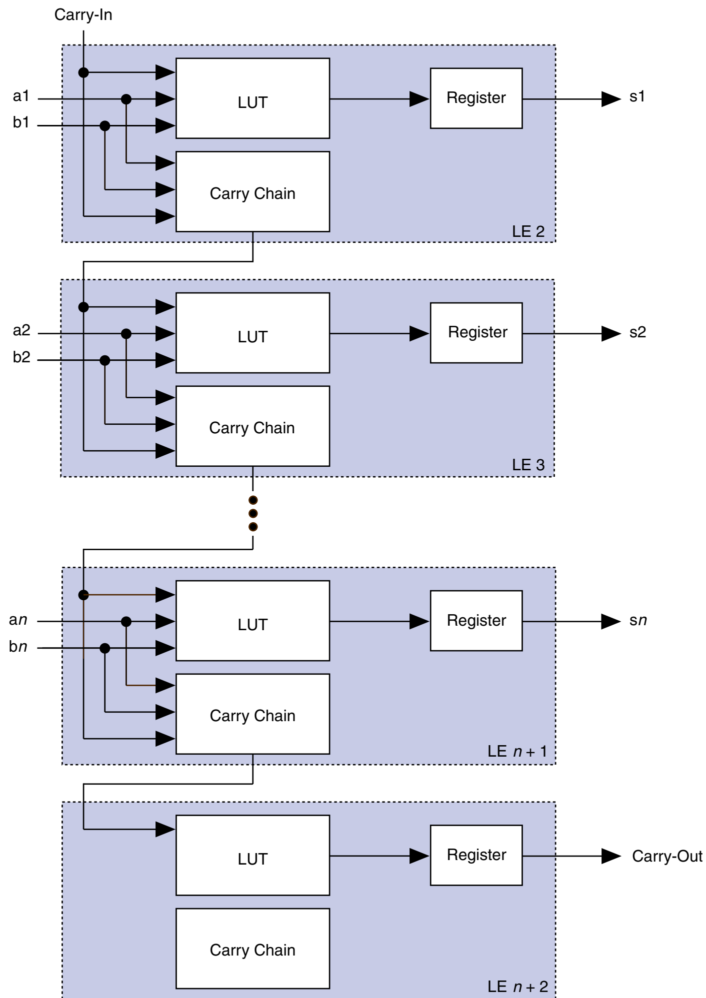
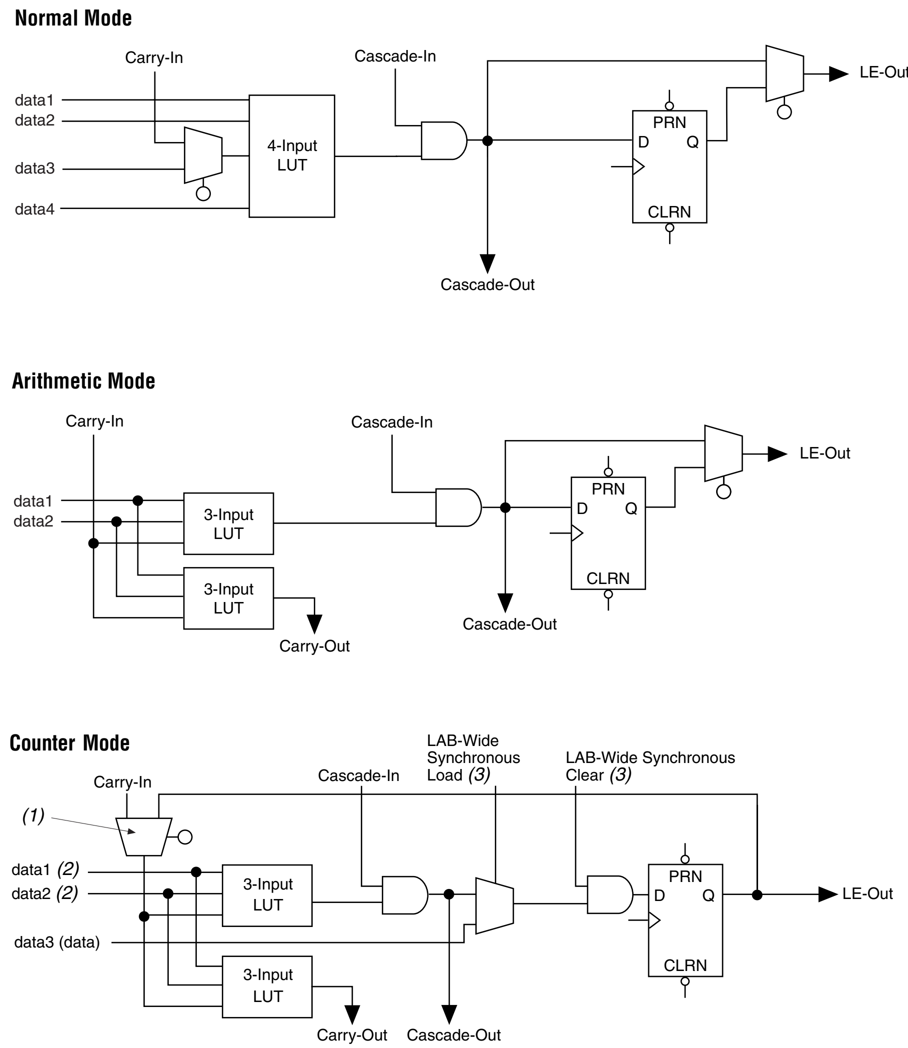


Figure 7. LE Operating Modes



Notes:

(1) The register feedback multiplexer is available on LE 2 of each LAB.

(2) The `data1` and `data2` input signals can supply a clock enable, up or down control, or register feedback signals for all LEs other than the second LE in an LAB.

(3) The LAB-wide synchronous clear and LAB-wide synchronous load affect all registers in an LAB.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The Altera software automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a 3-input function; the other generates a carry output. As shown in Figure 7, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

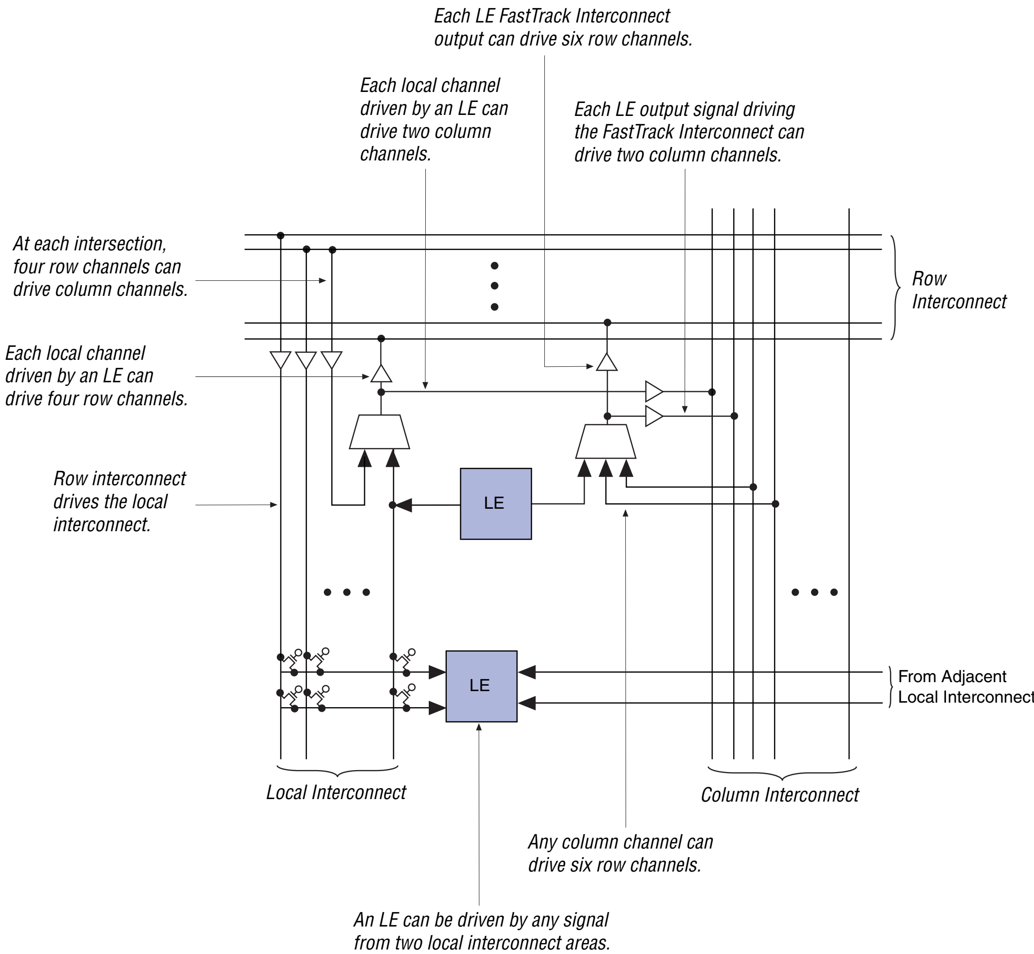
The Altera software implements logic functions to use the arithmetic mode automatically where appropriate; the designer does not have to decide how the carry chain will be used.

Counter Mode

The counter mode offers counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in a LAB use counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. In addition, the Altera software automatically places registers that are not in the counter into other LABs.

The counter mode uses two 3-input LUTs: one generates the counter data and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load will override any signal carried on the cascade chain. The synchronous clear overrides the synchronous load.

Figure 10. LAB Connections to Row & Column Interconnects



For improved routability, the row interconnect consists of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-length channel, which saves the other half of the channel for the other half of the row. One-third of the row channels are half-length channels.

Table 5 summarizes the FastTrack Interconnect resources available in each FLEX 6000 device.

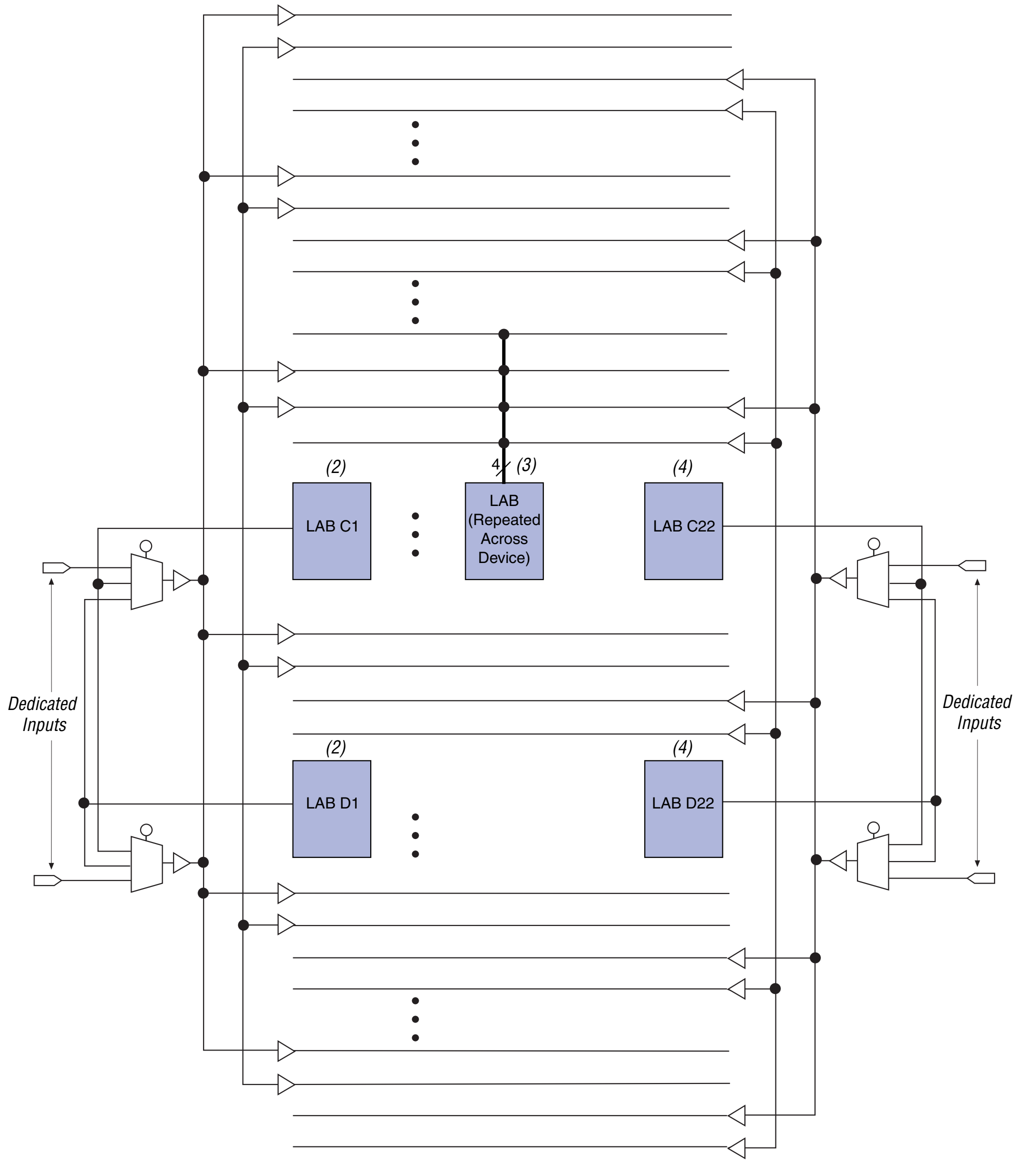
Table 5. FLEX 6000 FastTrack Interconnect Resources

Device	Rows	Channels per Row	Columns	Channels per Column
EPF6010A	4	144	22	20
EPF6016 EPF6016A	6	144	22	20
EPF6024A	7	186	28	30

In addition to general-purpose I/O pins, FLEX 6000 devices have four dedicated input pins that provide low-skew signal distribution across the device. These four inputs can be used for global clock and asynchronous clear control signals. These signals are available as control signals for all LEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device. Using dedicated inputs to route data signals provides a fast path for high fan-out signals.

The local interconnect from LABs located at either end of two rows can drive a global control signal. For instance, in an EPF6016 device, LABs C1, D1, C22, and D22 can all drive global control signals. When an LE drives a global control signal, the dedicated input pin that drives that signal cannot be used. Any LE in the device can drive a global control signal by driving the FastTrack Interconnect into the appropriate LAB. To minimize delay, however, the Altera software places the driving LE in the appropriate LAB. The LE-driving-global signal feature is optimized for speed for control signals; regular data signals are better routed on the FastTrack Interconnect and do not receive any advantage from being routed on global signals. This LE-driving-global control signal feature is controlled by the designer and is not used automatically by the Altera software. See Figure 11.

Figure 11. Global Clock & Clear Distribution *Note (1)*



Notes:

(1) The global clock and clear distribution signals are shown for EPF6016 and EPF6016A devices. In EPF6010A devices, LABs in rows B and C drive global signals. In EPF6024A devices, LABs in rows C and E drive global signals.

(2) The local interconnect from LABs C1 and D1 can drive two global control signals on the left side.

(3) Global signals drive into every LAB as clock, asynchronous clear, preset, and data signals.

(4) The local interconnect from LABs C22 and D22 can drive two global control signals on the right side.

Each IOE drives a row or column interconnect when used as an input or bidirectional pin. A row IOE can drive up to six row lines; a column IOE can drive up to two column lines. The input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time. Figure 13 shows how an IOE connects to a row interconnect, and Figure 14 shows how an IOE connects to a column interconnect.

Figure 13. IOE Connection to Row Interconnect

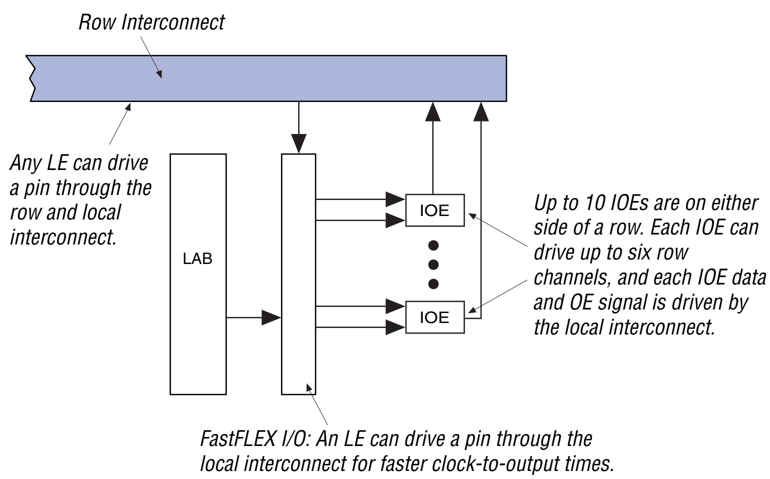
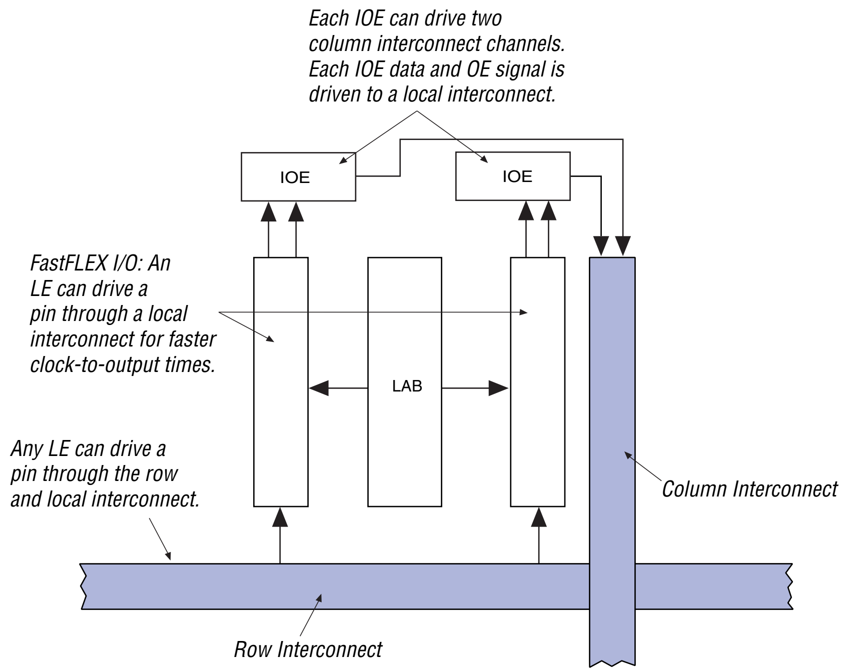


Figure 14. IOE Connection to Column Interconnect



SameFrame Pin-Outs

3.3-V FLEX 6000 devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support an EPF6016A device in a 100-pin FineLine BGA package or an EPF6024A device in a 256-pin FineLine BGA package.

The Altera software packages provide support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software packages generate pin-outs describing how to lay out a board to take advantage of this migration (see Figure 15).

Figure 15. SameFrame Pin-Out Example

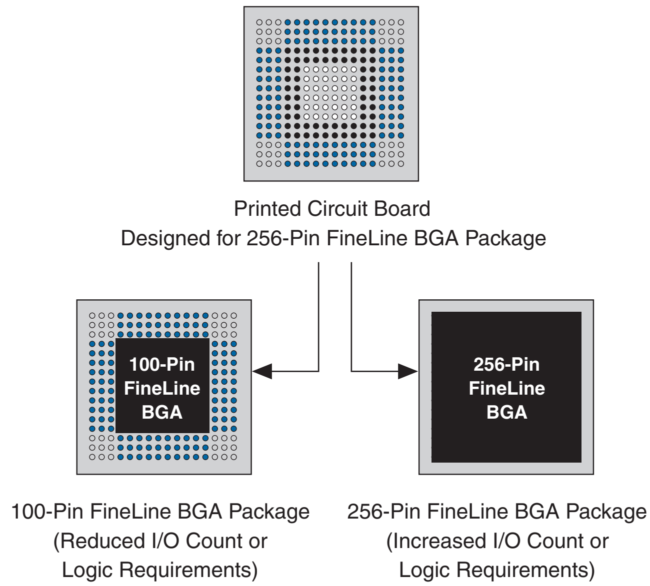


Table 6 lists the 3.3-V FLEX 6000 devices with the SameFrame pin-out feature.

Table 6. 3.3-V FLEX 6000 Devices with SameFrame Pin-Outs

Device	100-Pin FineLine BGA	256-Pin FineLine BGA
EPF6016A	v	v
EPF6024A		v

Output Configuration

This section discusses slew-rate control, the MultiVolt I/O interface, power sequencing, and hot-socketing for FLEX 6000 devices.

Slew-Rate Control

The output buffer in each IOE has an adjustable output slew-rate that can be configured for low-noise or high-speed performance. A slower slew-rate reduces system noise and adds a maximum delay of 6.8 ns. The fast slew-rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew-rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a device-wide basis. The slew-rate setting affects only the falling edge of the output.

MultiVolt I/O Interface

The FLEX 6000 device architecture supports the MultiVolt I/O interface feature, which allows FLEX 6000 devices to interface with systems of differing supply voltages. The EPF6016 device can be set for 3.3-V or 5.0-V I/O pin operation. This device has one set of V_{CC} pins for internal operation and input buffers (`VCCINT`), and another set for output drivers (`VCCIO`).

The `VCCINT` pins on 5.0-V FLEX 6000 devices must always be connected to a 5.0-V power supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The `VCCIO` pins on 5.0-V FLEX 6000 devices can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the `VCCIO` pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the `VCCIO` pins are connected to a 3.3-V power supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}.

On 3.3-V FLEX 6000 devices, the `VCCINT` pins must be connected to a 3.3-V power supply. Additionally, 3.3-V FLEX 6000A devices can interface with 2.5-V, 3.3-V, or 5.0-V systems when the `VCCIO` pins are tied to 2.5 V. The output can drive 2.5-V systems, and the inputs can be driven by 2.5-V, 3.3-V, or 5.0-V systems. When the `VCCIO` pins are tied to 3.3 V, the output can drive 3.3-V or 5.0-V systems. MultiVolt I/Os are not supported on 100-pin TQFP or 100-pin FineLine BGA packages.

Table 7 describes FLEX 6000 MultiVolt I/O support.

Table 7. FLEX 6000 MultiVolt I/O Support

V_{CCINT} (V)	V_{CCIO} (V)	Input Signal (V)			Output Signal (V)		
		2.5	3.3	5.0	2.5	3.3	5.0
3.3	2.5	v	v	v	v		
3.3	3.3	v	v	v	v *(1)*	v	v
5.0	3.3		v	v		v	v
5.0	5.0		v	v			v

Note:

(1) When V_{CCIO} = 3.3 V, a FLEX 6000 device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Table 15. FLEX 6000 3.3-V Device Absolute Maximum Ratings *Note (1)*					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage	With respect to ground *(2)*	–0.5	4.6	V
V_I	DC input voltage		–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, PLCC, and BGA packages		135	° C

Table 16. FLEX 6000 3.3-V Device Recommended Operating Conditions					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.30 (2.30)	2.70 (2.70)	V
V_I	Input voltage		–0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 17. FLEX 6000 3.3-V Device DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7		5.75	V
V_{IL}	Low-level input voltage		–0.5		0.8	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –8 mA DC, V_{CCIO} = 3.00 V *(7)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(7)*	V_{CCIO} – 0.2			V
	2.5-V high-level output voltage	I_{OH} = –100 µA DC, V_{CCIO} = 2.30 V *(7)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(7)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(7)*	1.7			V
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 8 mA DC, V_{CCIO} = 3.00 V *(8)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(8)*			0.2	V
	2.5-V low-level output voltage	I_{OL} = 100 µA DC, V_{CCIO} = 2.30 V *(8)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(8)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(8)*			0.7	V
I_I	Input pin leakage current	V_I = 5.3 V to ground *(8)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 5.3 V to ground *(8)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.5	5	mA

Table 18. FLEX 6000 3.3-V Device Capacitance *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance for I/O pin	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance for dedicated input	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) The minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
(5) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.
(6) These values are specified under Table 16 on page 33.
(7) The I_{OH} parameter refers to high-level TTL or CMOS output current.
(8) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(9) Capacitance is sample-tested only.

Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row can be calculated by adding the following parameters:

- LE register clock-to-output delay ($t_{CO} + t_{REG\_TO\_OUT}$)
- Routing delay ($t_{ROW} + t_{LOCAL}$)
- LE LUT delay ($t_{DATA\_TO\_REG}$)
- LE register setup time (t_{SU})

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

Timing simulation and delay prediction are available with the Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 19 shows the overall timing model, which maps the possible routing paths to and from the various elements of the FLEX 6000 device.

Figure 19. FLEX 6000 Timing Model

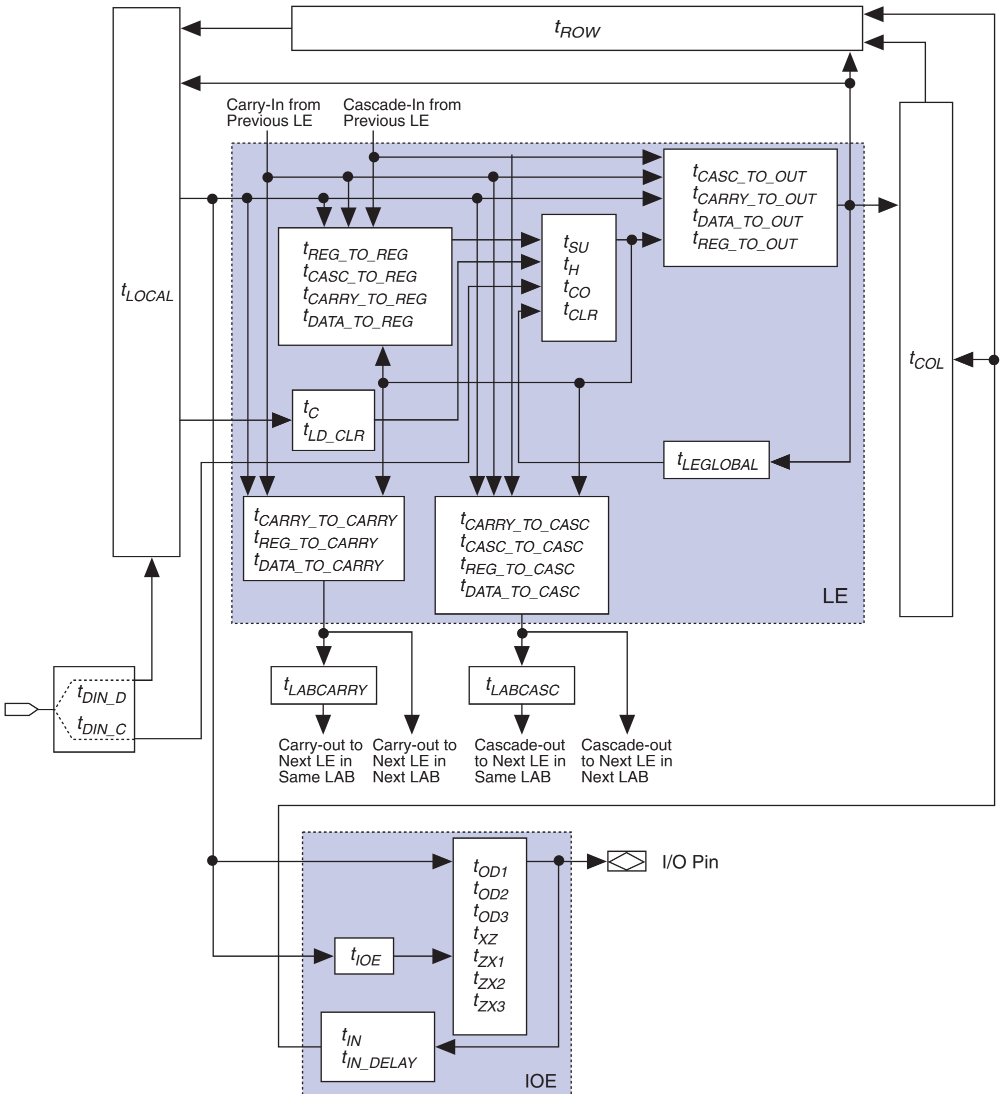


Table 20. IOE Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
t_{OD1}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = V_{CCINT}	C1 = 35 pF *(2)*
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF *(3)*
t_{OD3}	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF *(4)*
t_{XZ}	Output buffer disable delay	C1 = 5 pF
t_{ZX1}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = V_{CCINT}	C1 = 35 pF *(2)*
t_{ZX2}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF *(3)*
t_{ZX3}	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF *(4)*
t_{IOE}	Output enable control delay	
t_{IN}	Input pad and buffer to FastTrack Interconnect delay	
t_{IN_DELAY}	Input pad and buffer to FastTrack Interconnect delay with additional delay turned on	

Table 21. Interconnect Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
t_{LOCAL}	LAB local interconnect delay	
t_{ROW}	Row interconnect routing delay	*(5)*
t_{COL}	Column interconnect routing delay	*(5)*
t_{DIN_D}	Dedicated input to LE data delay	*(5)*
t_{DIN_C}	Dedicated input to LE control delay	
$t_{LEGLOBAL}$	LE output to LE control via internally-generated global signal delay	*(5)*
$t_{LABCARRY}$	Routing delay for the carry-out of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

Table 22. External Reference Timing Parameters

Symbol	Parameter	Conditions
$\mathbf{t_1}$	Register-to-register test pattern	*(6)*
$\mathbf{t_{DRR}}$	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects	*(7)*

Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 2 of 2)							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{CO}		0.3		0.4		0.4	ns
t_{CLR}		0.4		0.4		0.5	ns
t_{C}		1.8		2.1		2.6	ns
t_{LD_CLR}		1.8		2.1		2.6	ns
$t_{CARRY\_TO\_CARRY}$		0.1		0.1		0.1	ns
$t_{REG\_TO\_CARRY}$		1.6		1.9		2.3	ns
$t_{DATA\_TO\_CARRY}$		2.1		2.5		3.0	ns
$t_{CARRY\_TO\_CASC}$		1.0		1.1		1.4	ns
$t_{CASC\_TO\_CASC}$		0.5		0.6		0.7	ns
$t_{REG\_TO\_CASC}$		1.4		1.7		2.1	ns
$t_{DATA\_TO\_CASC}$		1.1		1.2		1.5	ns
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

Table 25. IOE Timing Microparameters for EPF6010A & EPF6016A Devices							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{OD1}		1.9		2.2		2.7	ns
t_{OD2}		4.1		4.8		5.8	ns
t_{OD3}		5.8		6.8		8.3	ns
t_{XZ}		1.4		1.7		2.1	ns
t_{XZ1}		1.4		1.7		2.1	ns
t_{XZ2}		3.6		4.3		5.2	ns
t_{XZ3}		5.3		6.3		7.7	ns
t_{IOE}		0.5		0.6		0.7	ns
t_{IN}		3.6		4.1		5.1	ns
t_{IN_DELAY}		4.8		5.4		6.7	ns

Tables 29 through 33 show the timing information for EPF6016 devices.

Table 29. LE Timing Microparameters for EPF6016 Devices

Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
$t_{REG\_TO\_REG}$		2.2		2.8	ns
$t_{CASC\_TO\_REG}$		0.9		1.2	ns
$t_{CARRY\_TO\_REG}$		1.6		2.1	ns
$t_{DATA\_TO\_REG}$		2.4		3.0	ns
$t_{CASC\_TO\_OUT}$		1.3		1.7	ns
$t_{CARRY\_TO\_OUT}$		2.4		3.0	ns
$t_{DATA\_TO\_OUT}$		2.7		3.4	ns
$t_{REG\_TO\_OUT}$		0.3		0.5	ns
t_{SU}	1.1		1.6		ns
t_{H}	1.8		2.3		ns
t_{CO}		0.3		0.4	ns
t_{CLR}		0.5		0.6	ns
t_{C}		1.2		1.5	ns
t_{LD_CLR}		1.2		1.5	ns
$t_{CARRY\_TO\_CARRY}$		0.2		0.4	ns
$t_{REG\_TO\_CARRY}$		0.8		1.1	ns
$t_{DATA\_TO\_CARRY}$		1.7		2.2	ns
$t_{CARRY\_TO\_CASC}$		1.7		2.2	ns
$t_{CASC\_TO\_CASC}$		0.9		1.2	ns
$t_{REG\_TO\_CASC}$		1.6		2.0	ns
$t_{DATA\_TO\_CASC}$		1.7		2.1	ns
t_{CH}	4.0		4.0		ns
t_{CL}	4.0		4.0		ns

Table 30. IOE Timing Microparameters for EPF6016 Devices

Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
t_{OD1}		2.3		2.8	ns
t_{OD2}		4.6		5.1	ns

Table 33. External Timing Parameters for EPF6016 Devices					
Parameter	**Speed Grade**				**Unit**
	-2		**-3**		
	Min	**Max**	**Min**	**Max**	
t_{INSU}	3.2		4.1		ns
t_{INH}	0.0		0.0		ns
t_{OUTCO}	2.0	7.9	2.0	9.9	ns

Tables 34 through 38 show the timing information for EPF6024A devices.

Table 34. LE Timing Microparameters for EPF6024A Devices							
Parameter	**Speed Grade**						**Unit**
	-1		**-2**		**-3**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{REG\_TO\_REG}$		1.2		1.3		1.6	ns
$t_{CASC\_TO\_REG}$		0.7		0.8		1.0	ns
$t_{CARRY\_TO\_REG}$		1.6		1.8		2.2	ns
$t_{DATA\_TO\_REG}$		1.3		1.4		1.7	ns
$t_{CASC\_TO\_OUT}$		1.2		1.3		1.6	ns
$t_{CARRY\_TO\_OUT}$		2.0		2.2		2.6	ns
$t_{DATA\_TO\_OUT}$		1.8		2.1		2.6	ns
$t_{REG\_TO\_OUT}$		0.3		0.3		0.4	ns
t_{SU}	0.9		1.0		1.2		ns
t_H	1.3		1.4		1.7		ns
t_{CO}		0.2		0.3		0.3	ns
t_{CLR}		0.3		0.3		0.4	ns
t_C		1.9		2.1		2.5	ns
t_{LD_CLR}		1.9		2.1		2.5	ns
$t_{CARRY\_TO\_CARRY}$		0.2		0.2		0.3	ns
$t_{REG\_TO\_CARRY}$		1.4		1.6		1.9	ns
$t_{DATA\_TO\_CARRY}$		1.3		1.4		1.7	ns
$t_{CARRY\_TO\_CASC}$		1.1		1.2		1.4	ns
$t_{CASC\_TO\_CASC}$		0.7		0.8		1.0	ns
$t_{REG\_TO\_CASC}$		1.4		1.6		1.9	ns
$t_{DATA\_TO\_CASC}$		1.0		1.1		1.3	ns
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

Operating Modes

The FLEX 6000 architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. This process of physically loading the SRAM data into a FLEX 6000 device is known as configuration. During initialization—a process that occurs immediately after configuration—the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. The configuration and initialization processes of a device are referred to as *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 6000 devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and is used to dynamically reconfigure an entire system. Also, in-field system upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for a FLEX 6000 device can be loaded with one of three configuration schemes, which is chosen on the basis of the target application. An EPC1 or EPC1441 configuration device or intelligent controller can be used to control the configuration of a FLEX 6000 device, allowing automatic configuration on system power-up.

Multiple FLEX 6000 devices can be configured in any of the three configuration schemes by connecting the configuration enable input (`nCE`) and configuration enable output (`nCEO`) pins on each device.

Table 40 shows the data sources for each configuration scheme.

Table 40. Configuration Schemes

Configuration Scheme	Data Source
Configuration device	EPC1 or EPC1441 configuration device
Passive serial (PS)	BitBlaster™, ByteBlasterMV™, or MasterBlaster™ download cables, or serial data source
Passive serial asynchronous (PSA)	BitBlaster, ByteBlasterMV, or MasterBlaster download cables, or serial data source