

Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	132
Number of Logic Elements/Cells	1320
Total RAM Bits	-
Number of I/O	204
Number of Gates	16000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-BGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf6016bi256-3

General Description

The Altera® FLEX 6000 programmable logic device (PLD) family provides a low-cost alternative to high-volume gate array designs. FLEX 6000 devices are based on the OptiFLEX architecture, which minimizes die size while maintaining high performance and routability. The devices have reconfigurable SRAM elements, which give designers the flexibility to quickly change their designs during prototyping and design testing. Designers can also change functionality during operation via in-circuit reconfiguration.

FLEX 6000 devices are reprogrammable, and they are 100% tested prior to shipment. As a result, designers are not required to generate test vectors for fault coverage purposes, allowing them to focus on simulation and design verification. In addition, the designer does not need to manage inventories of different gate array designs. FLEX 6000 devices are configured on the board for the specific functionality required.

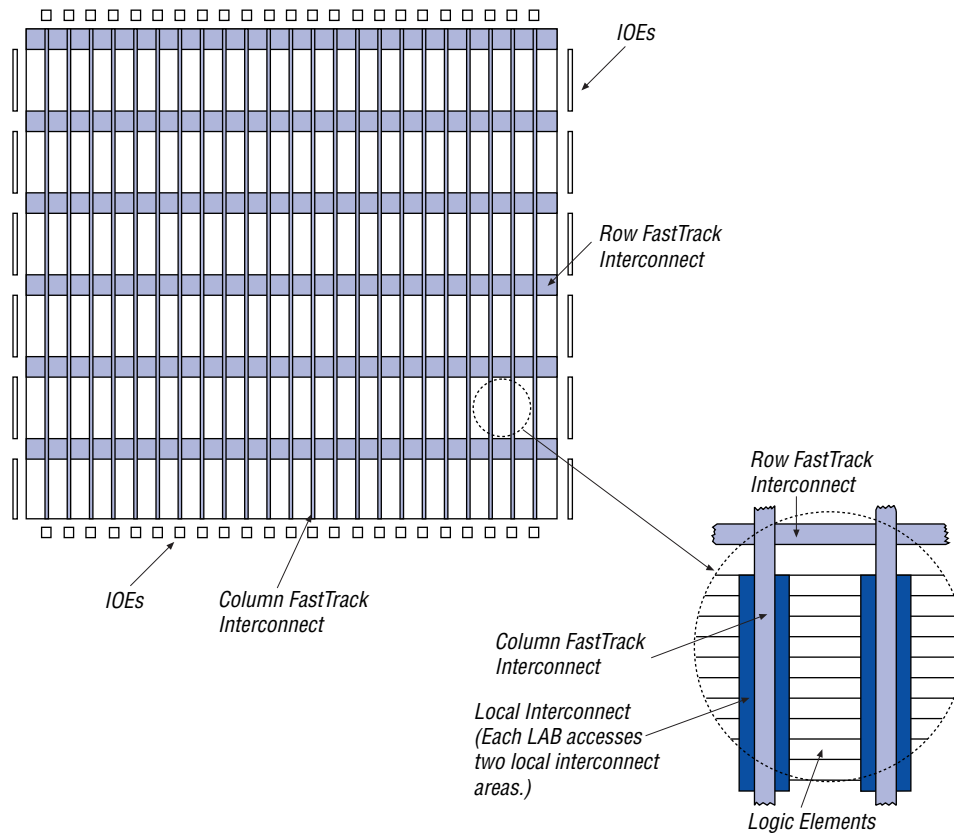
Table 3 shows FLEX 6000 performance for some common designs. All performance values shown were obtained using Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Table 3. FLEX 6000 Device Performance for Common Designs

Application	LEs Used	Performance			Units
		-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
16-bit loadable counter	16	172	153	133	MHz
16-bit accumulator	16	172	153	133	MHz
24-bit accumulator	24	136	123	108	MHz
16-to-1 multiplexer (pin-to-pin) (1)	10	12.1	13.4	16.6	ns
16 × 16 multiplier with a 4-stage pipeline	592	84	67	58	MHz

Note:

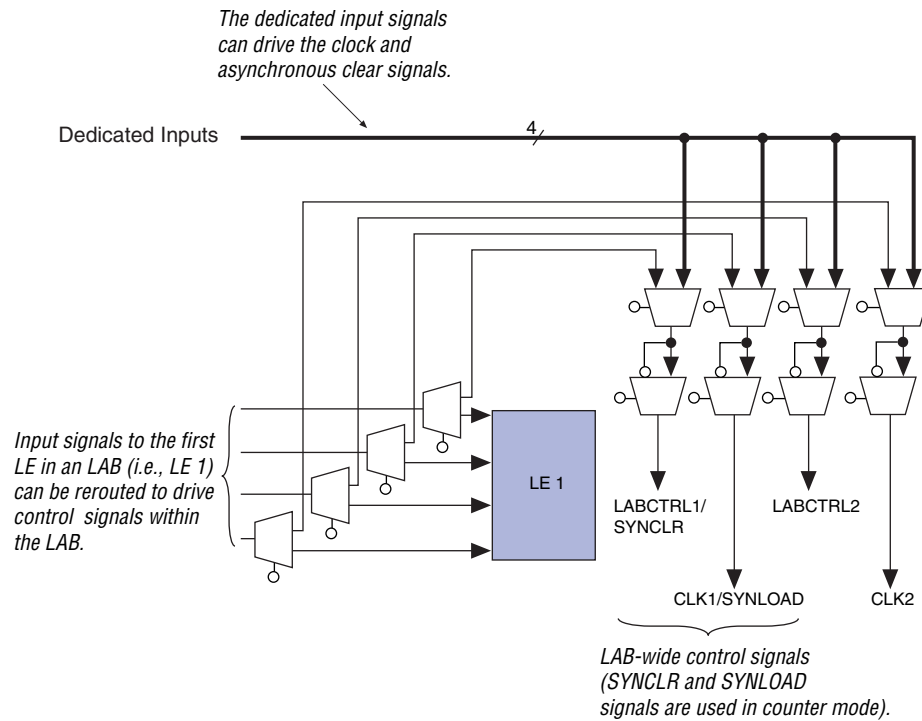
(1) This performance value is measured as a pin-to-pin delay.

Figure 1. OptiFLEX Architecture Block Diagram

FLEX 6000 devices provide four dedicated, global inputs that drive the control inputs of the flipflops to ensure efficient distribution of high-speed, low-skew control signals. These inputs use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. These inputs can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device. The dedicated global routing structure is built into the device, eliminating the need to create a clock tree.

Logic Array Block

An LAB consists of ten LEs, their associated carry and cascade chains, the LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 6000 architecture, and facilitates efficient routing with optimum device utilization and high performance.

Figure 3. LAB Control Signals

Logic Element

An LE, the smallest unit of logic in the FLEX 6000 architecture, has a compact size that provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. An LE contains a programmable flipflop, carry and cascade chains. Additionally, each LE drives both the local and the FastTrack Interconnect. See [Figure 4](#).

Carry Chain

The carry chain provides a very fast (0.1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 6000 architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Altera software during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

Because the first LE of each LAB can generate control signals for that LAB, the first LE in each LAB is not included in carry chains. In addition, the inputs of the first LE in each LAB may be used to generate synchronous clear and load enable signals for counters implemented with carry chains.

Carry chains longer than nine LEs are implemented automatically by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from an even-numbered LAB to another even-numbered LAB, or from an odd-numbered LAB to another odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the second LE of the third LAB in the row. In addition, the carry chain does not cross the middle of the row. For instance, in the EPF6016 device, the carry chain stops at the 11th LAB in a row and a new carry chain begins at the 12th LAB.

Figure 5 shows how an n -bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. Although the register can be bypassed for simple adders, it can be used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the FastTrack Interconnect.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The Altera software automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a 3-input function; the other generates a carry output. As shown in [Figure 7](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

The Altera software implements logic functions to use the arithmetic mode automatically where appropriate; the designer does not have to decide how the carry chain will be used.

Counter Mode

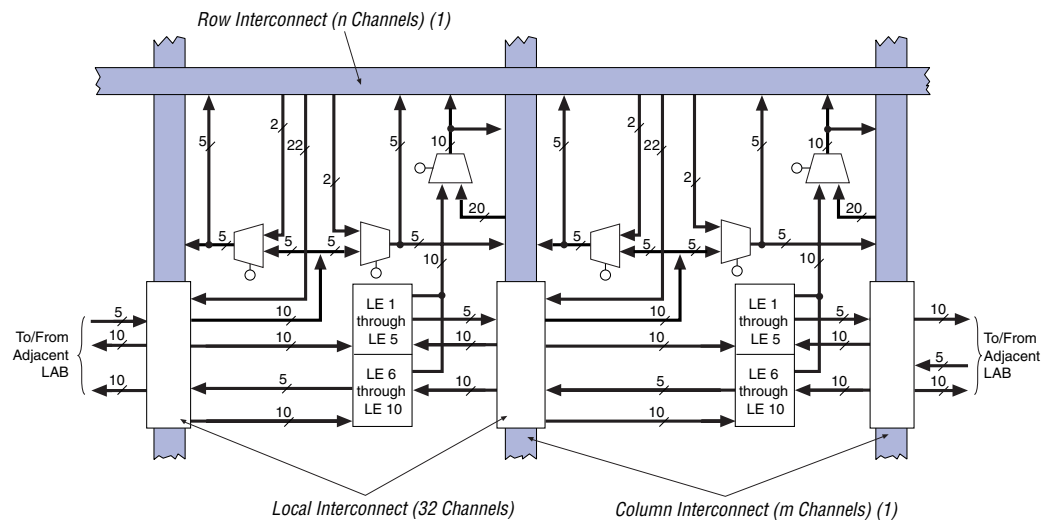
The counter mode offers counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in a LAB use counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. In addition, the Altera software automatically places registers that are not in the counter into other LABs.

The counter mode uses two 3-input LUTs: one generates the counter data and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load will override any signal carried on the cascade chain. The synchronous clear overrides the synchronous load.

The FastTrack Interconnect consists of column and row interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect, which routes signals between LABs in the same row, and also routes signals from I/O pins to LABs. Additionally, the local interconnect routes signals between LEs in the same LAB and in adjacent LABs. The column interconnect routes signals between rows and routes signals from I/O pins to rows.

LEs 1 through 5 of an LAB drive the local interconnect to the right, while LEs 6 through 10 drive the local interconnect to the left. The DATA1 and DATA3 inputs of each LE are driven by the local interconnect to the left; DATA2 and DATA4 are driven by the local interconnect to the right. The local interconnect also routes signals from LEs to I/O pins. Figure 9 shows an overview of the FLEX 6000 interconnect architecture. LEs in the first and last columns have drivers on both sides so that all LEs in the LAB can drive I/O pins via the local interconnect.

Figure 9. FastTrack Interconnect Architecture



Note:

- (1) For EPF6010A, EPF6016, and EPF6016A devices, $n = 144$ channels and $m = 20$ channels; for EPF6024A devices, $n = 186$ channels and $m = 30$ channels.

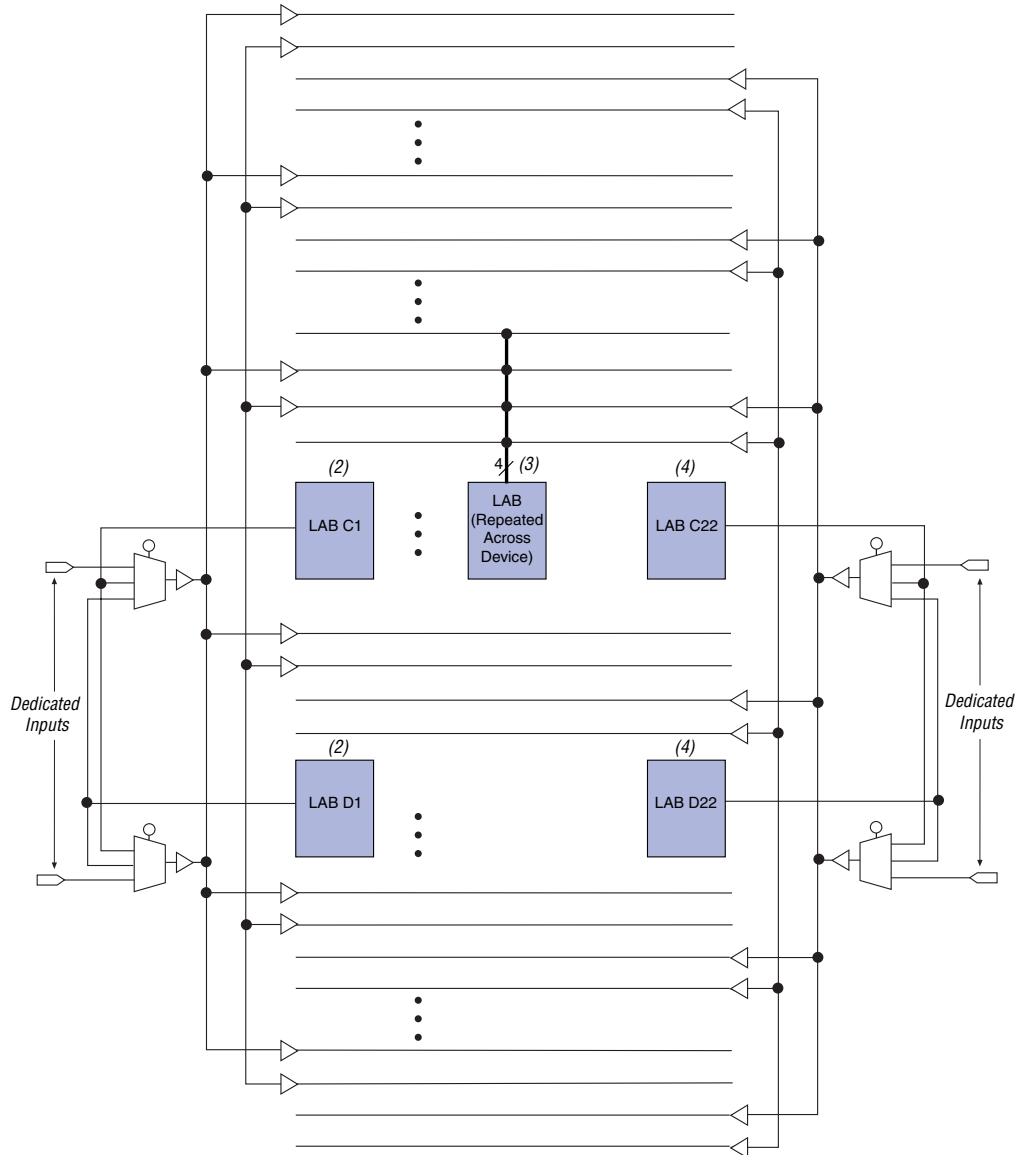
A row channel can be driven by an LE or by one of two column channels. These three signals feed a 3-to-1 multiplexer that connects to six specific row channels. Row channels drive into the local interconnect via multiplexers.

Each column of LABs is served by a dedicated column interconnect. The LEs in an LAB can drive the column interconnect. The LEs in an LAB, a column IOE, or a row interconnect can drive the column interconnect. The column interconnect can then drive another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect must be routed to the row interconnect before it can enter an LAB.

Each LE has a FastTrack Interconnect output and a local output. The FastTrack interconnect output can drive six row and two column lines directly; the local output drives the local interconnect. Each local interconnect channel driven by an LE can drive four row and two column channels. This feature provides additional flexibility, because each LE can drive any of ten row lines and four column lines.

In addition, LEs can drive global control signals. This feature is useful for distributing internally generated clock, asynchronous clear, and asynchronous preset signals. A pin-driven global signal can also drive data signals, which is useful for high-fan-out data signals.

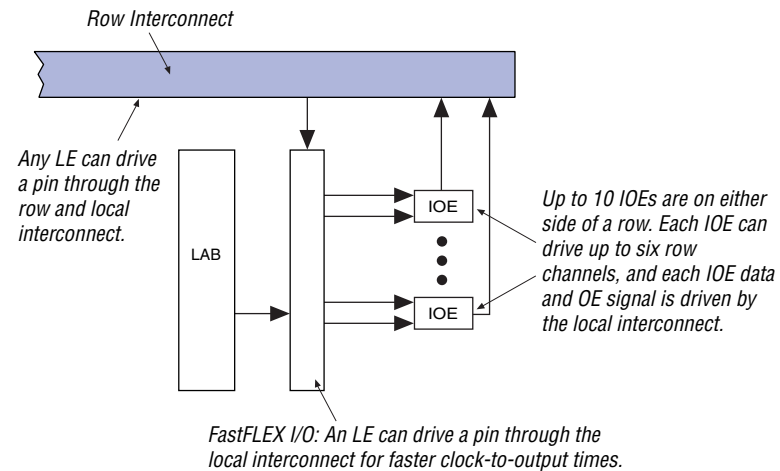
Each LAB drives two groups of local interconnects, which allows an LE to drive two LABs, or 20 LEs, via the local interconnect. The row-to-local multiplexers are used more efficiently, because the multiplexers can now drive two LABs. [Figure 10](#) shows how an LAB connects to row and column interconnects.

Figure 11. Global Clock & Clear Distribution *Note (1)***Notes:**

- (1) The global clock and clear distribution signals are shown for EPF6016 and EPF6016A devices. In EPF6010A devices, LABs in rows B and C drive global signals. In EPF6024A devices, LABs in rows C and E drive global signals.
- (2) The local interconnect from LABs C1 and D1 can drive two global control signals on the left side.
- (3) Global signals drive into every LAB as clock, asynchronous clear, preset, and data signals.
- (4) The local interconnect from LABs C22 and D22 can drive two global control signals on the right side.

Each IOE drives a row or column interconnect when used as an input or bidirectional pin. A row IOE can drive up to six row lines; a column IOE can drive up to two column lines. The input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time. Figure 13 shows how an IOE connects to a row interconnect, and Figure 14 shows how an IOE connects to a column interconnect.

Figure 13. IOE Connection to Row Interconnect



Open-drain output pins on 5.0-V or 3.3-V FLEX 6000 devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Output pins on 5.0-V FLEX 6000 devices with $V_{CCIO} = 3.3$ V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

Power Sequencing & Hot-Socketing

Because FLEX 6000 family devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into 3.3-V FLEX 6000 devices before and during power up without damaging the device. Additionally, FLEX 6000 devices do not drive out during power up. Once operating conditions are reached, FLEX 6000 devices operate as specified by the user.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 6000 devices provide JTAG BST circuitry that comply with the IEEE Std. 1149.1-1990 specification. [Table 8](#) shows JTAG instructions for FLEX 6000 devices. JTAG BST can be performed before or after configuration, but not during configuration (except when you disable JTAG support in user mode).

- 1 See [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#) for more information on JTAG BST circuitry.

Table 8. FLEX 6000 JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test result at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.

The instruction register length for FLEX 6000 devices is three bits. [Table 9](#) shows the boundary-scan register length for FLEX 6000 devices.

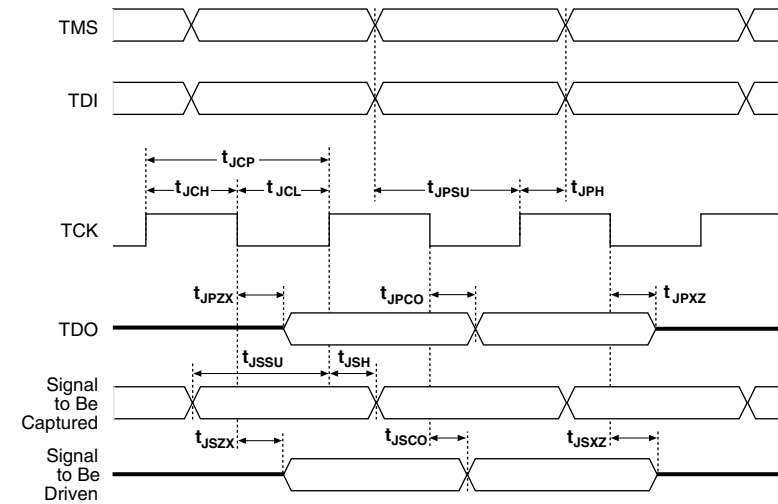
Table 9. FLEX 6000 Device Boundary-Scan Register Length	
Device	Boundary-Scan Register Length
EPF6010A	522
EPF6016	621
EPF6016A	522
EPF6024A	666

FLEX 6000 devices include a weak pull-up on JTAG pins.

f See [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#) for more information.

[Figure 16](#) shows the timing requirements for the JTAG signals.

Figure 16. JTAG Waveforms



[Table 10](#) shows the JTAG timing parameters and values for FLEX 6000 devices.

Operating Conditions

Tables 11 through 18 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V and 3.3-V FLEX 6000 devices.

Table 11. FLEX 6000 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground (2)	−2.0	7.0	V
V_I	DC input voltage		−2.0	7.0	V
I_{OUT}	DC output current, per pin		−25	25	mA
T_{STG}	Storage temperature	No bias	−65	150	° C
T_{AMB}	Ambient temperature	Under bias	−65	135	° C
T_J	Junction temperature	PQFP, TQFP, and BGA packages		135	° C

Table 12. FLEX 6000 5.0-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output buffers, 5.0-V operation	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
V_I	Input voltage		−0.5	$V_{CCINT} + 0.5$	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row can be calculated by adding the following parameters:

- LE register clock-to-output delay ($t_{CO} + t_{REG_TO_OUT}$)
- Routing delay ($t_{ROW} + t_{LOCAL}$)
- LE LUT delay ($t_{DATA_TO_REG}$)
- LE register setup time (t_{SU})

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

Timing simulation and delay prediction are available with the Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 19 shows the overall timing model, which maps the possible routing paths to and from the various elements of the FLEX 6000 device.

Table 20. IOE Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
t_{OD1}	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF (2)
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF (3)
t_{OD3}	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF (4)
t_{XZ}	Output buffer disable delay	C1 = 5 pF
t_{ZX1}	Output buffer enable delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF (2)
t_{ZX2}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF (3)
t_{ZX3}	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF (4)
t_{IOE}	Output enable control delay	
t_{IN}	Input pad and buffer to FastTrack Interconnect delay	
t_{IN_DELAY}	Input pad and buffer to FastTrack Interconnect delay with additional delay turned on	

Table 21. Interconnect Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
t_{LOCAL}	LAB local interconnect delay	
t_{ROW}	Row interconnect routing delay	(5)
t_{COL}	Column interconnect routing delay	(5)
t_{DIN_D}	Dedicated input to LE data delay	(5)
t_{DIN_C}	Dedicated input to LE control delay	
$t_{LEGLOBAL}$	LE output to LE control via internally-generated global signal delay	(5)
$t_{LABCARRY}$	Routing delay for the carry-out of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

Table 22. External Reference Timing Parameters

Symbol	Parameter	Conditions
t_1	Register-to-register test pattern	(6)
t_{DRR}	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects	(7)

Table 23. External Timing Parameters		
Symbol	Parameter	Conditions
t_{INSU}	Setup time with global clock at LE register	(8)
t_{INH}	Hold time with global clock at LE register	(8)
t_{OUTCO}	Clock-to-output delay with global clock with LE register using FastFLEX I/O pin	(8)

Notes to tables:

- (1) Microparameters are timing delays contributed by individual architectural elements and cannot be measured explicitly.
- (2) Operating conditions:
 $V_{\text{CCIO}} = 5.0 \text{ V} \pm 5\%$ for commercial use in 5.0-V FLEX 6000 devices.
 $V_{\text{CCIO}} = 5.0 \text{ V} \pm 10\%$ for industrial use in 5.0-V FLEX 6000 devices.
 $V_{\text{CCIO}} = 3.3 \text{ V} \pm 10\%$ for commercial or industrial use in 3.3-V FLEX 6000 devices.
- (3) Operating conditions:
 $V_{\text{CCIO}} = 3.3 \text{ V} \pm 10\%$ for commercial or industrial use in 5.0-V FLEX 6000 devices.
 $V_{\text{CCIO}} = 2.5 \text{ V} \pm 0.2 \text{ V}$ for commercial or industrial use in 3.3-V FLEX 6000 devices.
- (4) Operating conditions:
 $V_{\text{CCIO}} = 2.5 \text{ V}, 3.3 \text{ V}, \text{ or } 5.0 \text{ V}.$
- (5) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
- (6) This timing parameter shows the delay of a register-to-register test pattern and is used to determine speed grades. There are 12 LEs, including source and destination registers. The row and column interconnects between the registers vary in length.
- (7) This timing parameter is shown for reference and is specified by characterization.
- (8) This timing parameter is specified by characterization.

Tables 24 through 28 show the timing information for EPF6010A and EPF6016A devices.

Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 1 of 2)							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{REG_TO_REG}$		1.2		1.3		1.7	ns
$t_{CASC_TO_REG}$		0.9		1.0		1.2	ns
$t_{CARRY_TO_REG}$		0.9		1.0		1.2	ns
$t_{DATA_TO_REG}$		1.1		1.2		1.5	ns
$t_{CASC_TO_OUT}$		1.3		1.4		1.8	ns
$t_{CARRY_TO_OUT}$		1.6		1.8		2.3	ns
$t_{DATA_TO_OUT}$		1.7		2.0		2.5	ns
$t_{REG_TO_OUT}$		0.4		0.4		0.5	ns
t_{SU}	0.9		1.0		1.3		ns
t_H	1.4		1.7		2.1		ns

Table 26. Interconnect Timing Microparameters for EPF6010A & EPF6016A Devices

Table 26. Interconnect Timing Microparameters for EPF6010A & EPF6016A Devices							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LOCAL}		0.7		0.7		1.0	ns
t_{ROW}		2.9		3.2		3.2	ns
t_{COL}		1.2		1.3		1.4	ns
t_{DIN_D}		5.4		5.7		6.4	ns
t_{DIN_C}		4.3		5.0		6.1	ns
$t_{LEGLOBAL}$		2.6		3.0		3.7	ns
$t_{LABCARRY}$		0.7		0.8		0.9	ns
$t_{LABCASC}$		1.3		1.4		1.8	ns

Table 27. External Reference Timing Parameters for EPF6010A & EPF6016A Devices

Table 27. External Reference Timing Parameters for EPF6010A & EPF6016A Devices								
Parameter	Device	Speed Grade						Unit
		-1		-2		-3		
		Min	Max	Min	Max	Min	Max	
t ₁	EPF6010A		37.6		43.6		53.7	ns
	EPF6016A		38.0		44.0		54.1	ns

Table 28. External Timing Parameters for EPF6010A & EPF6016A Devices

Table 28. External Timing Parameters for EPF6010A & EPF6016A Devices							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t _{INSU}	2.1 (1)		2.4 (1)		3.3 (1)		ns
t _{INH}	0.2 (2)		0.3 (2)		0.1 (2)		ns
t _{OUTCO}	2.0	7.1	2.0	8.2	2.0	10.1	ns

Notes:

- (1) Setup times are longer when the *Increase Input Delay* option is turned on. The setup time values are shown with the *Increase Input Delay* option turned off.
- (2) Hold time is zero when the *Increase Input Delay* option is turned on.

Table 33. External Timing Parameters for EPF6016 Devices

Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
t _{INSU}	3.2		4.1		ns
t _{INH}	0.0		0.0		ns
t _{OUTCO}	2.0	7.9	2.0	9.9	ns

Tables 34 through 38 show the timing information for EPF6024A devices.

Table 34. LE Timing Microparameters for EPF6024A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{REG_TO_REG}$		1.2		1.3		1.6	ns
$t_{CASC_TO_REG}$		0.7		0.8		1.0	ns
$t_{CARRY_TO_REG}$		1.6		1.8		2.2	ns
$t_{DATA_TO_REG}$		1.3		1.4		1.7	ns
$t_{CASC_TO_OUT}$		1.2		1.3		1.6	ns
$t_{CARRY_TO_OUT}$		2.0		2.2		2.6	ns
$t_{DATA_TO_OUT}$		1.8		2.1		2.6	ns
$t_{REG_TO_OUT}$		0.3		0.3		0.4	ns
t_{SU}	0.9		1.0		1.2		ns
t_H	1.3		1.4		1.7		ns
t_{CO}		0.2		0.3		0.3	ns
t_{CLR}		0.3		0.3		0.4	ns
t_C		1.9		2.1		2.5	ns
t_{LD_CLR}		1.9		2.1		2.5	ns
$t_{CARRY_TO_CARRY}$		0.2		0.2		0.3	ns
$t_{REG_TO_CARRY}$		1.4		1.6		1.9	ns
$t_{DATA_TO_CARRY}$		1.3		1.4		1.7	ns
$t_{CARRY_TO_CASC}$		1.1		1.2		1.4	ns
$t_{CASC_TO_CASC}$		0.7		0.8		1.0	ns
$t_{REG_TO_CASC}$		1.4		1.6		1.9	ns
$t_{DATA_TO_CASC}$		1.0		1.1		1.3	ns
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

To better reflect actual designs, the power model (and the constant K in the power calculation equations shown above) for continuous interconnect FLEX devices assumes that LEs drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all LEs drive only one short interconnect segment. This assumption may lead to inaccurate results, compared to measured power consumption for an actual design in a segmented interconnect FPGA.

Figure 20 shows the relationship between the current and operating frequency for EPF6010A, EPF6016, EPF6016A, and EPF6024A devices.

Operating Modes

The FLEX 6000 architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. This process of physically loading the SRAM data into a FLEX 6000 device is known as configuration. During initialization—a process that occurs immediately after configuration—the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. The configuration and initialization processes of a device are referred to as *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 6000 devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and is used to dynamically reconfigure an entire system. Also, in-field system upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for a FLEX 6000 device can be loaded with one of three configuration schemes, which is chosen on the basis of the target application. An EPC1 or EPC1441 configuration device or intelligent controller can be used to control the configuration of a FLEX 6000 device, allowing automatic configuration on system power-up.

Multiple FLEX 6000 devices can be configured in any of the three configuration schemes by connecting the configuration enable input (nCE) and configuration enable output (nCEO) pins on each device.

Table 40 shows the data sources for each configuration scheme.

Table 40. Configuration Schemes	
Configuration Scheme	Data Source
Configuration device	EPC1 or EPC1441 configuration device
Passive serial (PS)	BitBlaster™, ByteBlasterMV™, or MasterBlaster™ download cables, or serial data source
Passive serial asynchronous (PSA)	BitBlaster, ByteBlasterMV, or MasterBlaster download cables, or serial data source



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
<http://www.altera.com>
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 544-7104
Literature Services:
(888) 3-ALTERA
lit_req@altera.com

Altera, BitBlaster, ByteBlasterMV, FastFlex, FastTrack, FineLine BGA, FLEX, MasterBlaster, MAX+PLUS II, MegaCore, MultiVolt, OptiFLEX, Quartus, SameFrame, and specific device designations are trademarks and/or service marks of Altera Corporation in the United States and other countries. Altera acknowledges the trademarks of other organizations for their respective products or services mentioned in this document, specifically: Verilog is a registered trademark of and Verilog-XL is a trademarks of Cadence Design Systems, Inc. DATA I/O is a registered trademark of Data I/O Corporation. HP is a registered trademark of Hewlett-Packard Company. Exemplar Logic is a registered trademark of Exemplar Logic, Inc. Pentium is a registered trademark of Intel Corporation. Mentor Graphics is a registered trademark of Mentor Graphics Corporation. OrCAD is a registered trademark of OrCAD Systems, Corporation. SPARCstation is a registered trademark of SPARC International, Inc. and is licensed exclusively to Sun Microsystems, Inc. Sun Workstation is a registered trademark of, and Sun is a registered trademark of Sun Microsystems, Inc. Synopsys is a registered trademark and DesignTime, HDL Compiler, and DesignWare are trademarks of Synopsys, Inc. VeriBest is a registered trademark of Viewlogic Systems, Inc. Viewlogic is a registered trademark of Viewlogic Systems, Inc. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

Copyright © 2001 Altera Corporation. All rights reserved.



I.S. EN ISO 9001

