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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	132
Number of Logic Elements/Cells	1320
Total RAM Bits	-
Number of I/O	171
Number of Gates	16000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf6016qi208-3n

Functional Description

The FLEX 6000 OptiFLEX architecture consists of logic elements (LEs). Each LE includes a 4-input look-up table (LUT), which can implement any 4-input function, a register, and dedicated paths for carry and cascade chain functions. Because each LE contains a register, a design can be easily pipelined without consuming more LEs. The specified gate count for FLEX 6000 devices includes all LUTs and registers.

LEs are combined into groups called logic array blocks (LABs); each LAB contains 10 LEs. The Altera software automatically places related LEs into the same LAB, minimizing the number of required interconnects. Each LAB can implement a medium-sized block of logic, such as a counter or multiplexer.

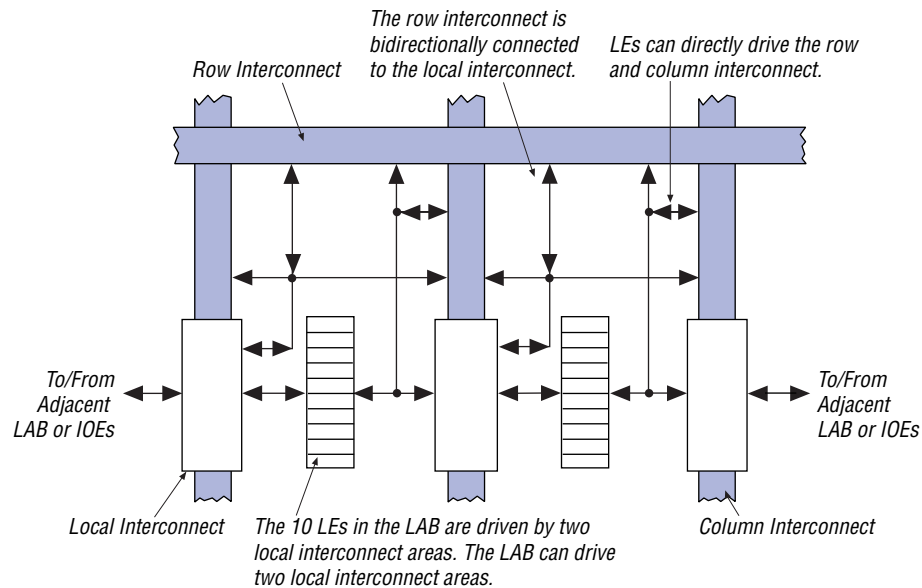
Signal interconnections within FLEX 6000 devices—and to and from device pins—are provided via the routing structure of the FastTrack Interconnect. The routing structure is a series of fast, continuous row and column channels that run the entire length and width of the device. Any LE or pin can feed or be fed by any other LE or pin via the FastTrack Interconnect. See “FastTrack Interconnect” on [page 17](#) of this data sheet for more information.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer. Each IOE is placed next to an LAB, where it can be driven by the local interconnect of that LAB. This feature allows fast clock-to-output times of less than 8 ns when a pin is driven by any of the 10 LEs in the adjacent LAB. Also, any LE can drive any pin via the row and column interconnect. I/O pins can drive the LE registers via the row and column interconnect, providing setup times as low as 2 ns and hold times of 0 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, and tri-state buffers.

[Figure 1](#) shows a block diagram of the FLEX 6000 OptiFLEX architecture. Each group of ten LEs is combined into an LAB, and the LABs are arranged into rows and columns. The LABs are interconnected by the FastTrack Interconnect. IOEs are located at the end of each FastTrack Interconnect row and column.

The interleaved LAB structure—an innovative feature of the FLEX 6000 architecture—allows each LAB to drive two local interconnects. This feature minimizes the use of the FastTrack Interconnect, providing higher performance. An LAB can drive 20 LEs in adjacent LABs via the local interconnect, which maximizes fitting flexibility while minimizing die size. See [Figure 2](#).

Figure 2. Logic Array Block



In most designs, the registers only use global clock and clear signals. However, in some cases, other clock or asynchronous clear signals are needed. In addition, counters may also have synchronous clear or load signals. In a design that uses non-global clock and clear signals, inputs from the first LE in an LAB are re-routed to drive the control signals for that LAB. See [Figure 3](#).

Carry Chain

The carry chain provides a very fast (0.1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 6000 architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Altera software during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

Because the first LE of each LAB can generate control signals for that LAB, the first LE in each LAB is not included in carry chains. In addition, the inputs of the first LE in each LAB may be used to generate synchronous clear and load enable signals for counters implemented with carry chains.

Carry chains longer than nine LEs are implemented automatically by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from an even-numbered LAB to another even-numbered LAB, or from an odd-numbered LAB to another odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the second LE of the third LAB in the row. In addition, the carry chain does not cross the middle of the row. For instance, in the EPF6016 device, the carry chain stops at the 11th LAB in a row and a new carry chain begins at the 12th LAB.

Figure 5 shows how an n -bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. Although the register can be bypassed for simple adders, it can be used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the FastTrack Interconnect.

Cascade Chain

The cascade chain enables the FLEX 6000 architecture to implement very wide fan-in functions. Adjacent LUTs can be used to implement portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR gate (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 0.5 ns per LE. Cascade chain logic can be created automatically by the Altera software during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of cascade chains for the appropriate functions.

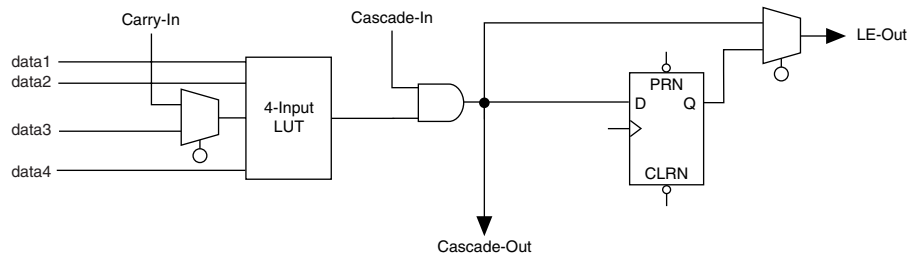
A cascade chain implementing an AND gate can use the register in the last LE; a cascade chain implementing an OR gate cannot use this register because of the inversion required to implement the OR gate.

Because the first LE of an LAB can generate control signals for that LAB, the first LE in each LAB is not included in cascade chains. Moreover, cascade chains longer than nine bits are automatically implemented by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from an even-numbered LAB to another even-numbered LAB, or from an odd-numbered LAB to another odd-numbered LAB. For example, the last LE of the first LAB in a row cascades to the second LE of the third LAB. The cascade chain does not cross the center of the row. For example, in an EPF6016 device, the cascade chain stops at the 11th LAB in a row and a new cascade chain begins at the 12th LAB.

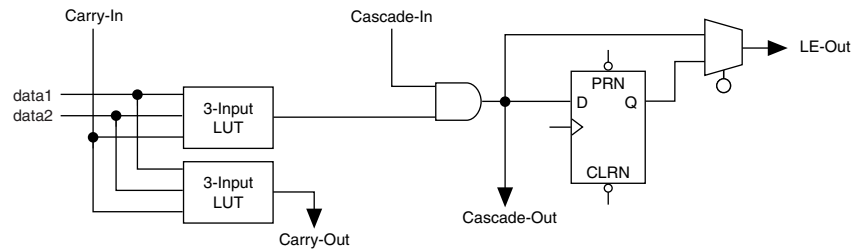
Figure 6 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. In this example, functions of $4n$ variables are implemented with n LEs. The cascade chain requires 3.4 ns to decode a 16-bit address.

Figure 7. LE Operating Modes

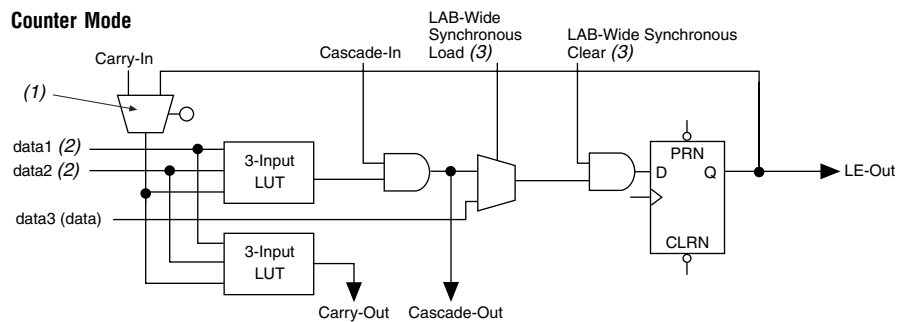
Normal Mode



Arithmetic Mode



Counter Mode



Notes:

- (1) The register feedback multiplexer is available on LE 2 of each LAB.
- (2) The data1 and data2 input signals can supply a clock enable, up or down control, or register feedback signals for all LEs other than the second LE in an LAB.
- (3) The LAB-wide synchronous clear and LAB-wide synchronous load affect all registers in an LAB.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The Altera software automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a 3-input function; the other generates a carry output. As shown in [Figure 7](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

The Altera software implements logic functions to use the arithmetic mode automatically where appropriate; the designer does not have to decide how the carry chain will be used.

Counter Mode

The counter mode offers counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in a LAB use counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. In addition, the Altera software automatically places registers that are not in the counter into other LABs.

The counter mode uses two 3-input LUTs: one generates the counter data and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load will override any signal carried on the cascade chain. The synchronous clear overrides the synchronous load.

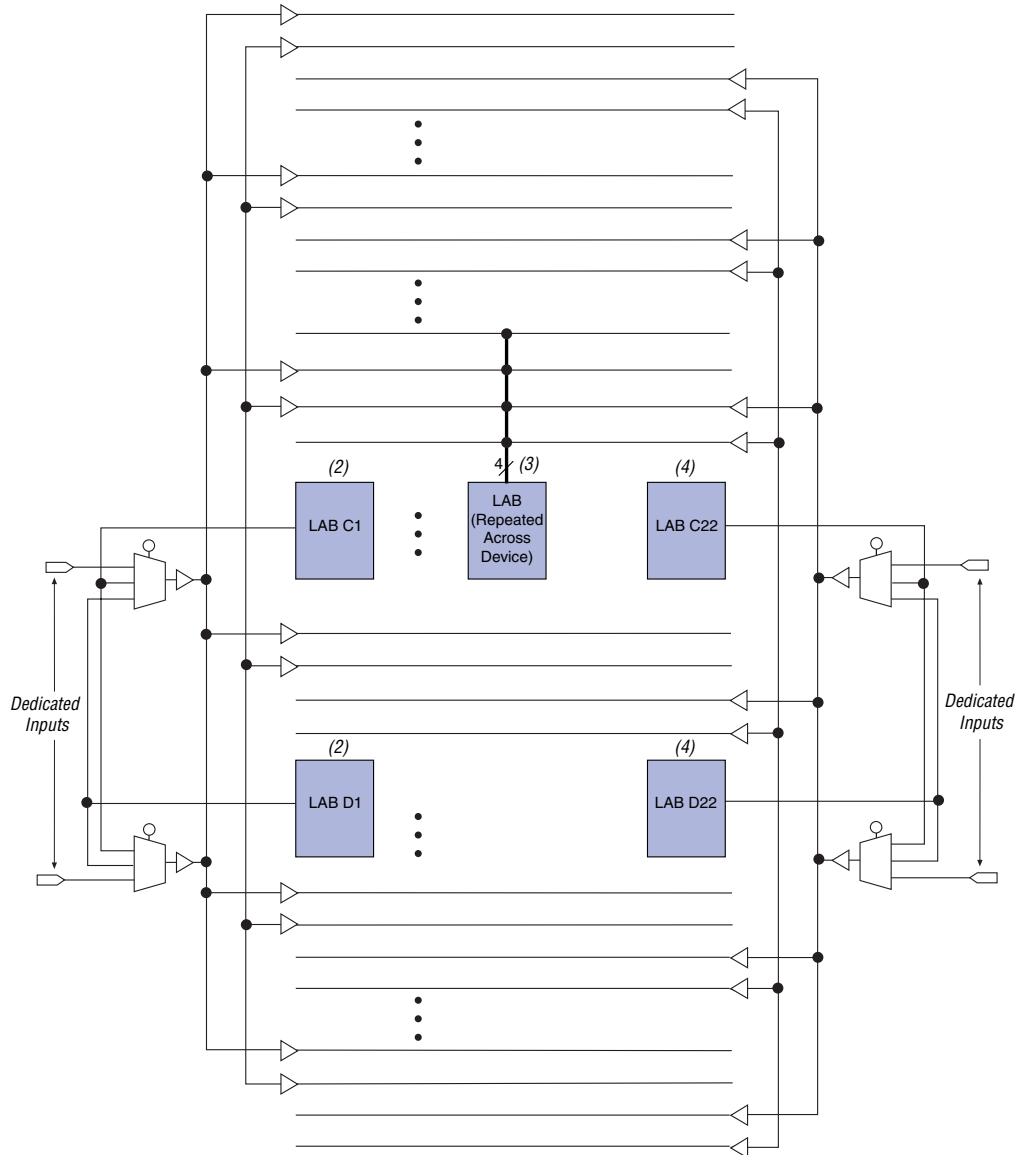
A row channel can be driven by an LE or by one of two column channels. These three signals feed a 3-to-1 multiplexer that connects to six specific row channels. Row channels drive into the local interconnect via multiplexers.

Each column of LABs is served by a dedicated column interconnect. The LEs in an LAB can drive the column interconnect. The LEs in an LAB, a column IOE, or a row interconnect can drive the column interconnect. The column interconnect can then drive another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect must be routed to the row interconnect before it can enter an LAB.

Each LE has a FastTrack Interconnect output and a local output. The FastTrack interconnect output can drive six row and two column lines directly; the local output drives the local interconnect. Each local interconnect channel driven by an LE can drive four row and two column channels. This feature provides additional flexibility, because each LE can drive any of ten row lines and four column lines.

In addition, LEs can drive global control signals. This feature is useful for distributing internally generated clock, asynchronous clear, and asynchronous preset signals. A pin-driven global signal can also drive data signals, which is useful for high-fan-out data signals.

Each LAB drives two groups of local interconnects, which allows an LE to drive two LABs, or 20 LEs, via the local interconnect. The row-to-local multiplexers are used more efficiently, because the multiplexers can now drive two LABs. [Figure 10](#) shows how an LAB connects to row and column interconnects.

Figure 11. Global Clock & Clear Distribution *Note (1)***Notes:**

- (1) The global clock and clear distribution signals are shown for EPF6016 and EPF6016A devices. In EPF6010A devices, LABs in rows B and C drive global signals. In EPF6024A devices, LABs in rows C and E drive global signals.
- (2) The local interconnect from LABs C1 and D1 can drive two global control signals on the left side.
- (3) Global signals drive into every LAB as clock, asynchronous clear, preset, and data signals.
- (4) The local interconnect from LABs C22 and D22 can drive two global control signals on the right side.

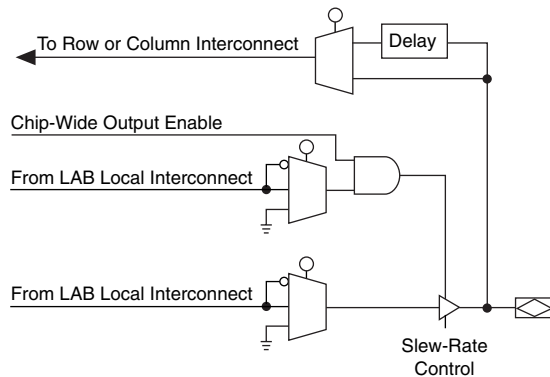
I/O Elements

An IOE contains a bidirectional I/O buffer and a tri-state buffer. IOEs can be used as input, output, or bidirectional pins. An IOE receives its data signals from the adjacent local interconnect, which can be driven by a row or column interconnect (allowing any LE in the device to drive the IOE) or by an adjacent LE (allowing fast clock-to-output delays). A FastFLEX™ I/O pin is a row or column output pin that receives its data signals from the adjacent local interconnect driven by an adjacent LE. The IOE receives its output enable signal through the same path, allowing individual output enables for every pin and permitting emulation of open-drain buffers. The Altera Compiler uses programmable inversion to invert the data or output enable signals automatically where appropriate. Open-drain emulation is provided by driving the data input low and toggling the OE of each IOE. This emulation is possible because there is one OE per pin.

A chip-wide output enable feature allows the designer to disable all pins of the device by asserting one pin (DEV_OE). This feature is useful during board debugging or testing.

Figure 12 shows the IOE block diagram.

Figure 12. IOE Block Diagram



Each IOE drives a row or column interconnect when used as an input or bidirectional pin. A row IOE can drive up to six row lines; a column IOE can drive up to two column lines. The input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time. Figure 13 shows how an IOE connects to a row interconnect, and Figure 14 shows how an IOE connects to a column interconnect.

Figure 13. IOE Connection to Row Interconnect

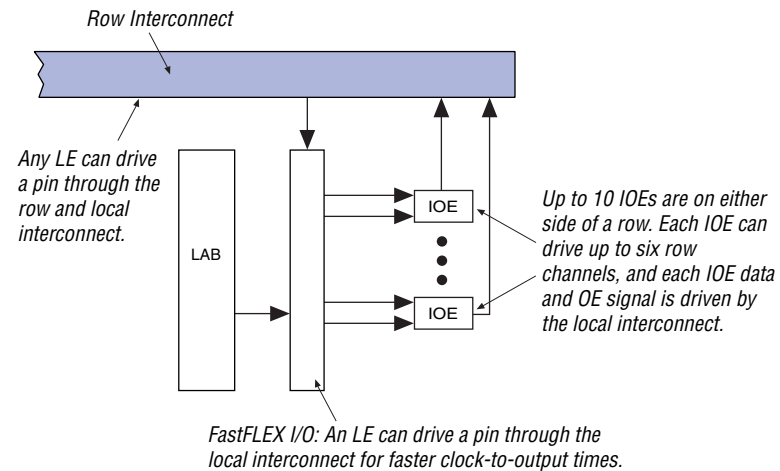
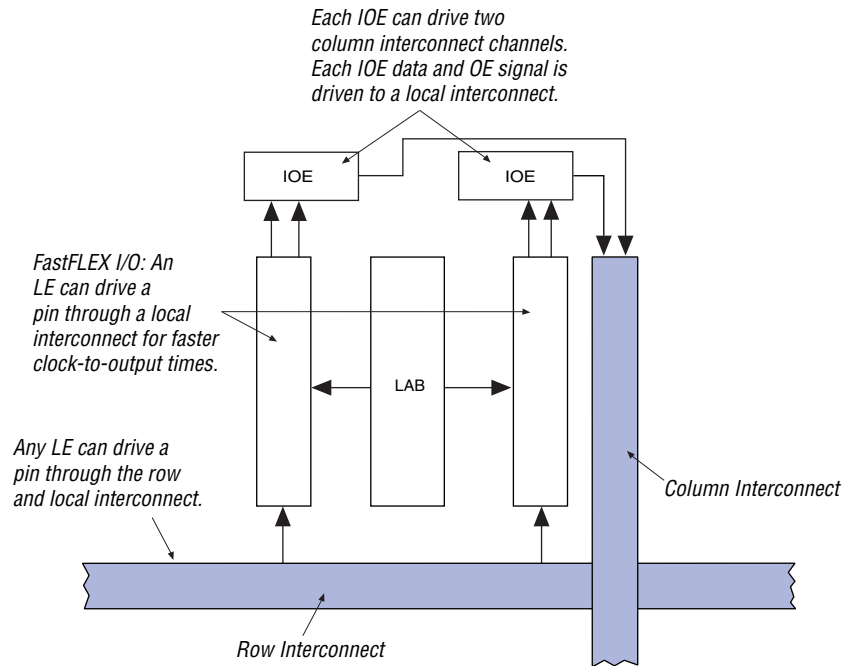


Figure 14. IOE Connection to Column Interconnect

SameFrame Pin-Outs

3.3-V FLEX 6000 devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support an EPF6016A device in a 100-pin FineLine BGA package or an EPF6024A device in a 256-pin FineLine BGA package.

The Altera software packages provide support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software packages generate pin-outs describing how to lay out a board to take advantage of this migration (see [Figure 15](#)).

Open-drain output pins on 5.0-V or 3.3-V FLEX 6000 devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Output pins on 5.0-V FLEX 6000 devices with $V_{CCIO} = 3.3$ V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

Power Sequencing & Hot-Socketing

Because FLEX 6000 family devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into 3.3-V FLEX 6000 devices before and during power up without damaging the device. Additionally, FLEX 6000 devices do not drive out during power up. Once operating conditions are reached, FLEX 6000 devices operate as specified by the user.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 6000 devices provide JTAG BST circuitry that comply with the IEEE Std. 1149.1-1990 specification. [Table 8](#) shows JTAG instructions for FLEX 6000 devices. JTAG BST can be performed before or after configuration, but not during configuration (except when you disable JTAG support in user mode).

- 1 See [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#) for more information on JTAG BST circuitry.

Table 8. FLEX 6000 JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test result at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.

The instruction register length for FLEX 6000 devices is three bits. [Table 9](#) shows the boundary-scan register length for FLEX 6000 devices.

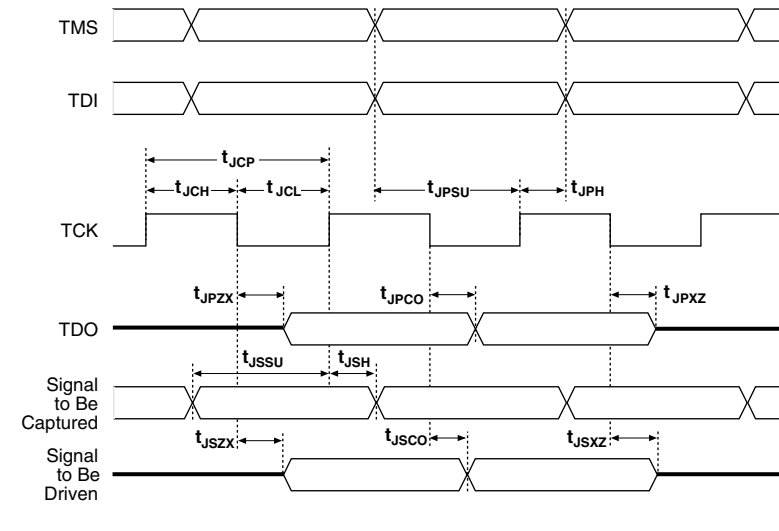
Table 9. FLEX 6000 Device Boundary-Scan Register Length	
Device	Boundary-Scan Register Length
EPF6010A	522
EPF6016	621
EPF6016A	522
EPF6024A	666

FLEX 6000 devices include a weak pull-up on JTAG pins.

f See [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#) for more information.

[Figure 16](#) shows the timing requirements for the JTAG signals.

Figure 16. JTAG Waveforms



[Table 10](#) shows the JTAG timing parameters and values for FLEX 6000 devices.

Operating Conditions

Tables 11 through 18 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V and 3.3-V FLEX 6000 devices.

Table 11. FLEX 6000 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground (2)	−2.0	7.0	V
V_I	DC input voltage		−2.0	7.0	V
I_{OUT}	DC output current, per pin		−25	25	mA
T_{STG}	Storage temperature	No bias	−65	150	° C
T_{AMB}	Ambient temperature	Under bias	−65	135	° C
T_J	Junction temperature	PQFP, TQFP, and BGA packages		135	° C

Table 12. FLEX 6000 5.0-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output buffers, 5.0-V operation	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
V_I	Input voltage		−0.5	$V_{CCINT} + 0.5$	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Figure 18 shows the typical output drive characteristics of 5.0-V and 3.3-V FLEX 6000 devices with 5.0-V, 3.3-V, and 2.5-V V_{CCIO} . When $V_{CCIO} = 5.0$ V on EPF6016 devices, the output driver is compliant with the *PCI Local Bus Specification, Revision 2.2* for 5.0-V operation. When $V_{CCIO} = 3.3$ V on the EPF6010A and EPF6016A devices, the output driver is compliant with the *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation.

Figure 18. Output Drive Characteristics

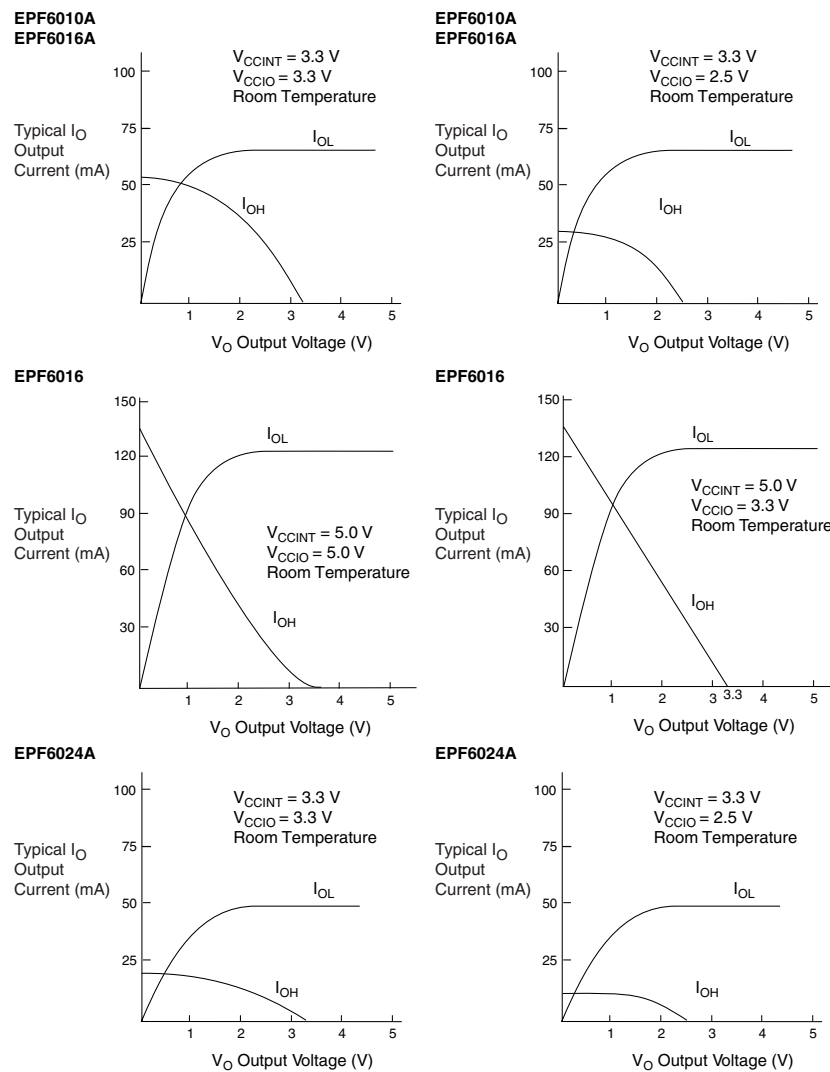


Table 23. External Timing Parameters		
Symbol	Parameter	Conditions
t_{INSU}	Setup time with global clock at LE register	(8)
t_{INH}	Hold time with global clock at LE register	(8)
t_{OUTCO}	Clock-to-output delay with global clock with LE register using FastFLEX I/O pin	(8)

Notes to tables:

- (1) Microparameters are timing delays contributed by individual architectural elements and cannot be measured explicitly.
- (2) Operating conditions:
 $V_{\text{CCIO}} = 5.0 \text{ V} \pm 5\%$ for commercial use in 5.0-V FLEX 6000 devices.
 $V_{\text{CCIO}} = 5.0 \text{ V} \pm 10\%$ for industrial use in 5.0-V FLEX 6000 devices.
 $V_{\text{CCIO}} = 3.3 \text{ V} \pm 10\%$ for commercial or industrial use in 3.3-V FLEX 6000 devices.
- (3) Operating conditions:
 $V_{\text{CCIO}} = 3.3 \text{ V} \pm 10\%$ for commercial or industrial use in 5.0-V FLEX 6000 devices.
 $V_{\text{CCIO}} = 2.5 \text{ V} \pm 0.2 \text{ V}$ for commercial or industrial use in 3.3-V FLEX 6000 devices.
- (4) Operating conditions:
 $V_{\text{CCIO}} = 2.5 \text{ V}, 3.3 \text{ V}, \text{ or } 5.0 \text{ V}.$
- (5) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
- (6) This timing parameter shows the delay of a register-to-register test pattern and is used to determine speed grades. There are 12 LEs, including source and destination registers. The row and column interconnects between the registers vary in length.
- (7) This timing parameter is shown for reference and is specified by characterization.
- (8) This timing parameter is specified by characterization.

Tables 24 through 28 show the timing information for EPF6010A and EPF6016A devices.

Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 1 of 2)							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{REG_TO_REG}$		1.2		1.3		1.7	ns
$t_{CASC_TO_REG}$		0.9		1.0		1.2	ns
$t_{CARRY_TO_REG}$		0.9		1.0		1.2	ns
$t_{DATA_TO_REG}$		1.1		1.2		1.5	ns
$t_{CASC_TO_OUT}$		1.3		1.4		1.8	ns
$t_{CARRY_TO_OUT}$		1.6		1.8		2.3	ns
$t_{DATA_TO_OUT}$		1.7		2.0		2.5	ns
$t_{REG_TO_OUT}$		0.4		0.4		0.5	ns
t_{SU}	0.9		1.0		1.3		ns
t_H	1.4		1.7		2.1		ns

Table 30. IOE Timing Microparameters for EPF6016 Devices

Table 30. IOE Timing Microparameters for EPF6016 Devices					
Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
t_{OD3}		4.7		5.2	ns
t_{XZ}		2.3		2.8	ns
t_{ZX1}		2.3		2.8	ns
t_{ZX2}		4.6		5.1	ns
t_{ZX3}		4.7		5.2	ns
t_{IOE}		0.5		0.6	ns
t_{IN}		3.3		4.0	ns
t_{IN_DELAY}		4.6		5.6	ns

Table 31. Interconnect Timing Microparameters for EPF6016 Devices

Table 31. Interconnect Timing Microparameters for EPF6016 Devices					
Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
t_{LOCAL}		0.8		1.0	ns
t_{ROW}		2.9		3.3	ns
t_{COL}		2.3		2.5	ns
t_{DIN_D}		4.9		6.0	ns
t_{DIN_C}		4.8		6.0	ns
$t_{LEGLOBAL}$		3.1		3.9	ns
$t_{LABCARRY}$		0.4		0.5	ns
$t_{LABCASC}$		0.8		1.0	ns

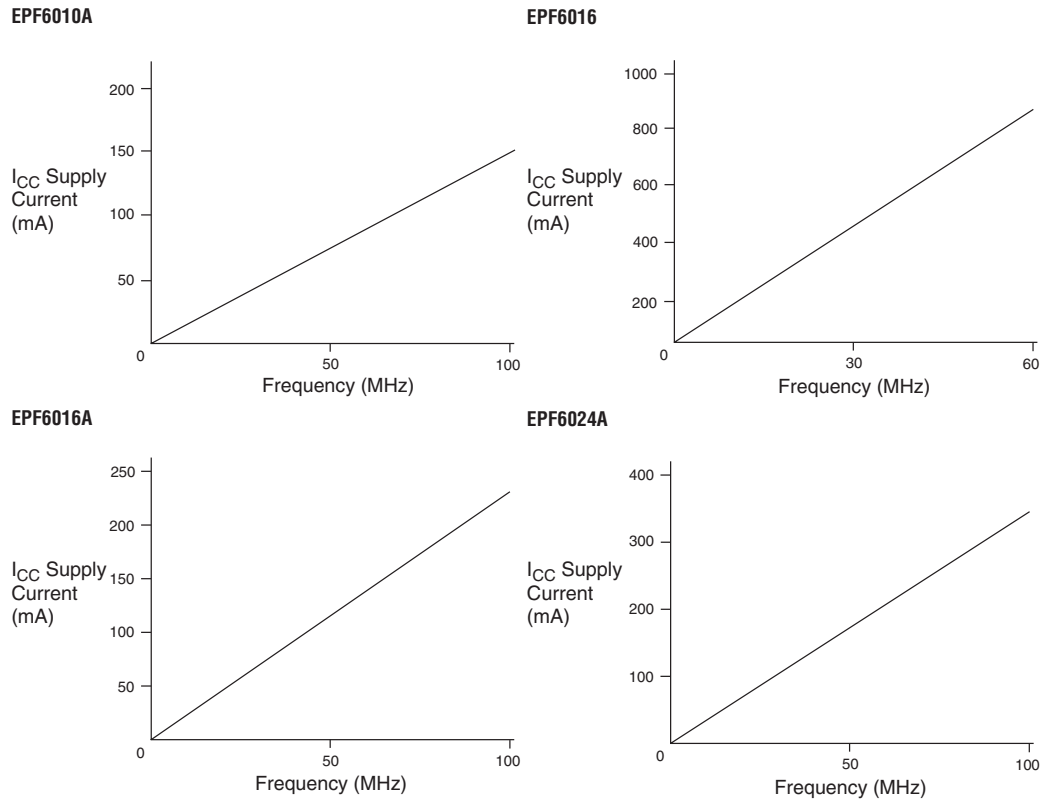
Table 32. External Reference Timing Parameters for EPF6016 Devices

Table 32. External Reference Timing Parameters for EPF6016 Devices					
Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
t ₁		53.0		65.0	ns
t _{DDR}		16.0		20.0	ns

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

To better reflect actual designs, the power model (and the constant K in the power calculation equations shown above) for continuous interconnect FLEX devices assumes that LEs drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all LEs drive only one short interconnect segment. This assumption may lead to inaccurate results, compared to measured power consumption for an actual design in a segmented interconnect FPGA.

Figure 20 shows the relationship between the current and operating frequency for EPF6010A, EPF6016, EPF6016A, and EPF6024A devices.

Figure 20. $I_{CCACTIVE}$ vs. Operating Frequency

Device Configuration & Operation

The FLEX 6000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.

- f See [Application Note 116 \(Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices\)](#) for detailed information on configuring FLEX 6000 devices, including sample schematics, timing diagrams, configuration options, pins names, and timing parameters.

Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.