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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	132
Number of Logic Elements/Cells	1320
Total RAM Bits	-
Number of I/O	117
Number of Gates	16000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf6016ti144-2

General Description

The Altera® FLEX 6000 programmable logic device (PLD) family provides a low-cost alternative to high-volume gate array designs. FLEX 6000 devices are based on the OptiFLEX architecture, which minimizes die size while maintaining high performance and routability. The devices have reconfigurable SRAM elements, which give designers the flexibility to quickly change their designs during prototyping and design testing. Designers can also change functionality during operation via in-circuit reconfiguration.

FLEX 6000 devices are reprogrammable, and they are 100% tested prior to shipment. As a result, designers are not required to generate test vectors for fault coverage purposes, allowing them to focus on simulation and design verification. In addition, the designer does not need to manage inventories of different gate array designs. FLEX 6000 devices are configured on the board for the specific functionality required.

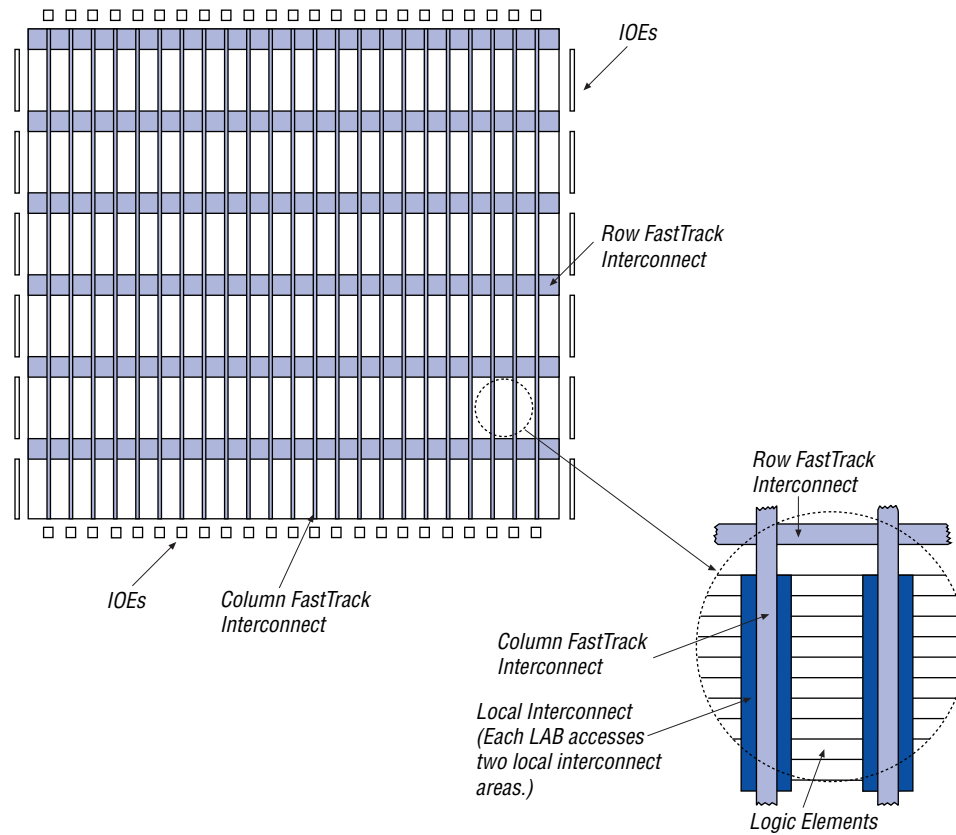
Table 3 shows FLEX 6000 performance for some common designs. All performance values shown were obtained using Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Table 3. FLEX 6000 Device Performance for Common Designs

Application	LEs Used	Performance			Units
		-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
16-bit loadable counter	16	172	153	133	MHz
16-bit accumulator	16	172	153	133	MHz
24-bit accumulator	24	136	123	108	MHz
16-to-1 multiplexer (pin-to-pin) (1)	10	12.1	13.4	16.6	ns
16 × 16 multiplier with a 4-stage pipeline	592	84	67	58	MHz

Note:

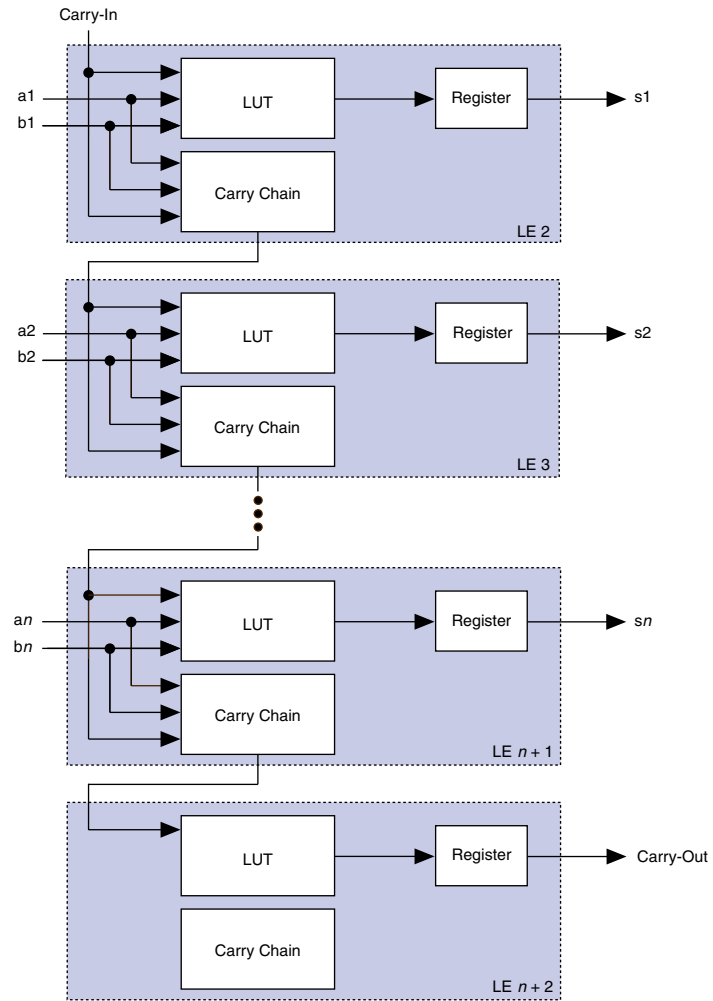
(1) This performance value is measured as a pin-to-pin delay.

Figure 1. OptiFLEX Architecture Block Diagram

FLEX 6000 devices provide four dedicated, global inputs that drive the control inputs of the flipflops to ensure efficient distribution of high-speed, low-skew control signals. These inputs use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. These inputs can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device. The dedicated global routing structure is built into the device, eliminating the need to create a clock tree.

Logic Array Block

An LAB consists of ten LEs, their associated carry and cascade chains, the LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 6000 architecture, and facilitates efficient routing with optimum device utilization and high performance.

Figure 5. Carry Chain Operation

Cascade Chain

The cascade chain enables the FLEX 6000 architecture to implement very wide fan-in functions. Adjacent LUTs can be used to implement portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR gate (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 0.5 ns per LE. Cascade chain logic can be created automatically by the Altera software during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of cascade chains for the appropriate functions.

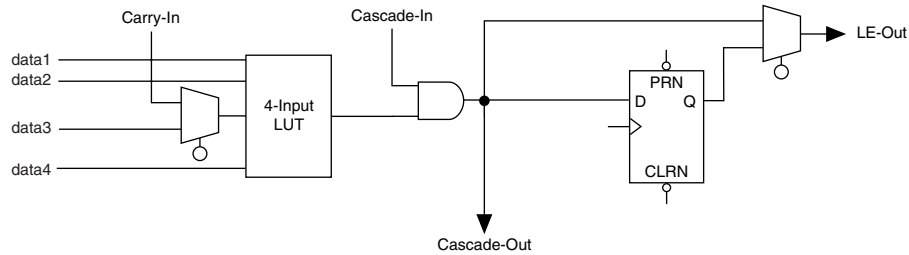
A cascade chain implementing an AND gate can use the register in the last LE; a cascade chain implementing an OR gate cannot use this register because of the inversion required to implement the OR gate.

Because the first LE of an LAB can generate control signals for that LAB, the first LE in each LAB is not included in cascade chains. Moreover, cascade chains longer than nine bits are automatically implemented by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from an even-numbered LAB to another even-numbered LAB, or from an odd-numbered LAB to another odd-numbered LAB. For example, the last LE of the first LAB in a row cascades to the second LE of the third LAB. The cascade chain does not cross the center of the row. For example, in an EPF6016 device, the cascade chain stops at the 11th LAB in a row and a new cascade chain begins at the 12th LAB.

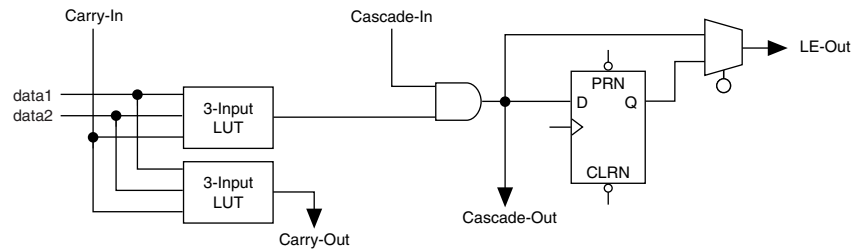
Figure 6 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. In this example, functions of $4n$ variables are implemented with n LEs. The cascade chain requires 3.4 ns to decode a 16-bit address.

Figure 7. LE Operating Modes

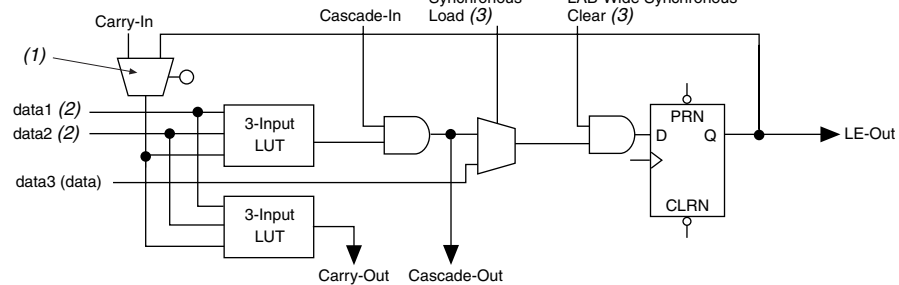
Normal Mode



Arithmetic Mode



Counter Mode



Notes:

- (1) The register feedback multiplexer is available on LE 2 of each LAB.
- (2) The data1 and data2 input signals can supply a clock enable, up or down control, or register feedback signals for all LEs other than the second LE in an LAB.
- (3) The LAB-wide synchronous clear and LAB-wide synchronous load affect all registers in an LAB.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The Altera software automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a 3-input function; the other generates a carry output. As shown in [Figure 7](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

The Altera software implements logic functions to use the arithmetic mode automatically where appropriate; the designer does not have to decide how the carry chain will be used.

Counter Mode

The counter mode offers counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in a LAB use counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. In addition, the Altera software automatically places registers that are not in the counter into other LABs.

The counter mode uses two 3-input LUTs: one generates the counter data and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load will override any signal carried on the cascade chain. The synchronous clear overrides the synchronous load.

Either the counter enable or the up/down control may be used for a given counter. Moreover, the synchronous load can be used as a count enable by routing the register output into the data input automatically when requested by the designer.

The second LE of each LAB has a special function for counter mode; the carry-in of the LE can be driven by a fast feedback path from the register. This function gives a faster counter speed for counter carry chains starting in the second LE of an LAB.

The Altera software implements functions to use the counter mode automatically where appropriate. The designer does not have to decide how the carry chain will be used.

Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

Clear & Preset Logic Control

Logic for the programmable register's clear and preset functions is controlled by the LAB-wide signals LABCTRL1 and LABCTRL2. The LE register has an asynchronous clear that can implement an asynchronous preset. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear or preset. Because the clear and preset functions are active-low, the Altera software automatically assigns a logic high to an unused clear or preset signal. The clear and preset logic is implemented in either the asynchronous clear or asynchronous preset mode, which is chosen during design entry (see [Figure 8](#)).

A row channel can be driven by an LE or by one of two column channels. These three signals feed a 3-to-1 multiplexer that connects to six specific row channels. Row channels drive into the local interconnect via multiplexers.

Each column of LABs is served by a dedicated column interconnect. The LEs in an LAB can drive the column interconnect. The LEs in an LAB, a column IOE, or a row interconnect can drive the column interconnect. The column interconnect can then drive another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect must be routed to the row interconnect before it can enter an LAB.

Each LE has a FastTrack Interconnect output and a local output. The FastTrack interconnect output can drive six row and two column lines directly; the local output drives the local interconnect. Each local interconnect channel driven by an LE can drive four row and two column channels. This feature provides additional flexibility, because each LE can drive any of ten row lines and four column lines.

In addition, LEs can drive global control signals. This feature is useful for distributing internally generated clock, asynchronous clear, and asynchronous preset signals. A pin-driven global signal can also drive data signals, which is useful for high-fan-out data signals.

Each LAB drives two groups of local interconnects, which allows an LE to drive two LABs, or 20 LEs, via the local interconnect. The row-to-local multiplexers are used more efficiently, because the multiplexers can now drive two LABs. [Figure 10](#) shows how an LAB connects to row and column interconnects.

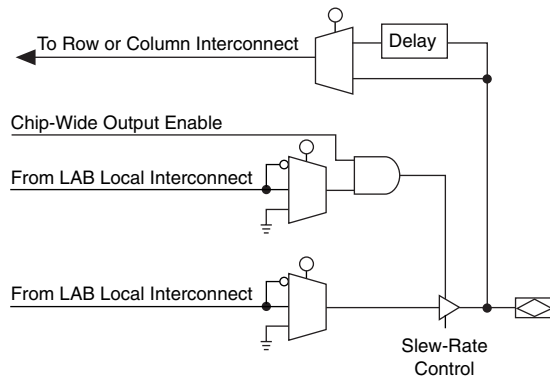
I/O Elements

An IOE contains a bidirectional I/O buffer and a tri-state buffer. IOEs can be used as input, output, or bidirectional pins. An IOE receives its data signals from the adjacent local interconnect, which can be driven by a row or column interconnect (allowing any LE in the device to drive the IOE) or by an adjacent LE (allowing fast clock-to-output delays). A FastFLEX™ I/O pin is a row or column output pin that receives its data signals from the adjacent local interconnect driven by an adjacent LE. The IOE receives its output enable signal through the same path, allowing individual output enables for every pin and permitting emulation of open-drain buffers. The Altera Compiler uses programmable inversion to invert the data or output enable signals automatically where appropriate. Open-drain emulation is provided by driving the data input low and toggling the OE of each IOE. This emulation is possible because there is one OE per pin.

A chip-wide output enable feature allows the designer to disable all pins of the device by asserting one pin (DEV_OE). This feature is useful during board debugging or testing.

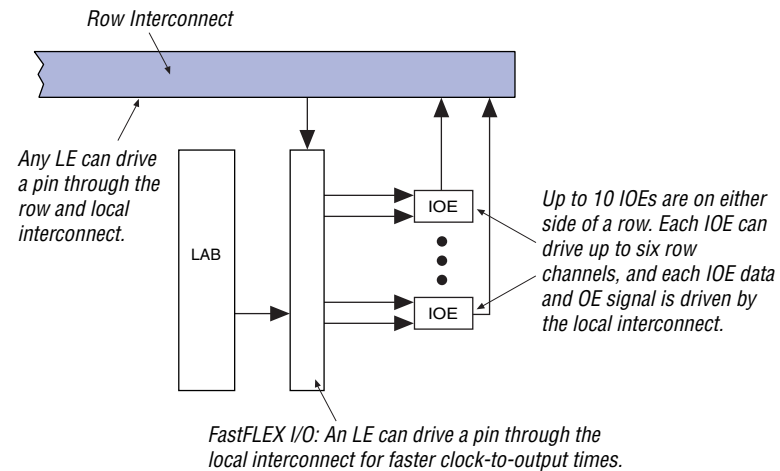
Figure 12 shows the IOE block diagram.

Figure 12. IOE Block Diagram



Each IOE drives a row or column interconnect when used as an input or bidirectional pin. A row IOE can drive up to six row lines; a column IOE can drive up to two column lines. The input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time. Figure 13 shows how an IOE connects to a row interconnect, and Figure 14 shows how an IOE connects to a column interconnect.

Figure 13. IOE Connection to Row Interconnect



The instruction register length for FLEX 6000 devices is three bits. [Table 9](#) shows the boundary-scan register length for FLEX 6000 devices.

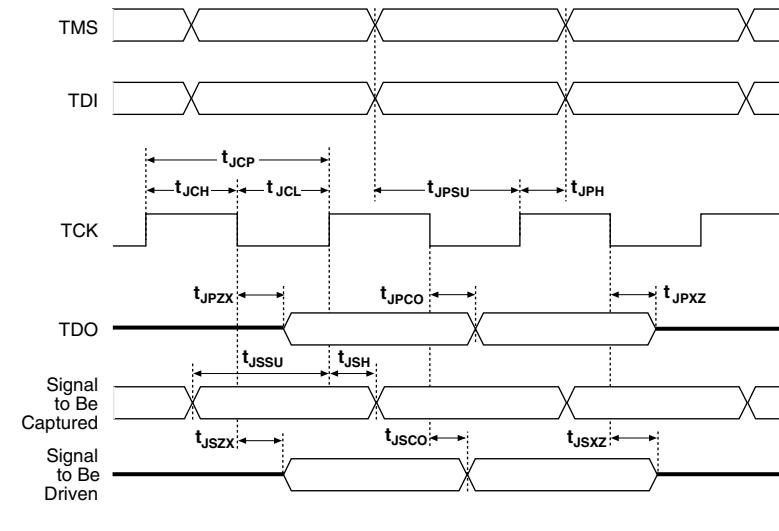
Table 9. FLEX 6000 Device Boundary-Scan Register Length	
Device	Boundary-Scan Register Length
EPF6010A	522
EPF6016	621
EPF6016A	522
EPF6024A	666

FLEX 6000 devices include a weak pull-up on JTAG pins.

f See [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#) for more information.

[Figure 16](#) shows the timing requirements for the JTAG signals.

Figure 16. JTAG Waveforms



[Table 10](#) shows the JTAG timing parameters and values for FLEX 6000 devices.

Table 10. JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock-to-output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock-to-output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

Generic Testing

Each FLEX 6000 device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 6000 devices are made under conditions equivalent to those shown in [Figure 17](#). Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 17. AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers without parentheses are for 5.0-V devices or outputs. Numbers in parentheses are for 3.3-V devices or outputs. Numbers in brackets are for 2.5-V devices or outputs.

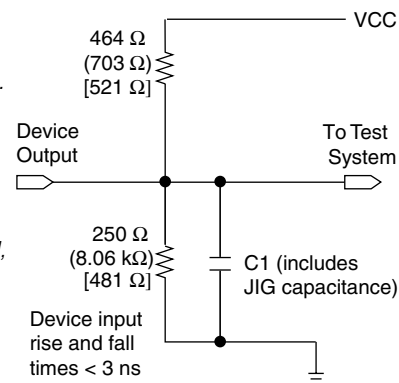


Table 13. FLEX 6000 5.0-V Device DC Operating Conditions Notes (5), (6)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		$V_{CCINT} + 0.5$	V
V_{IL}	Low-level input voltage		-0.5		0.8	V
V_{OH}	5.0-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 4.75$ V (7)	2.4			V
	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (7)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (7)	$V_{CCIO} - 0.2$			V
V_{OL}	5.0-V low-level TTL output voltage	$I_{OL} = 8$ mA DC, $V_{CCIO} = 4.75$ V (8)			0.45	V
	3.3-V low-level TTL output voltage	$I_{OL} = 8$ mA DC, $V_{CCIO} = 3.00$ V (8)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (8)			0.2	V
I_I	Input pin leakage current	$V_I = V_{CC}$ or ground (8)	-10		10	μ A
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CC}$ or ground (8)	-40		40	μ A
I_{CC0}	V_{CC} supply current (standby)	$V_I =$ ground, no load		0.5	5	mA

Table 14. FLEX 6000 5.0-V Device Capacitance Note (9)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance for I/O pin	$V_{IN} = 0$ V, $f = 1.0$ MHz		8	pF
C_{INCLK}	Input capacitance for dedicated input	$V_{IN} = 0$ V, $f = 1.0$ MHz		12	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		8	pF

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum V_{CC} rise time to 100 ms. V_{CC} must rise monotonically.
- (5) Typical values are for $T_A = 25^\circ$ C and $V_{CC} = 5.0$ V.
- (6) These values are specified under the FLEX 6000 Recommended Operating Conditions shown in Table 12 on page 31.
- (7) The I_{OH} parameter refers to high-level TTL or CMOS output current.
- (8) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (9) Capacitance is sample-tested only.

Table 15. FLEX 6000 3.3-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground (2)	−0.5	4.6	V
V_I	DC input voltage		−2.0	5.75	V
I_{OUT}	DC output current, per pin		−25	25	mA
T_{STG}	Storage temperature	No bias	−65	150	°C
T_{AMB}	Ambient temperature	Under bias	−65	135	°C
T_J	Junction temperature	PQFP, PLCC, and BGA packages		135	°C

Table 16. FLEX 6000 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.30 (2.30)	2.70 (2.70)	V
V_I	Input voltage		−0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating temperature	For commercial use	0	85	°C
		For industrial use	−40	100	°C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 17. FLEX 6000 3.3-V Device DC Operating Conditions <i>Notes (5), (6)</i>						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7		5.75	V
V_{IL}	Low-level input voltage		-0.5		0.8	V
V_{OH}	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (7)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (7)	$V_{CCIO} - 0.2$			V
	2.5-V high-level output voltage	$I_{OH} = -100$ μ A DC, $V_{CCIO} = 2.30$ V (7)	2.1			V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (7)	2.0			V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (7)	1.7			V
V_{OL}	3.3-V low-level TTL output voltage	$I_{OL} = 8$ mA DC, $V_{CCIO} = 3.00$ V (8)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (8)			0.2	V
	2.5-V low-level output voltage	$I_{OL} = 100$ μ A DC, $V_{CCIO} = 2.30$ V (8)			0.2	V
		$I_{OL} = 1$ mA DC, $V_{CCIO} = 2.30$ V (8)			0.4	V
		$I_{OL} = 2$ mA DC, $V_{CCIO} = 2.30$ V (8)			0.7	V
I_I	Input pin leakage current	$V_I = 5.3$ V to ground (8)	-10		10	μ A
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = 5.3$ V to ground (8)	-10		10	μ A
I_{CC0}	V_{CC} supply current (standby)	$V_I =$ ground, no load		0.5	5	mA

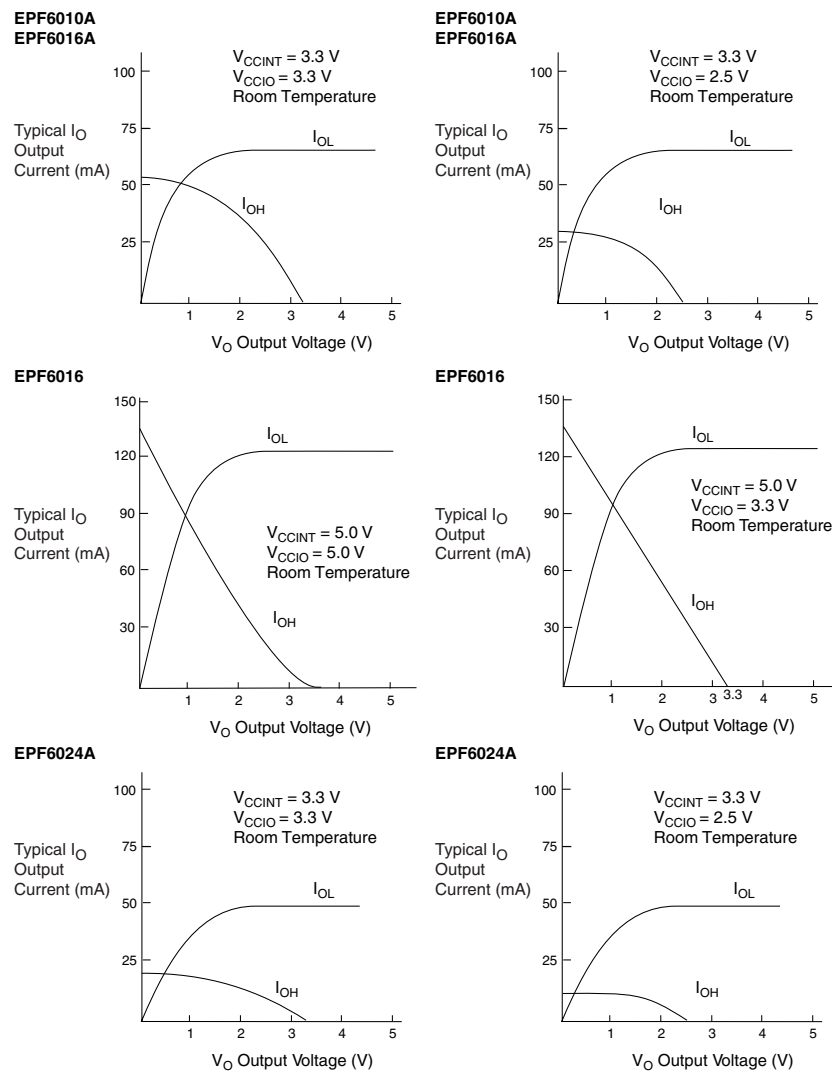
Table 18. FLEX 6000 3.3-V Device Capacitance <i>Note (9)</i>					
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance for I/O pin	$V_{IN} = 0$ V, $f = 1.0$ MHz		8	pF
C_{INCLK}	Input capacitance for dedicated input	$V_{IN} = 0$ V, $f = 1.0$ MHz		12	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		8	pF

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) The minimum DC input voltage is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
- (5) Typical values are for $T_A = 25^\circ$ C and $V_{CC} = 3.3$ V.
- (6) These values are specified under [Table 16 on page 33](#).
- (7) The I_{OH} parameter refers to high-level TTL or CMOS output current.
- (8) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (9) Capacitance is sample-tested only.

Figure 18 shows the typical output drive characteristics of 5.0-V and 3.3-V FLEX 6000 devices with 5.0-V, 3.3-V, and 2.5-V V_{CCIO} . When $V_{CCIO} = 5.0$ V on EPF6016 devices, the output driver is compliant with the *PCI Local Bus Specification, Revision 2.2* for 5.0-V operation. When $V_{CCIO} = 3.3$ V on the EPF6010A and EPF6016A devices, the output driver is compliant with the *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation.

Figure 18. Output Drive Characteristics



Tables 19 through 21 describe the FLEX 6000 internal timing microparameters, which are expressed as worst-case values. Using hand calculations, these parameters can be used to estimate design performance. However, before committing designs to silicon, actual worst-case performance should be modeled using timing simulation and timing analysis. Tables 22 and 23 describe FLEX 6000 external timing parameters.

Table 19. LE Timing Microparameters <i>Note (1)</i>		
Symbol	Parameter	Conditions
$t_{REG_TO_REG}$	LUT delay for LE register feedback in carry chain	
$t_{CASC_TO_REG}$	Cascade-in to register delay	
$t_{CARRY_TO_REG}$	Carry-in to register delay	
$t_{DATA_TO_REG}$	LE input to register delay	
$t_{CASC_TO_OUT}$	Cascade-in to LE output delay	
$t_{CARRY_TO_OUT}$	Carry-in to LE output delay	
$t_{DATA_TO_OUT}$	LE input to LE output delay	
$t_{REG_TO_OUT}$	Register output to LE output delay	
t_{SU}	LE register setup time before clock; LE register recovery time after asynchronous clear	
t_H	LE register hold time after clock	
t_{CO}	LE register clock-to-output delay	
t_{CLR}	LE register clear delay	
t_C	LE register control signal delay	
t_{LD_CLR}	Synchronous load or clear delay in counter mode	
$t_{CARRY_TO_CARRY}$	Carry-in to carry-out delay	
$t_{REG_TO_CARRY}$	Register output to carry-out delay	
$t_{DATA_TO_CARRY}$	LE input to carry-out delay	
$t_{CARRY_TO_CASC}$	Carry-in to cascade-out delay	
$t_{CASC_TO_CASC}$	Cascade-in to cascade-out delay	
$t_{REG_TO_CASC}$	Register-out to cascade-out delay	
$t_{DATA_TO_CASC}$	LE input to cascade-out delay	
t_{CH}	LE register clock high time	
t_{CL}	LE register clock low time	

Table 20. IOE Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
t_{OD1}	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF (2)
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF (3)
t_{OD3}	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF (4)
t_{XZ}	Output buffer disable delay	C1 = 5 pF
t_{ZX1}	Output buffer enable delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF (2)
t_{ZX2}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF (3)
t_{ZX3}	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF (4)
t_{IOE}	Output enable control delay	
t_{IN}	Input pad and buffer to FastTrack Interconnect delay	
t_{IN_DELAY}	Input pad and buffer to FastTrack Interconnect delay with additional delay turned on	

Table 21. Interconnect Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
t_{LOCAL}	LAB local interconnect delay	
t_{ROW}	Row interconnect routing delay	(5)
t_{COL}	Column interconnect routing delay	(5)
t_{DIN_D}	Dedicated input to LE data delay	(5)
t_{DIN_C}	Dedicated input to LE control delay	
$t_{LEGLOBAL}$	LE output to LE control via internally-generated global signal delay	(5)
$t_{LABCARRY}$	Routing delay for the carry-out of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

Table 22. External Reference Timing Parameters

Symbol	Parameter	Conditions
t_1	Register-to-register test pattern	(6)
t_{DRR}	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects	(7)

Table 23. External Timing Parameters		
Symbol	Parameter	Conditions
t_{INSU}	Setup time with global clock at LE register	(8)
t_{INH}	Hold time with global clock at LE register	(8)
t_{OUTCO}	Clock-to-output delay with global clock with LE register using FastFLEX I/O pin	(8)

Notes to tables:

- (1) Microparameters are timing delays contributed by individual architectural elements and cannot be measured explicitly.
- (2) Operating conditions:
 $V_{\text{CCIO}} = 5.0 \text{ V} \pm 5\%$ for commercial use in 5.0-V FLEX 6000 devices.
 $V_{\text{CCIO}} = 5.0 \text{ V} \pm 10\%$ for industrial use in 5.0-V FLEX 6000 devices.
 $V_{\text{CCIO}} = 3.3 \text{ V} \pm 10\%$ for commercial or industrial use in 3.3-V FLEX 6000 devices.
- (3) Operating conditions:
 $V_{\text{CCIO}} = 3.3 \text{ V} \pm 10\%$ for commercial or industrial use in 5.0-V FLEX 6000 devices.
 $V_{\text{CCIO}} = 2.5 \text{ V} \pm 0.2 \text{ V}$ for commercial or industrial use in 3.3-V FLEX 6000 devices.
- (4) Operating conditions:
 $V_{\text{CCIO}} = 2.5 \text{ V}, 3.3 \text{ V}, \text{ or } 5.0 \text{ V}.$
- (5) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
- (6) This timing parameter shows the delay of a register-to-register test pattern and is used to determine speed grades. There are 12 LEs, including source and destination registers. The row and column interconnects between the registers vary in length.
- (7) This timing parameter is shown for reference and is specified by characterization.
- (8) This timing parameter is specified by characterization.

Tables 24 through 28 show the timing information for EPF6010A and EPF6016A devices.

Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 1 of 2)							
Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{REG_TO_REG}$		1.2		1.3		1.7	ns
$t_{CASC_TO_REG}$		0.9		1.0		1.2	ns
$t_{CARRY_TO_REG}$		0.9		1.0		1.2	ns
$t_{DATA_TO_REG}$		1.1		1.2		1.5	ns
$t_{CASC_TO_OUT}$		1.3		1.4		1.8	ns
$t_{CARRY_TO_OUT}$		1.6		1.8		2.3	ns
$t_{DATA_TO_OUT}$		1.7		2.0		2.5	ns
$t_{REG_TO_OUT}$		0.4		0.4		0.5	ns
t_{SU}	0.9		1.0		1.3		ns
t_H	1.4		1.7		2.1		ns

Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.