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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	196
Number of Logic Elements/Cells	1960
Total RAM Bits	-
Number of I/O	171
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf6024aqc208-3n

Functional Description

The FLEX 6000 OptiFLEX architecture consists of logic elements (LEs). Each LE includes a 4-input look-up table (LUT), which can implement any 4-input function, a register, and dedicated paths for carry and cascade chain functions. Because each LE contains a register, a design can be easily pipelined without consuming more LEs. The specified gate count for FLEX 6000 devices includes all LUTs and registers.

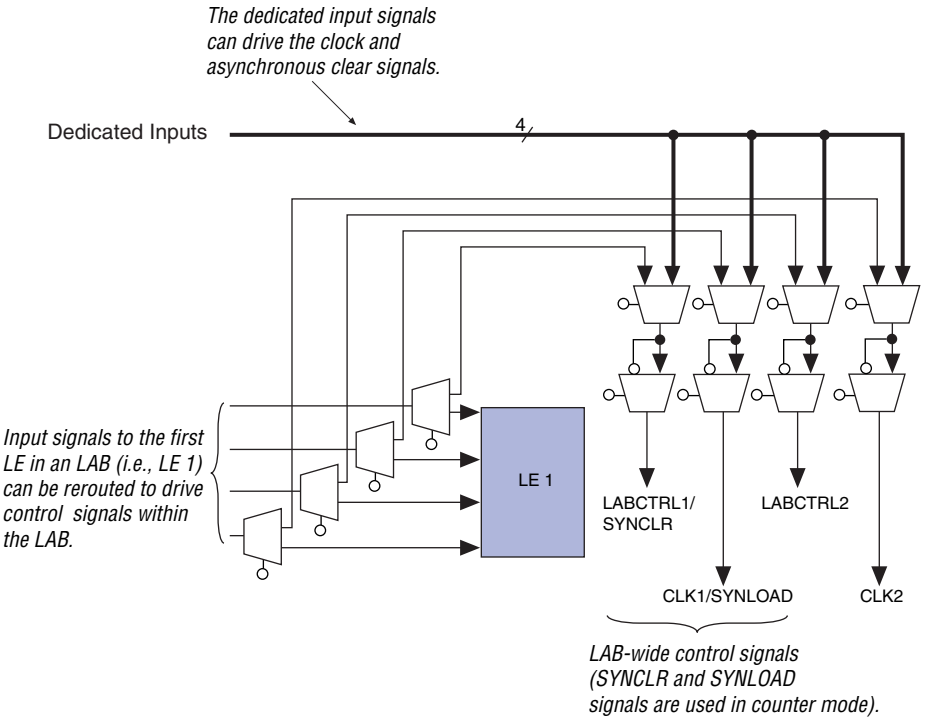
LEs are combined into groups called logic array blocks (LABs); each LAB contains 10 LEs. The Altera software automatically places related LEs into the same LAB, minimizing the number of required interconnects. Each LAB can implement a medium-sized block of logic, such as a counter or multiplexer.

Signal interconnections within FLEX 6000 devices—and to and from device pins—are provided via the routing structure of the FastTrack Interconnect. The routing structure is a series of fast, continuous row and column channels that run the entire length and width of the device. Any LE or pin can feed or be fed by any other LE or pin via the FastTrack Interconnect. See "FastTrack Interconnect" on page 17 of this data sheet for more information.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer. Each IOE is placed next to an LAB, where it can be driven by the local interconnect of that LAB. This feature allows fast clock-to-output times of less than 8 ns when a pin is driven by any of the 10 LEs in the adjacent LAB. Also, any LE can drive any pin via the row and column interconnect. I/O pins can drive the LE registers via the row and column interconnect, providing setup times as low as 2 ns and hold times of 0 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, and tri-state buffers.

Figure 1 shows a block diagram of the FLEX 6000 OptiFLEX architecture. Each group of ten LEs is combined into an LAB, and the LABs are arranged into rows and columns. The LABs are interconnected by the FastTrack Interconnect. IOEs are located at the end of each FastTrack Interconnect row and column.

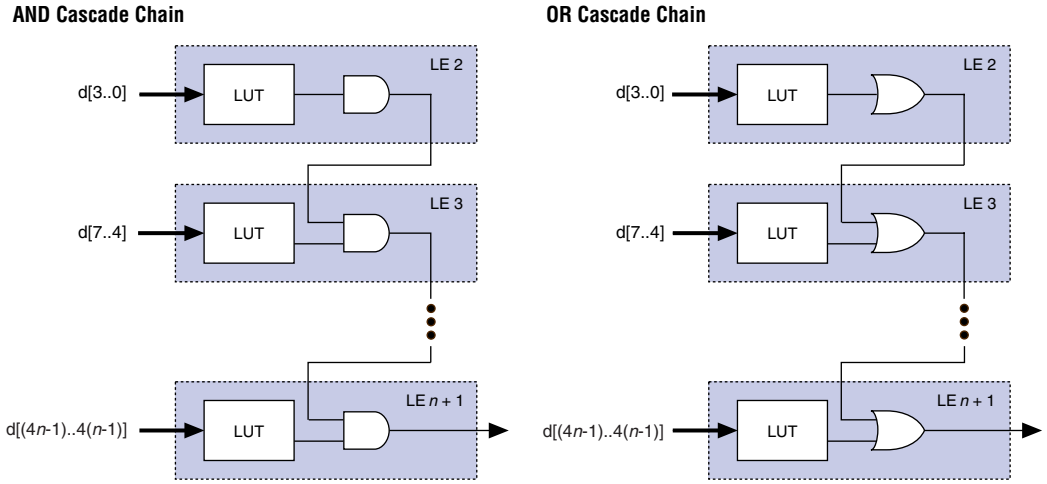
Figure 3. LAB Control Signals



Logic Element

An LE, the smallest unit of logic in the FLEX 6000 architecture, has a compact size that provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. An LE contains a programmable flipflop, carry and cascade chains. Additionally, each LE drives both the local and the FastTrack Interconnect. See Figure 4.

Figure 6. Cascade Chain Operation



LE Operating Modes

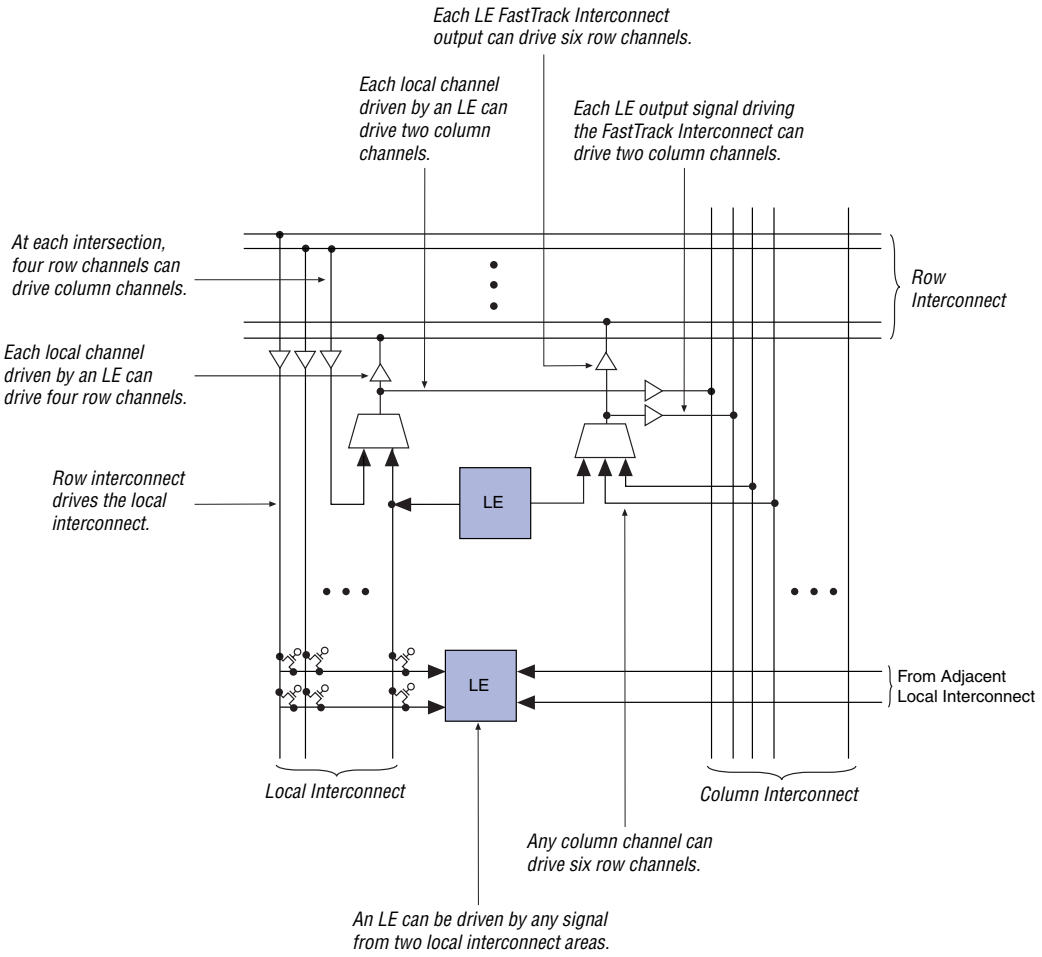
The FLEX 6000 LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, synchronous clear, and synchronous load control for the register. The Altera software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions to use an LE operating mode for optimal performance.

Figure 7 shows the LE operating modes.

Figure 10. LAB Connections to Row & Column Interconnects



For improved routability, the row interconnect consists of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-length channel, which saves the other half of the channel for the other half of the row. One-third of the row channels are half-length channels.

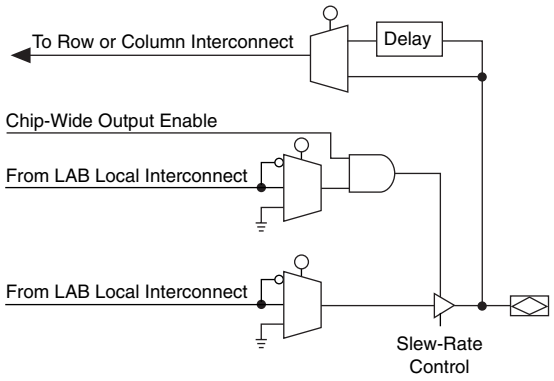
I/O Elements

An IOE contains a bidirectional I/O buffer and a tri-state buffer. IOEs can be used as input, output, or bidirectional pins. An IOE receives its data signals from the adjacent local interconnect, which can be driven by a row or column interconnect (allowing any LE in the device to drive the IOE) or by an adjacent LE (allowing fast clock-to-output delays). A FastFLEX™ I/O pin is a row or column output pin that receives its data signals from the adjacent local interconnect driven by an adjacent LE. The IOE receives its output enable signal through the same path, allowing individual output enables for every pin and permitting emulation of open-drain buffers. The Altera Compiler uses programmable inversion to invert the data or output enable signals automatically where appropriate. Open-drain emulation is provided by driving the data input low and toggling the OE of each IOE. This emulation is possible because there is one OE per pin.

A chip-wide output enable feature allows the designer to disable all pins of the device by asserting one pin (DEV_OE). This feature is useful during board debugging or testing.

Figure 12 shows the IOE block diagram.

Figure 12. IOE Block Diagram



Each IOE drives a row or column interconnect when used as an input or bidirectional pin. A row IOE can drive up to six row lines; a column IOE can drive up to two column lines. The input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time. Figure 13 shows how an IOE connects to a row interconnect, and Figure 14 shows how an IOE connects to a column interconnect.

Figure 13. IOE Connection to Row Interconnect

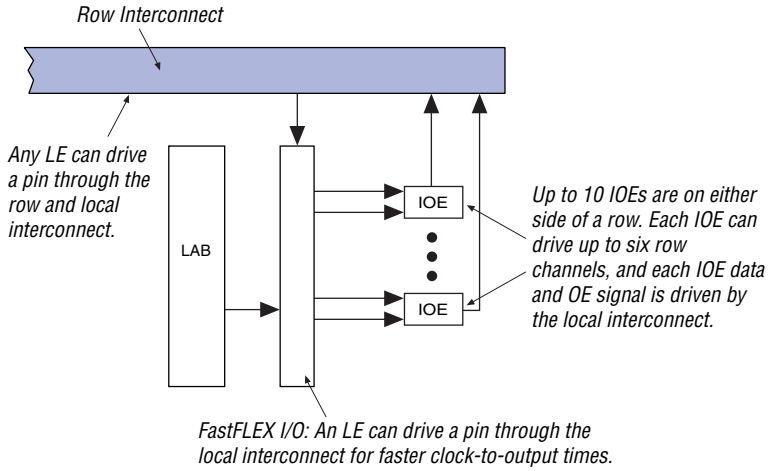
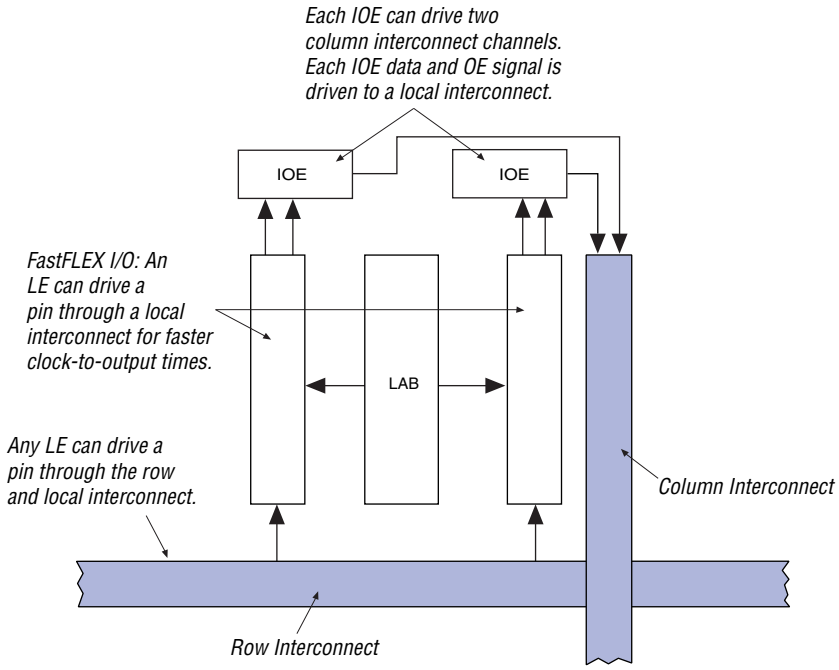


Figure 14. IOE Connection to Column Interconnect



SameFrame Pin-Outs

3.3-V FLEX 6000 devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support an EPF6016A device in a 100-pin FineLine BGA package or an EPF6024A device in a 256-pin FineLine BGA package.

The Altera software packages provide support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software packages generate pin-outs describing how to lay out a board to take advantage of this migration (see Figure 15).

Figure 15. SameFrame Pin-Out Example

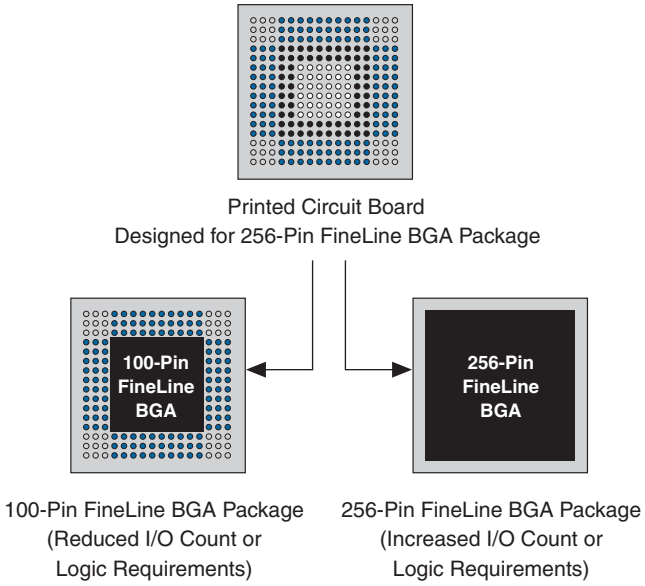


Table 6 lists the 3.3-V FLEX 6000 devices with the SameFrame pin-out feature.

Table 6. 3.3-V FLEX 6000 Devices with SameFrame Pin-Outs

Device	100-Pin FineLine BGA	256-Pin FineLine BGA
EPF6016A	v	v
EPF6024A		v

Output Configuration

This section discusses slew-rate control, the MultiVolt I/O interface, power sequencing, and hot-socketing for FLEX 6000 devices.

Slew-Rate Control

The output buffer in each IOE has an adjustable output slew-rate that can be configured for low-noise or high-speed performance. A slower slew-rate reduces system noise and adds a maximum delay of 6.8 ns. The fast slew-rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew-rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a device-wide basis. The slew-rate setting affects only the falling edge of the output.

Table 10. JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock-to-output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock-to-output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

Generic Testing

Each FLEX 6000 device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 6000 devices are made under conditions equivalent to those shown in Figure 17. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 17. AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers without parentheses are for 5.0-V devices or outputs. Numbers in parentheses are for 3.3-V devices or outputs. Numbers in brackets are for 2.5-V devices or outputs.

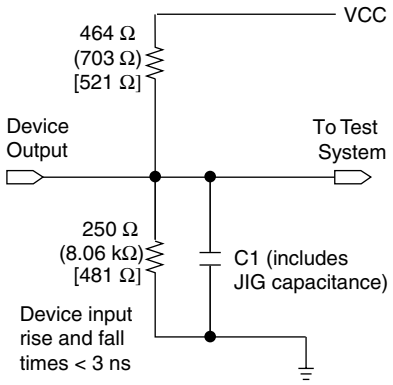


Table 13. FLEX 6000 5.0-V Device DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CCINT} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –8 mA DC, V_{CCIO} = 4.75 V *(7)*	2.4			V
	3.3-V high-level TTL output voltage	I_{OH} = –8 mA DC, V_{CCIO} = 3.00 V *(7)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(7)*	V_{CCIO} – 0.2			V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 8 mA DC, V_{CCIO} = 4.75 V *(8)*			0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 8 mA DC, V_{CCIO} = 3.00 V *(8)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(8)*			0.2	V
I_I	Input pin leakage current	V_I = V_{CC} or ground *(8)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = V_{CC} or ground *(8)*	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.5	5	mA

Table 14. FLEX 6000 5.0-V Device Capacitance *Note (9)*

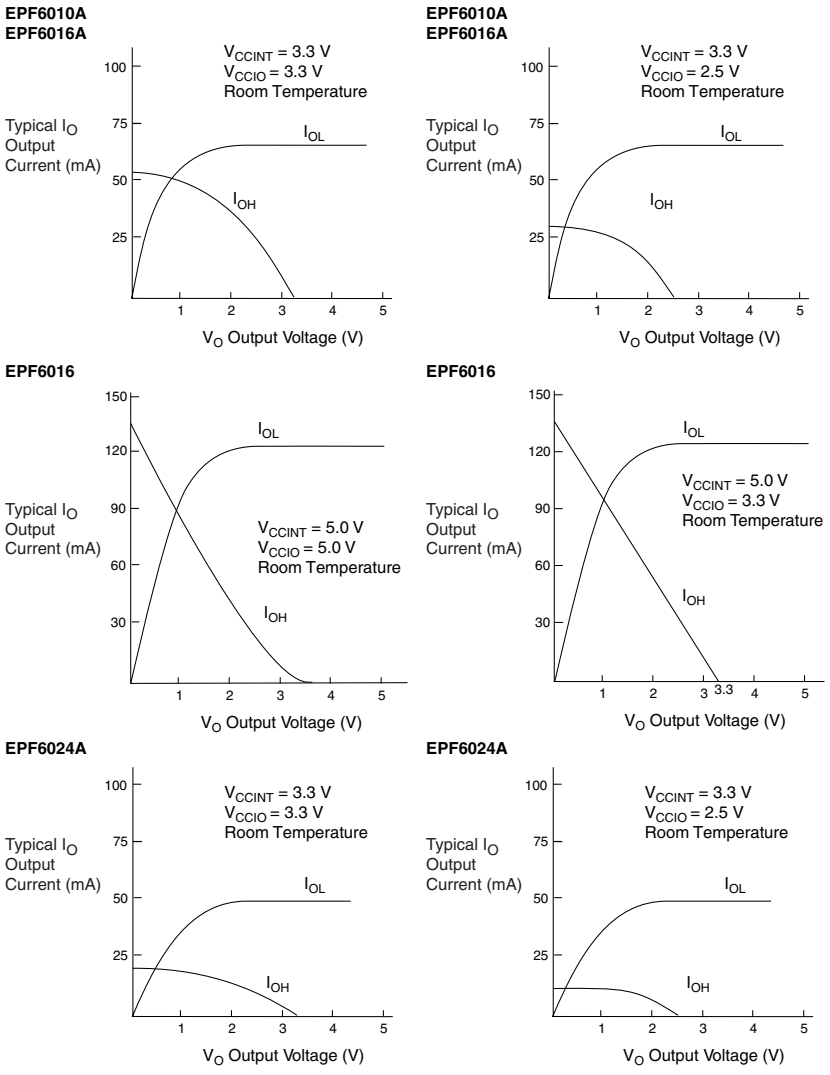
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance for I/O pin	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance for dedicated input	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time to 100 ms. V_{CC} must rise monotonically.
(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(6) These values are specified under the FLEX 6000 Recommended Operating Conditions shown in Table 12 on page 31.
(7) The I_{OH} parameter refers to high-level TTL or CMOS output current.
(8) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(9) Capacitance is sample-tested only.

Figure 18 shows the typical output drive characteristics of 5.0-V and 3.3-V FLEX 6000 devices with 5.0-V, 3.3-V, and 2.5-V V_{CCIO}. When V_{CCIO} = 5.0 V on EPF6016 devices, the output driver is compliant with the ***PCI Local Bus Specification, Revision 2.2*** for 5.0-V operation. When V_{CCIO} = 3.3 V on the EPF6010A and EPF6016A devices, the output driver is compliant with the ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation.

Figure 18. Output Drive Characteristics



Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row can be calculated by adding the following parameters:

- LE register clock-to-output delay (t_{CO} + $t_{REG\_TO\_OUT}$)
- Routing delay (t_{ROW} + t_{LOCAL})
- LE LUT delay ($t_{DATA\_TO\_REG}$)
- LE register setup time (t_{SU})

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

Timing simulation and delay prediction are available with the Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 19 shows the overall timing model, which maps the possible routing paths to and from the various elements of the FLEX 6000 device.

Figure 19. FLEX 6000 Timing Model

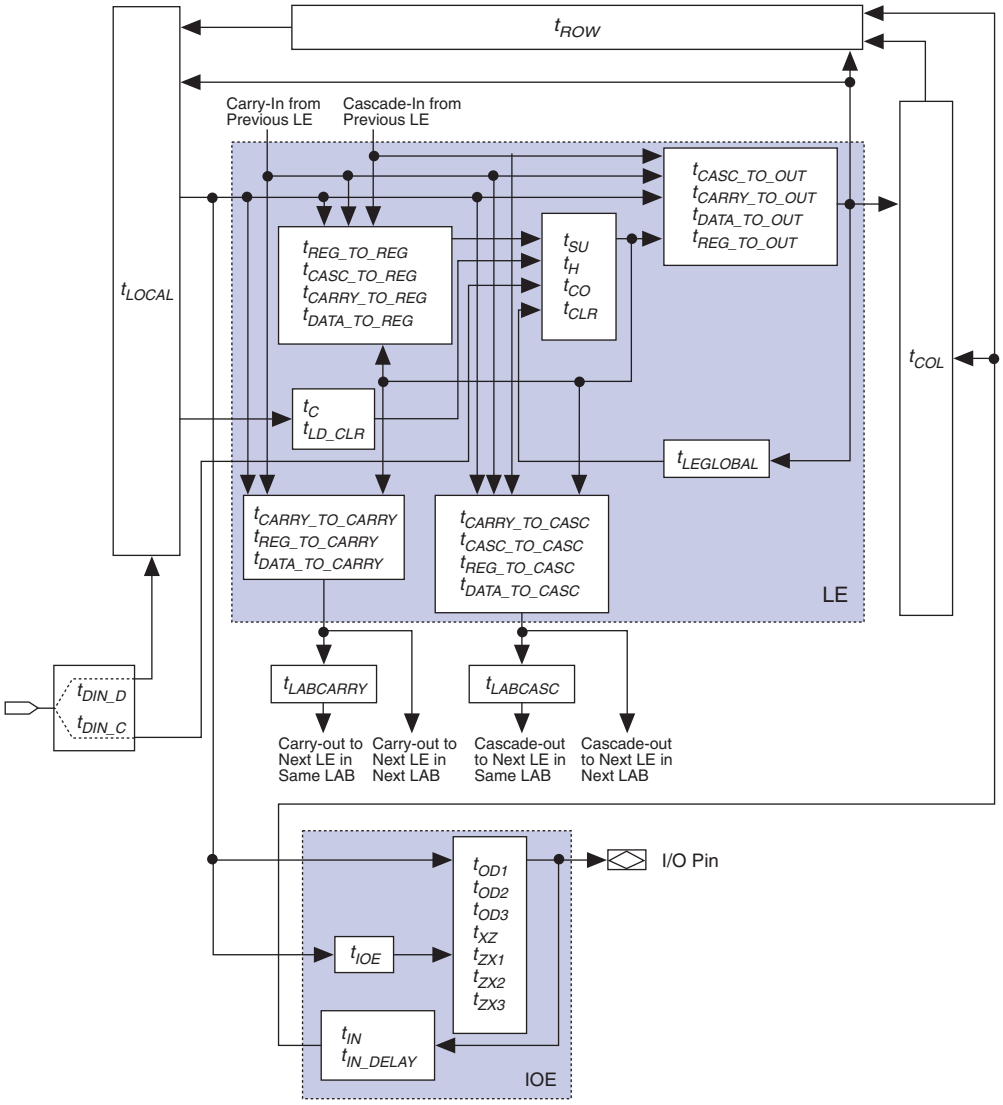


Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 2 of 2)

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{CO}		0.3		0.4		0.4	ns
t_{CLR}		0.4		0.4		0.5	ns
t_{C}		1.8		2.1		2.6	ns
t_{LD_CLR}		1.8		2.1		2.6	ns
$t_{CARRY\_TO\_CARRY}$		0.1		0.1		0.1	ns
$t_{REG\_TO\_CARRY}$		1.6		1.9		2.3	ns
$t_{DATA\_TO\_CARRY}$		2.1		2.5		3.0	ns
$t_{CARRY\_TO\_CASC}$		1.0		1.1		1.4	ns
$t_{CASC\_TO\_CASC}$		0.5		0.6		0.7	ns
$t_{REG\_TO\_CASC}$		1.4		1.7		2.1	ns
$t_{DATA\_TO\_CASC}$		1.1		1.2		1.5	ns
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

Table 25. IOE Timing Microparameters for EPF6010A & EPF6016A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{OD1}		1.9		2.2		2.7	ns
t_{OD2}		4.1		4.8		5.8	ns
t_{OD3}		5.8		6.8		8.3	ns
t_{XZ}		1.4		1.7		2.1	ns
t_{XZ1}		1.4		1.7		2.1	ns
t_{XZ2}		3.6		4.3		5.2	ns
t_{XZ3}		5.3		6.3		7.7	ns
t_{IOE}		0.5		0.6		0.7	ns
t_{IN}		3.6		4.1		5.1	ns
t_{IN_DELAY}		4.8		5.4		6.7	ns

Table 26. Interconnect Timing Microparameters for EPF6010A & EPF6016A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LOCAL}		0.7		0.7		1.0	ns
t_{ROW}		2.9		3.2		3.2	ns
t_{COL}		1.2		1.3		1.4	ns
t_{DIN_D}		5.4		5.7		6.4	ns
t_{DIN_C}		4.3		5.0		6.1	ns
$t_{LEGLOBAL}$		2.6		3.0		3.7	ns
$t_{LABCARRY}$		0.7		0.8		0.9	ns
$t_{LABCASC}$		1.3		1.4		1.8	ns

Table 27. External Reference Timing Parameters for EPF6010A & EPF6016A Devices

Parameter	Device	Speed Grade						Unit
		-1		-2		-3		
		Min	Max	Min	Max	Min	Max	
t_1	EPF6010A		37.6		43.6		53.7	ns
	EPF6016A		38.0		44.0		54.1	ns

Table 28. External Timing Parameters for EPF6010A & EPF6016A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.1 *(1)*		2.4 *(1)*		3.3 *(1)*		ns
t_{INH}	0.2 *(2)*		0.3 *(2)*		0.1 *(2)*		ns
t_{OUTCO}	2.0	7.1	2.0	8.2	2.0	10.1	ns

Notes:
(1) Setup times are longer when the *Increase Input Delay* option is turned on. The setup time values are shown with the *Increase Input Delay* option turned off.
(2) Hold time is zero when the *Increase Input Delay* option is turned on.

Table 33. External Timing Parameters for EPF6016 Devices

Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
t_{INSU}	3.2		4.1		ns
t_{INH}	0.0		0.0		ns
t_{OUTCO}	2.0	7.9	2.0	9.9	ns

Tables 34 through 38 show the timing information for EPF6024A devices.

Table 34. LE Timing Microparameters for EPF6024A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{REG\_TO\_REG}$		1.2		1.3		1.6	ns
$t_{CASC\_TO\_REG}$		0.7		0.8		1.0	ns
$t_{CARRY\_TO\_REG}$		1.6		1.8		2.2	ns
$t_{DATA\_TO\_REG}$		1.3		1.4		1.7	ns
$t_{CASC\_TO\_OUT}$		1.2		1.3		1.6	ns
$t_{CARRY\_TO\_OUT}$		2.0		2.2		2.6	ns
$t_{DATA\_TO\_OUT}$		1.8		2.1		2.6	ns
$t_{REG\_TO\_OUT}$		0.3		0.3		0.4	ns
t_{SU}	0.9		1.0		1.2		ns
t_{H}	1.3		1.4		1.7		ns
t_{CO}		0.2		0.3		0.3	ns
t_{CLR}		0.3		0.3		0.4	ns
t_{C}		1.9		2.1		2.5	ns
t_{LD_CLR}		1.9		2.1		2.5	ns
$t_{CARRY\_TO\_CARRY}$		0.2		0.2		0.3	ns
$t_{REG\_TO\_CARRY}$		1.4		1.6		1.9	ns
$t_{DATA\_TO\_CARRY}$		1.3		1.4		1.7	ns
$t_{CARRY\_TO\_CASC}$		1.1		1.2		1.4	ns
$t_{CASC\_TO\_CASC}$		0.7		0.8		1.0	ns
$t_{REG\_TO\_CASC}$		1.4		1.6		1.9	ns
$t_{DATA\_TO\_CASC}$		1.0		1.1		1.3	ns
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

Table 38. External Timing Parameters for EPF6024A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.0 *(1)*		2.2 *(1)*		2.6 *(1)*		ns
t_{INH}	0.2 *(2)*		0.2 *(2)*		0.3 *(2)*		ns
t_{OUTCO}	2.0	7.4	2.0	8.2	2.0	9.9	ns

Notes:
(1) Setup times are longer when the *Increase Input Delay* option is turned on. The setup time values are shown with the *Increase Input Delay* option turned off.
(2) Hold time is zero when the *Increase Input Delay* option is turned on.

Power Consumption

The supply power (P) for FLEX 6000 devices can be calculated with the following equations:

$$P = P_{INT} + P_{IO}$$
$$P = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in the "FLEX 6000 Device DC Operating Conditions" table on pages 31 and 33 of this data sheet. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is based on the amount of current that each LE typically consumes. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The $I_{CCACTIVE}$ value can be calculated with the following equation:

$$I_{CCACTIVE} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

Where:
$\mathbf{f_{MAX}}$ = Maximum operating frequency in MHz
N = Total number of LEs used in a FLEX 6000 device
$\mathbf{tog_{LC}}$ = Average percentage of LEs toggling at each clock (typically 12.5%)
K = Constant, shown in Table 39

Table 39. K Constant Values

Device	K Value
EPF6010A	14
EPF6016	88
EPF6016A	14
EPF6024A	14

Operating Modes

The FLEX 6000 architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. This process of physically loading the SRAM data into a FLEX 6000 device is known as configuration. During initialization—a process that occurs immediately after configuration—the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. The configuration and initialization processes of a device are referred to as *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 6000 devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and is used to dynamically reconfigure an entire system. Also, in-field system upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for a FLEX 6000 device can be loaded with one of three configuration schemes, which is chosen on the basis of the target application. An EPC1 or EPC1441 configuration device or intelligent controller can be used to control the configuration of a FLEX 6000 device, allowing automatic configuration on system power-up.

Multiple FLEX 6000 devices can be configured in any of the three configuration schemes by connecting the configuration enable input (nCE) and configuration enable output (nCEO) pins on each device.

Table 40 shows the data sources for each configuration scheme.

Table 40. Configuration Schemes

Configuration Scheme	Data Source
Configuration device	EPC1 or EPC1441 configuration device
Passive serial (PS)	BitBlaster™, ByteBlasterMV™, or MasterBlaster™ download cables, or serial data source
Passive serial asynchronous (PSA)	BitBlaster, ByteBlasterMV, or MasterBlaster download cables, or serial data source

Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* for pin-out information.

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