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Understanding [Embedded - FPGAs (Field Programmable Gate Array)](https://www.e-xfl.com)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	196
Number of Logic Elements/Cells	1960
Total RAM Bits	-
Number of I/O	199
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf6024aqc240-2

General Description

The Altera® FLEX 6000 programmable logic device (PLD) family provides a low-cost alternative to high-volume gate array designs. FLEX 6000 devices are based on the OptiFLEX architecture, which minimizes die size while maintaining high performance and routability. The devices have reconfigurable SRAM elements, which give designers the flexibility to quickly change their designs during prototyping and design testing. Designers can also change functionality during operation via in-circuit reconfiguration.

FLEX 6000 devices are reprogrammable, and they are 100% tested prior to shipment. As a result, designers are not required to generate test vectors for fault coverage purposes, allowing them to focus on simulation and design verification. In addition, the designer does not need to manage inventories of different gate array designs. FLEX 6000 devices are configured on the board for the specific functionality required.

Table 3 shows FLEX 6000 performance for some common designs. All performance values shown were obtained using Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Table 3. FLEX 6000 Device Performance for Common Designs

Application	LEs Used	Performance			Units
		-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
16-bit loadable counter	16	172	153	133	MHz
16-bit accumulator	16	172	153	133	MHz
24-bit accumulator	24	136	123	108	MHz
16-to-1 multiplexer (pin-to-pin) (1)	10	12.1	13.4	16.6	ns
16 × 16 multiplier with a 4-stage pipeline	592	84	67	58	MHz

Note:

(1)   This performance value is measured as a pin-to-pin delay.

*Figure 1. OptiFLEX Architecture Block Diagram*
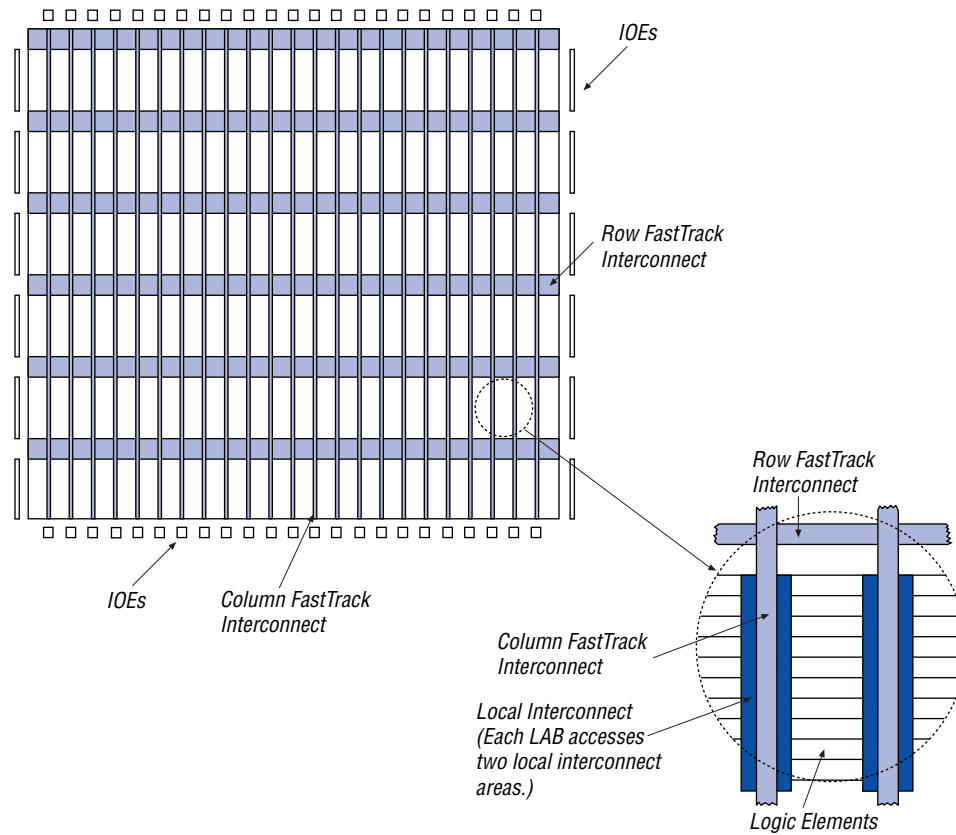
FLEX 6000 devices provide four dedicated, global inputs that drive the control inputs of the flipflops to ensure efficient distribution of high-speed, low-skew control signals. These inputs use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. These inputs can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device. The dedicated global routing structure is built into the device, eliminating the need to create a clock tree.
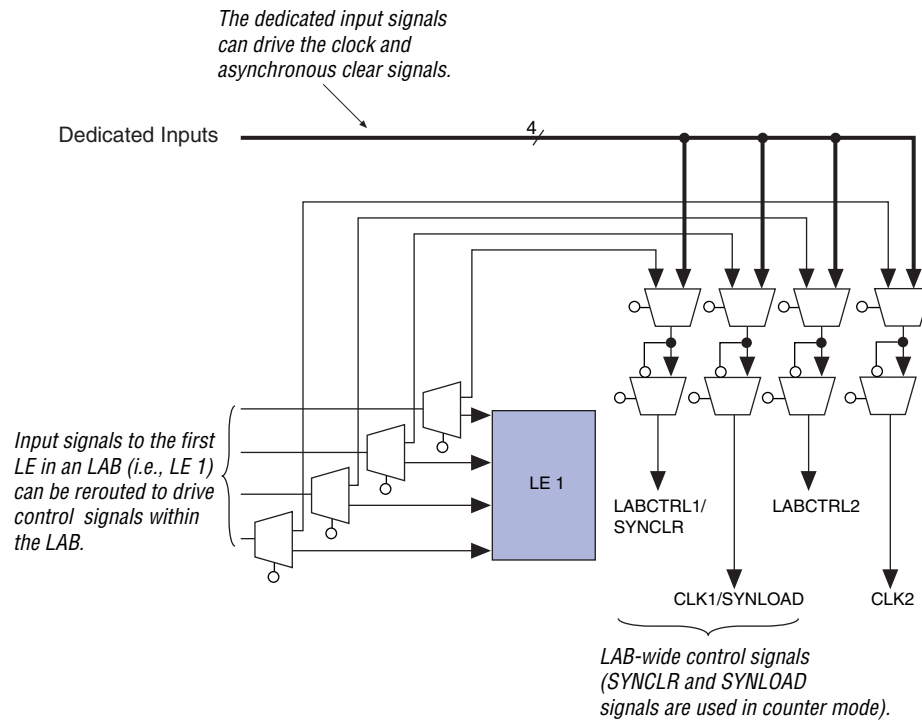
Logic Array Block

An LAB consists of ten LEs, their associated carry and cascade chains, the LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 6000 architecture, and facilitates efficient routing with optimum device utilization and high performance.

The interleaved LAB structure—an innovative feature of the FLEX 6000 architecture—allows each LAB to drive two local interconnects. This feature minimizes the use of the FastTrack Interconnect, providing higher performance. An LAB can drive 20 LEs in adjacent LABs via the local interconnect, which maximizes fitting flexibility while minimizing die size. See Figure 2.

Figure 2. Logic Array Block
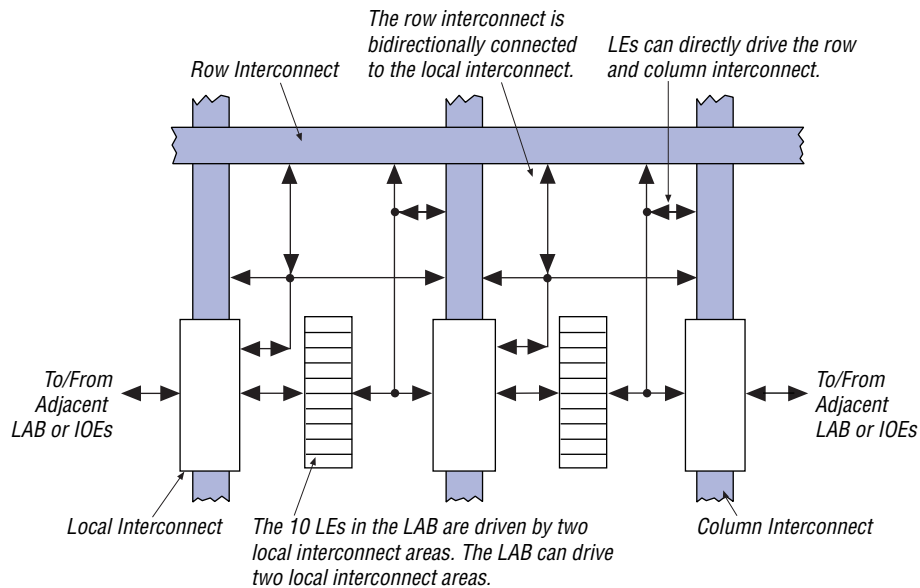
In most designs, the registers only use global clock and clear signals. However, in some cases, other clock or asynchronous clear signals are needed. In addition, counters may also have synchronous clear or load signals. In a design that uses non-global clock and clear signals, inputs from the first LE in an LAB are re-routed to drive the control signals for that LAB. See Figure 3.

Figure 3. LAB Control Signals

The dedicated input signals can drive the clock and asynchronous clear signals.

Dedicated Inputs

Input signals to the first LE in an LAB (i.e., LE 1) can be rerouted to drive control signals within the LAB.

LE 1

LABCTRL1/
SYNCLR

LABCTRL2

CLK1/SYNLOAD

CLK2

LAB-wide control signals (SYNCLR and SYNLOAD signals are used in counter mode).

Logic Element

An LE, the smallest unit of logic in the FLEX 6000 architecture, has a compact size that provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. An LE contains a programmable flipflop, carry and cascade chains. Additionally, each LE drives both the local and the FastTrack Interconnect. See Figure 4.

Cascade Chain

The cascade chain enables the FLEX 6000 architecture to implement very wide fan-in functions. Adjacent LUTs can be used to implement portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR gate (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 0.5 ns per LE. Cascade chain logic can be created automatically by the Altera software during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of cascade chains for the appropriate functions.

A cascade chain implementing an AND gate can use the register in the last LE; a cascade chain implementing an OR gate cannot use this register because of the inversion required to implement the OR gate.

Because the first LE of an LAB can generate control signals for that LAB, the first LE in each LAB is not included in cascade chains. Moreover, cascade chains longer than nine bits are automatically implemented by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from an even-numbered LAB to another even-numbered LAB, or from an odd-numbered LAB to another odd-numbered LAB. For example, the last LE of the first LAB in a row cascades to the second LE of the third LAB. The cascade chain does not cross the center of the row. For example, in an EPF6016 device, the cascade chain stops at the 11th LAB in a row and a new cascade chain begins at the 12th LAB.
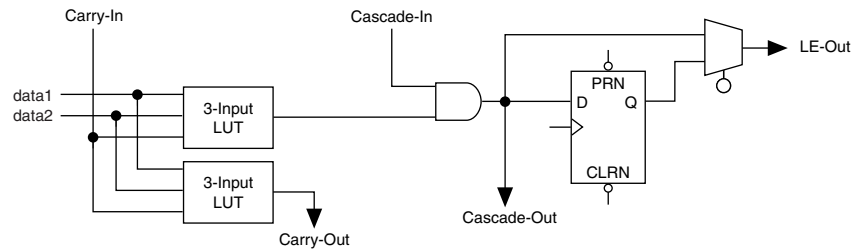
Figure 6 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. In this example, functions of $4n$ variables are implemented with n LEs. The cascade chain requires 3.4 ns to decode a 16-bit address.
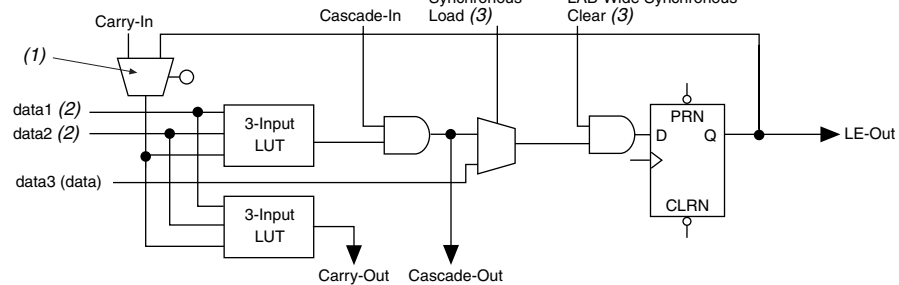
Figure 7. LE Operating Modes

Normal Mode
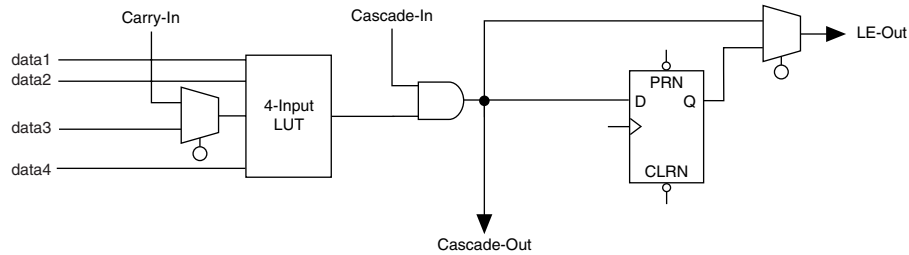
Arithmetic Mode

Counter Mode

Notes:

(1) The register feedback multiplexer is available on LE 2 of each LAB.

(2) The data1 and data2 input signals can supply a clock enable, up or down control, or register feedback signals for all LEs other than the second LE in an LAB.

(3) The LAB-wide synchronous clear and LAB-wide synchronous load affect all registers in an LAB.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The Altera software automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a 3-input function; the other generates a carry output. As shown in Figure 7, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

The Altera software implements logic functions to use the arithmetic mode automatically where appropriate; the designer does not have to decide how the carry chain will be used.

Counter Mode

The counter mode offers counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in a LAB use counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. In addition, the Altera software automatically places registers that are not in the counter into other LABs.

The counter mode uses two 3-input LUTs: one generates the counter data and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load will override any signal carried on the cascade chain. The synchronous clear overrides the synchronous load.

Either the counter enable or the up/down control may be used for a given counter. Moreover, the synchronous load can be used as a count enable by routing the register output into the data input automatically when requested by the designer.

The second LE of each LAB has a special function for counter mode; the carry-in of the LE can be driven by a fast feedback path from the register. This function gives a faster counter speed for counter carry chains starting in the second LE of an LAB.

The Altera software implements functions to use the counter mode automatically where appropriate. The designer does not have to decide how the carry chain will be used.

Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

Clear & Preset Logic Control

Logic for the programmable register's clear and preset functions is controlled by the LAB-wide signals LABCTRL1 and LABCTRL2. The LE register has an asynchronous clear that can implement an asynchronous preset. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear or preset. Because the clear and preset functions are active-low, the Altera software automatically assigns a logic high to an unused clear or preset signal. The clear and preset logic is implemented in either the asynchronous clear or asynchronous preset mode, which is chosen during design entry (see Figure 8).

Figure 8. LE Clear & Preset Modes
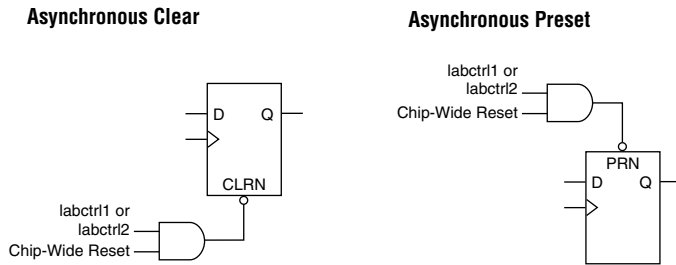
Asynchronous Clear

The flipflop can be cleared by either `LABCTRL1` or `LABCTRL2`.

Asynchronous Preset

An asynchronous preset is implemented with an asynchronous clear. The Altera software provides preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, this technique can be used when a register drives logic or drives a pin.

In addition to the two clear and preset modes, FLEX 6000 devices provide a chip-wide reset pin (`DEV_CLRn`) that can reset all registers in the device. The option to use this pin is set in the Altera software before compilation. The chip-wide reset overrides all other control signals. Any register with an asynchronous preset will be preset when the chip-wide reset is asserted because of the inversion technique used to implement the asynchronous preset.

The Altera software can use a programmable `NOT`-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses an additional three LEs per register.

FastTrack Interconnect

In the FLEX 6000 OptiFLEX architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even for complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

Figure 11. Global Clock & Clear Distribution   *Note (1)*
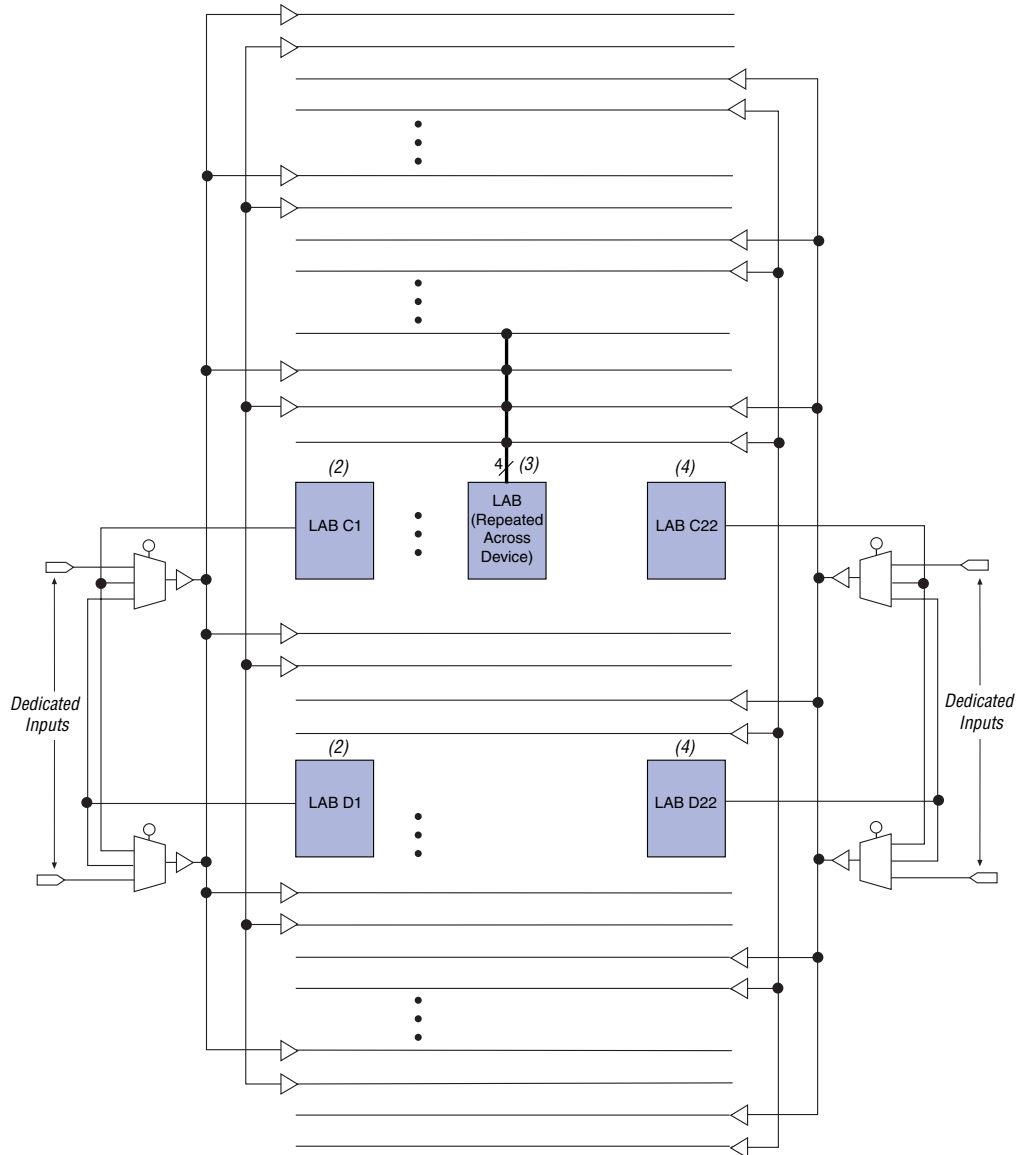
Notes:

(1) The global clock and clear distribution signals are shown for EPF6016 and EPF6016A devices. In EPF6010A devices, LABs in rows B and C drive global signals. In EPF6024A devices, LABs in rows C and E drive global signals.
(2) The local interconnect from LABs C1 and D1 can drive two global control signals on the left side.
(3) Global signals drive into every LAB as clock, asynchronous clear, preset, and data signals.
(4) The local interconnect from LABs C22 and D22 can drive two global control signals on the right side.

Each IOE drives a row or column interconnect when used as an input or bidirectional pin. A row IOE can drive up to six row lines; a column IOE can drive up to two column lines. The input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time. Figure 13 shows how an IOE connects to a row interconnect, and Figure 14 shows how an IOE connects to a column interconnect.

Figure 13. IOE Connection to Row Interconnect

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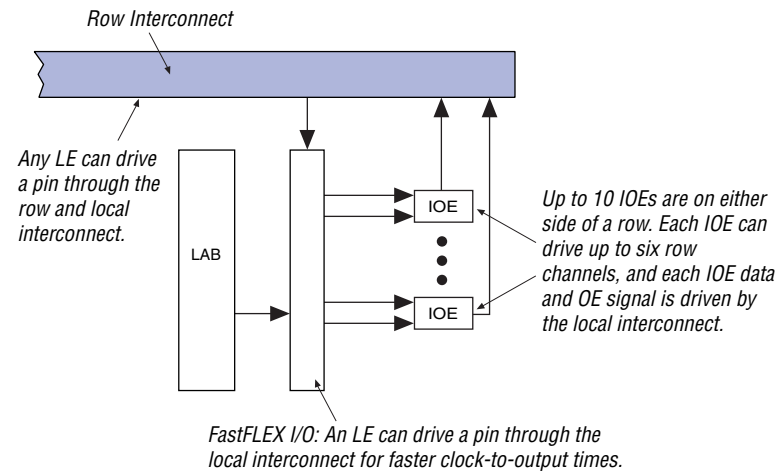
MultiVolt I/O Interface

The FLEX 6000 device architecture supports the MultiVolt I/O interface feature, which allows FLEX 6000 devices to interface with systems of differing supply voltages. The EPF6016 device can be set for 3.3-V or 5.0-V I/O pin operation. This device has one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for output drivers (VCCIO).

The VCCINT pins on 5.0-V FLEX 6000 devices must always be connected to a 5.0-V power supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The VCCIO pins on 5.0-V FLEX 6000 devices can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}.

On 3.3-V FLEX 6000 devices, the VCCINT pins must be connected to a 3.3-V power supply. Additionally, 3.3-V FLEX 6000A devices can interface with 2.5-V, 3.3-V, or 5.0-V systems when the VCCIO pins are tied to 2.5 V. The output can drive 2.5-V systems, and the inputs can be driven by 2.5-V, 3.3-V, or 5.0-V systems. When the VCCIO pins are tied to 3.3 V, the output can drive 3.3-V or 5.0-V systems. MultiVolt I/Os are not supported on 100-pin TQFP or 100-pin FineLine BGA packages.

Table 7 describes FLEX 6000 MultiVolt I/O support.

Table 7. FLEX 6000 MultiVolt I/O Support

V_{CCINT} (V)	V_{CCIO} (V)	Input Signal (V)			Output Signal (V)		
		2.5	3.3	5.0	2.5	3.3	5.0
3.3	2.5	v	v	v	v		
3.3	3.3	v	v	v	v *(1)*	v	v
5.0	3.3		v	v		v	v
5.0	5.0		v	v			v

Note:

(1)   When V_{CCIO} = 3.3 V, a FLEX 6000 device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V or 3.3-V FLEX 6000 devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Output pins on 5.0-V FLEX 6000 devices with V_{CCIO} = 3.3 V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

Power Sequencing & Hot-Socketing

Because FLEX 6000 family devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into 3.3-V FLEX 6000 devices before and during power up without damaging the device. Additionally, FLEX 6000 devices do not drive out during power up. Once operating conditions are reached, FLEX 6000 devices operate as specified by the user.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 6000 devices provide JTAG BST circuitry that comply with the IEEE Std. 1149.1-1990 specification. Table 8 shows JTAG instructions for FLEX 6000 devices. JTAG BST can be performed before or after configuration, but not during configuration (except when you disable JTAG support in user mode).

1️⃣ See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG BST circuitry.

Table 8. FLEX 6000 JTAG Instructions	
JTAG Instruction	**Description**
SAMPLE/PRELOAD	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test result at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.

Table 13. FLEX 6000 5.0-V Device DC Operating Conditions   Notes (5), (6)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CCINT} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –8 mA DC, V_{CCIO} = 4.75 V (7)	2.4			V
	3.3-V high-level TTL output voltage	I_{OH} = –8 mA DC, V_{CCIO} = 3.00 V (7)	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V (7)	V_{CCIO} – 0.2			V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 8 mA DC, V_{CCIO} = 4.75 V (8)			0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 8 mA DC, V_{CCIO} = 3.00 V (8)			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V (8)			0.2	V
I_I	Input pin leakage current	V_I = V_{CC} or ground (8)	–10		10	μA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = V_{CC} or ground (8)	–40		40	μA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.5	5	mA

Table 14. FLEX 6000 5.0-V Device Capacitance   Note (9)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance for I/O pin	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance for dedicated input	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.

(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) Numbers in parentheses are for industrial-temperature-range devices.

(4) Maximum V_{CC} rise time to 100 ms. V_{CC} must rise monotonically.

(5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.

(6) These values are specified under the FLEX 6000 Recommended Operating Conditions shown in Table 12 on page 31.

(7) The I_{OH} parameter refers to high-level TTL or CMOS output current.

(8) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.

(9) Capacitance is sample-tested only.

Table 15. FLEX 6000 3.3-V Device Absolute Maximum Ratings   Note (1)

Symbol	Parameter	Conditions	Min	Max	Unit
V$_{CC}$	Supply voltage	With respect to ground (2)	−0.5	4.6	V
V$_I$	DC input voltage		−2.0	5.75	V
I$_{OUT}$	DC output current, per pin		−25	25	mA
T$_{STG}$	Storage temperature	No bias	−65	150	° C
T$_{AMB}$	Ambient temperature	Under bias	−65	135	° C
T$_J$	Junction temperature	PQFP, PLCC, and BGA packages		135	° C

Table 16. FLEX 6000 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V$_{CCINT}$	Supply voltage for internal logic and input buffers	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
V$_{CCIO}$	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.30 (2.30)	2.70 (2.70)	V
V$_I$	Input voltage		−0.5	5.75	V
V$_O$	Output voltage		0	V$_{CCIO}$	V
T$_J$	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
t$_R$	Input rise time			40	ns
t$_F$	Input fall time			40	ns

Table 20. IOE Timing Microparameters   *Note (1)*

Symbol	Parameter	Conditions
t_{OD1}	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF *(2)*
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF *(3)*
t_{OD3}	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF *(4)*
t_{XZ}	Output buffer disable delay	C1 = 5 pF
t_{ZX1}	Output buffer enable delay, slow slew rate = off, $V_{CCIO} = V_{CCINT}$	C1 = 35 pF *(2)*
t_{ZX2}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = low voltage	C1 = 35 pF *(3)*
t_{ZX3}	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF *(4)*
t_{IOE}	Output enable control delay	
t_{IN}	Input pad and buffer to FastTrack Interconnect delay	
t_{IN_DELAY}	Input pad and buffer to FastTrack Interconnect delay with additional delay turned on	

Table 21. Interconnect Timing Microparameters   *Note (1)*

Symbol	Parameter	Conditions
t_{LOCAL}	LAB local interconnect delay	
t_{ROW}	Row interconnect routing delay	*(5)*
t_{COL}	Column interconnect routing delay	*(5)*
t_{DIN_D}	Dedicated input to LE data delay	*(5)*
t_{DIN_C}	Dedicated input to LE control delay	
$t_{LEGLOBAL}$	LE output to LE control via internally-generated global signal delay	*(5)*
$t_{LABCARRY}$	Routing delay for the carry-out of an LE driving the carry-in signal of a different LE in a different LAB	
$t_{LABCASC}$	Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB	

Table 22. External Reference Timing Parameters

Symbol	Parameter	Conditions
t_1	Register-to-register test pattern	*(6)*
t_{DRR}	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects	*(7)*

Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices   (Part 2 of 2)

Parameter	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	Max	Min	Max	Min	Max	
t_{CO}		0.3		0.4		0.4	ns
t_{CLR}		0.4		0.4		0.5	ns
t_C		1.8		2.1		2.6	ns
t_{LD_CLR}		1.8		2.1		2.6	ns
$t_{CARRY\_TO\_CARRY}$		0.1		0.1		0.1	ns
$t_{REG\_TO\_CARRY}$		1.6		1.9		2.3	ns
$t_{DATA\_TO\_CARRY}$		2.1		2.5		3.0	ns
$t_{CARRY\_TO\_CASC}$		1.0		1.1		1.4	ns
$t_{CASC\_TO\_CASC}$		0.5		0.6		0.7	ns
$t_{REG\_TO\_CASC}$		1.4		1.7		2.1	ns
$t_{DATA\_TO\_CASC}$		1.1		1.2		1.5	ns
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

Table 25. IOE Timing Microparameters for EPF6010A & EPF6016A Devices

Parameter	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	Max	Min	Max	Min	Max	
t_{OD1}		1.9		2.2		2.7	ns
t_{OD2}		4.1		4.8		5.8	ns
t_{OD3}		5.8		6.8		8.3	ns
t_{XZ}		1.4		1.7		2.1	ns
t_{XZ1}		1.4		1.7		2.1	ns
t_{XZ2}		3.6		4.3		5.2	ns
t_{XZ3}		5.3		6.3		7.7	ns
t_{IOE}		0.5		0.6		0.7	ns
t_{IN}		3.6		4.1		5.1	ns
t_{IN_DELAY}		4.8		5.4		6.7	ns

Table 26. Interconnect Timing Microparameters for EPF6010A & EPF6016A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{LOCAL}		0.7		0.7		1.0	ns
t_{ROW}		2.9		3.2		3.2	ns
t_{COL}		1.2		1.3		1.4	ns
t_{DIN_D}		5.4		5.7		6.4	ns
t_{DIN_C}		4.3		5.0		6.1	ns
$t_{LEGLOBAL}$		2.6		3.0		3.7	ns
$t_{LABCARRY}$		0.7		0.8		0.9	ns
$t_{LABCASC}$		1.3		1.4		1.8	ns

Table 27. External Reference Timing Parameters for EPF6010A & EPF6016A Devices

Parameter	Device	Speed Grade						Unit
		-1		-2		-3		
		Min	Max	Min	Max	Min	Max	
t_1	EPF6010A		37.6		43.6		53.7	ns
	EPF6016A		38.0		44.0		54.1	ns

Table 28. External Timing Parameters for EPF6010A & EPF6016A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.1 *(1)*		2.4 *(1)*		3.3 *(1)*		ns
t_{INH}	0.2 *(2)*		0.3 *(2)*		0.1 *(2)*		ns
t_{OUTCO}	2.0	7.1	2.0	8.2	2.0	10.1	ns

Notes:

(1) Setup times are longer when the *Increase Input Delay* option is turned on. The setup time values are shown with the *Increase Input Delay* option turned off.

(2) Hold time is zero when the *Increase Input Delay* option is turned on.

Table 38. External Timing Parameters for EPF6024A Devices

Parameter	Speed Grade						Unit
	-1		**-2**		**-3**		
	Min	Max	Min	Max	Min	Max	
t$_{INSU}$	2.0 *(1)*		2.2 *(1)*		2.6 *(1)*		ns
t$_{INH}$	0.2 *(2)*		0.2 *(2)*		0.3 *(2)*		ns
t$_{OUTCO}$	2.0	7.4	2.0	8.2	2.0	9.9	ns

Notes:
(1) Setup times are longer when the *Increase Input Delay* option is turned on. The setup time values are shown with the *Increase Input Delay* option turned off.
(2) Hold time is zero when the *Increase Input Delay* option is turned on.

Power Consumption

The supply power (P) for FLEX 6000 devices can be calculated with the following equations:

$$P = P_{INT} + P_{IO}$$
$$P = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

Typical I$_{CCSTANDBY}$ values are shown as I$_{CC0}$ in the "FLEX 6000 Device DC Operating Conditions" table on of this data sheet. The I$_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is based on the amount of current that each LE typically consumes. The P$_{IO}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The I$_{CCACTIVE}$ value can be calculated with the following equation:

$$I_{CCACTIVE} = K \times f_{MAX} \times N \times tog_{LC} \times \frac{\mu A}{MHz \times LE}$$

Where:

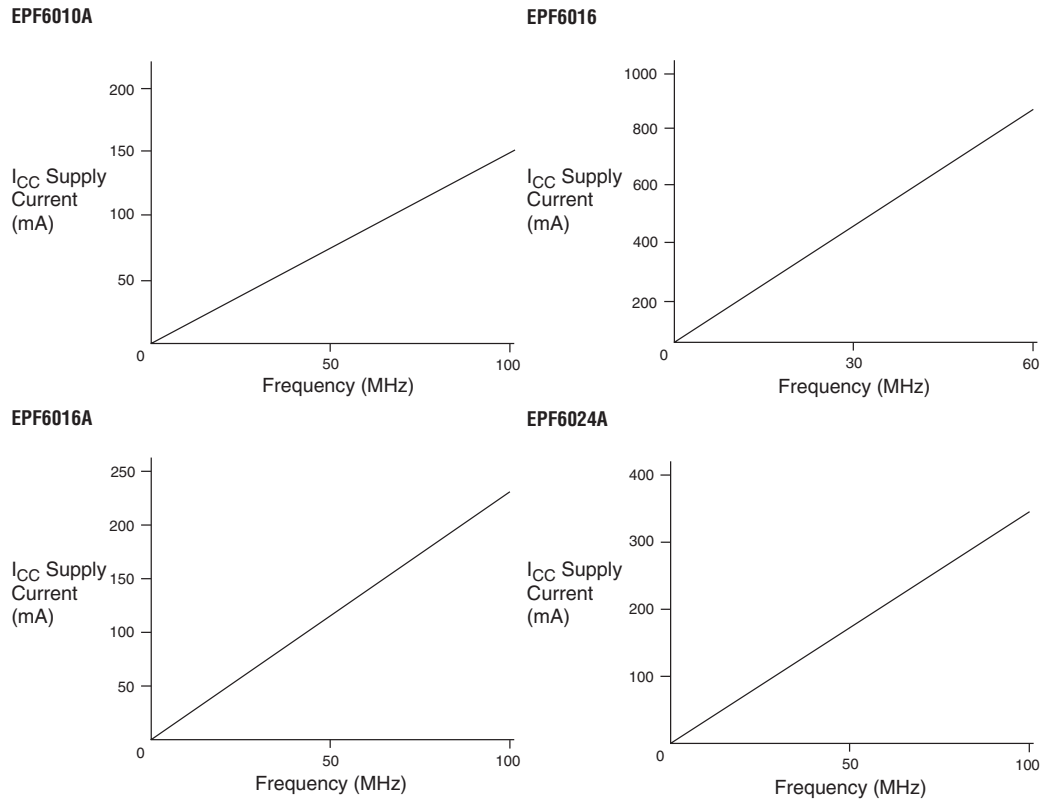|		
f$_{MAX}$	=	Maximum operating frequency in MHz
N	=	Total number of LEs used in a FLEX 6000 device
tog$_{LC}$	=	Average percentage of LEs toggling at each clock (typically 12.5%)
K	=	Constant, shown in Table 39

Table 39. K Constant Values

Device	K Value
EPF6010A	14
EPF6016	88
EPF6016A	14
EPF6024A	14

Figure 20. $I_{CCACTIVE}$ vs. Operating Frequency

EPF6010A

EPF6016

EPF6016A

EPF6024A

Device Configuration & Operation

The FLEX 6000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.