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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	196
Number of Logic Elements/Cells	1960
Total RAM Bits	-
Number of I/O	171
Number of Gates	24000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf6024aqi208-3

…and More Features

- Powerful I/O pins
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Fast path from register to I/O pin for fast clock-to-output time
- Flexible interconnect
  - FastTrack® Interconnect continuous routing structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Tri-state emulation that implements internal tri-state networks
  - Four low-skew global paths for clock, clear, preset, or logic signals
- Software design support and automatic place-and-route provided by Altera's development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800
- Flexible package options
  - Available in a variety of packages with 100 to 256 pins, including the innovative FineLine BGA™ packages (see Table 2)
  - SameFrame™ pin-compatibility (with other FLEX® 6000 devices) across device densities and pin counts
  - Thin quad flat pack (TQFP), plastic quad flat pack (PQFP), and ball-grid array (BGA) packages (see Table 2)
  - Footprint- and pin-compatibility with other FLEX 6000 devices in the same package
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, the library of parameterized modules (LPM), Verilog HDL, VHDL, DesignWare components, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Table 2. FLEX 6000 Package Options & I/O Pin Count

Device	100-Pin TQFP	100-Pin FineLine BGA	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin BGA	256-pin FineLine BGA
EPF6010A	71		102				
EPF6016			117	171	199	204	
EPF6016A	81	81	117	171			171
EPF6024A			117	171	199	218	219

Table 4 shows FLEX 6000 performance for more complex designs.

Table 4. FLEX 6000 Device Performance for Complex Designs *Note (1)*

Application	LEs Used	Performance			Units
		-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
8-bit, 16-tap parallel finite impulse response (FIR) filter	599	94	80	72	MSPS
8-bit, 512-point fast Fourier transform (FFT) function	1,182	75 63	89 53	109 43	µS MHz
a16450 universal asynchronous receiver/transmitter (UART)	487	36	30	25	MHz
PCI bus target with zero wait states	609	56	49	42	MHz

Note:
(1) The applications in this table were created using Altera MegaCore™ functions.

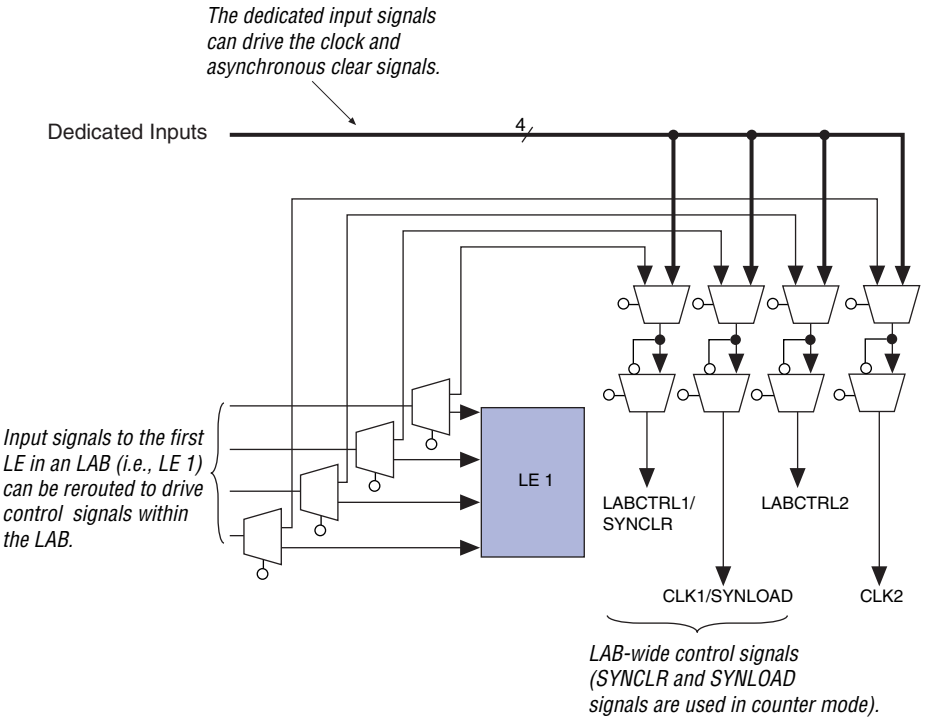
FLEX 6000 devices are supported by Altera development systems; a single, integrated package that offers schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development systems include DesignWare functions that are optimized for the FLEX 6000 architecture.

The Altera development system runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800.

f See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet* for more information.

Figure 3. LAB Control Signals



Logic Element

An LE, the smallest unit of logic in the FLEX 6000 architecture, has a compact size that provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. An LE contains a programmable flipflop, carry and cascade chains. Additionally, each LE drives both the local and the FastTrack Interconnect. See Figure 4.

Figure 5. Carry Chain Operation

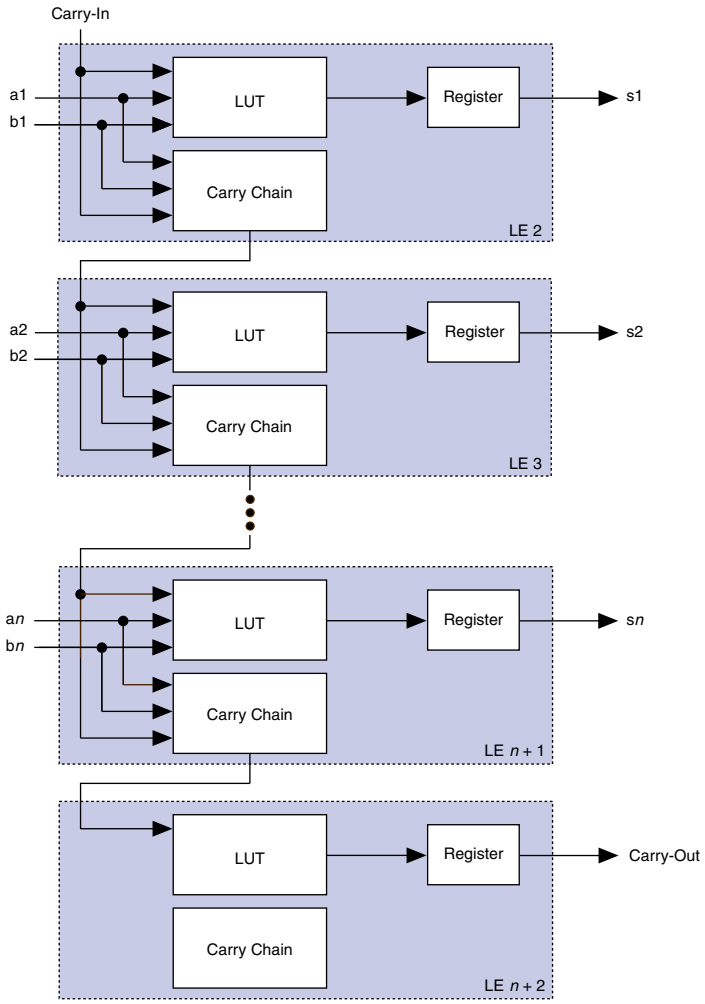
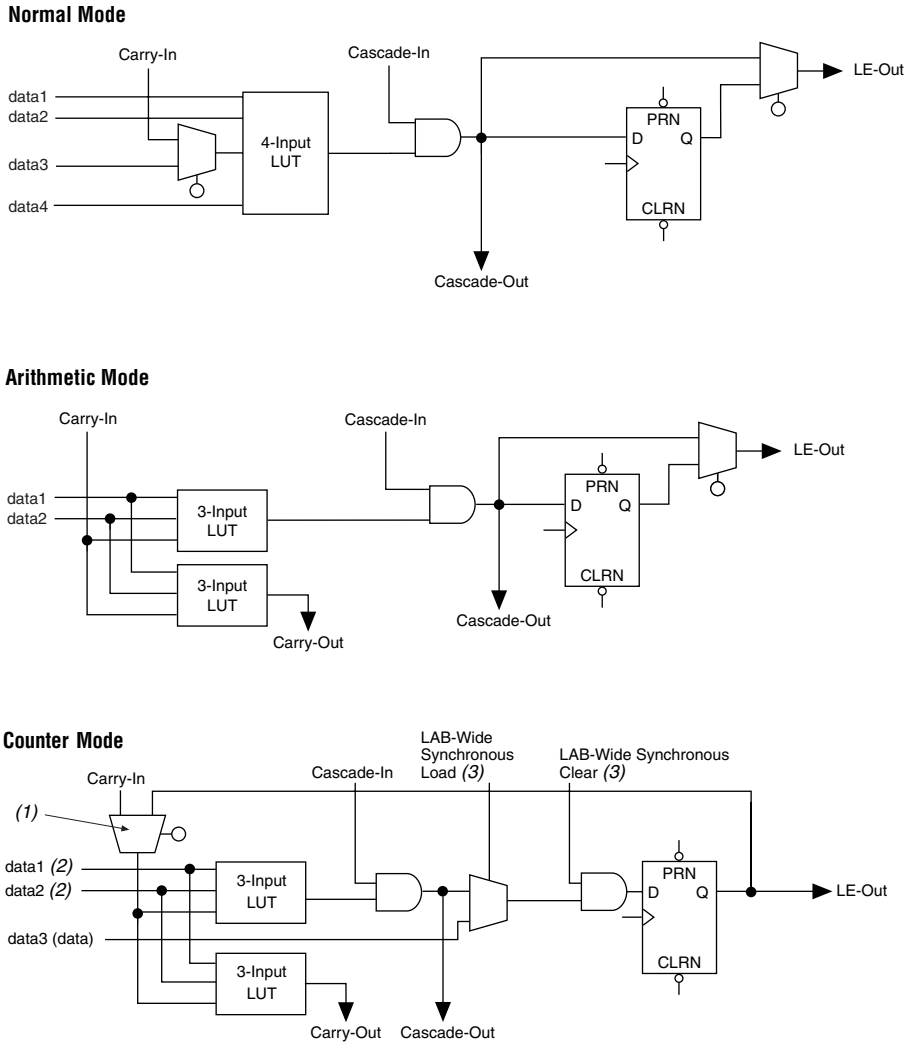


Figure 7. LE Operating Modes



Notes:

(1) The register feedback multiplexer is available on LE 2 of each LAB.

(2) The `data1` and `data2` input signals can supply a clock enable, up or down control, or register feedback signals for all LEs other than the second LE in an LAB.

(3) The LAB-wide synchronous clear and LAB-wide synchronous load affect all registers in an LAB.

Either the counter enable or the up/down control may be used for a given counter. Moreover, the synchronous load can be used as a count enable by routing the register output into the data input automatically when requested by the designer.

The second LE of each LAB has a special function for counter mode; the carry-in of the LE can be driven by a fast feedback path from the register. This function gives a faster counter speed for counter carry chains starting in the second LE of an LAB.

The Altera software implements functions to use the counter mode automatically where appropriate. The designer does not have to decide how the carry chain will be used.

Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

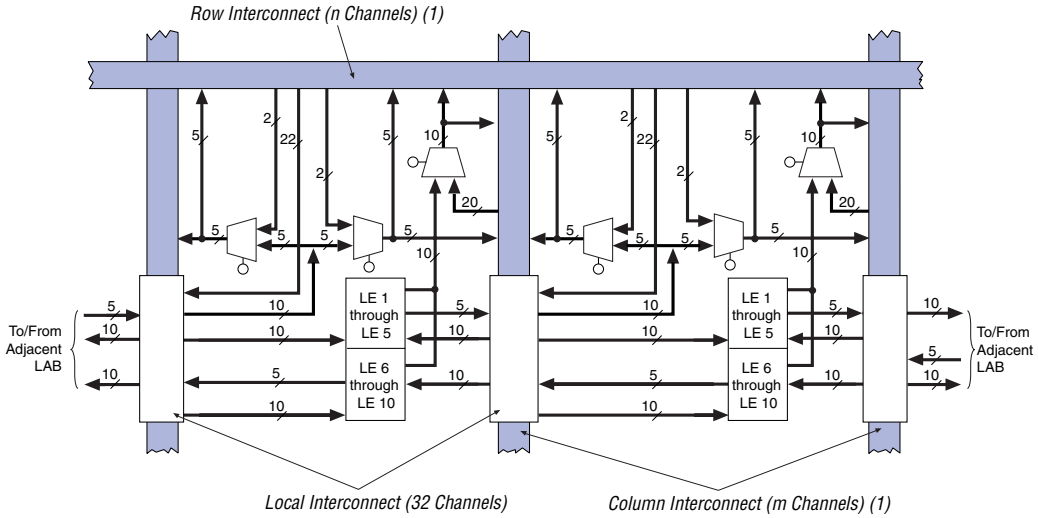
Clear & Preset Logic Control

Logic for the programmable register's clear and preset functions is controlled by the LAB-wide signals `LABCTRL1` and `LABCTRL2`. The LE register has an asynchronous clear that can implement an asynchronous preset. Either `LABCTRL1` or `LABCTRL2` can control the asynchronous clear or preset. Because the clear and preset functions are active-low, the Altera software automatically assigns a logic high to an unused clear or preset signal. The clear and preset logic is implemented in either the asynchronous clear or asynchronous preset mode, which is chosen during design entry (see Figure 8).

The FastTrack Interconnect consists of column and row interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect, which routes signals between LABs in the same row, and also routes signals from I/O pins to LABs. Additionally, the local interconnect routes signals between LEs in the same LAB and in adjacent LABs. The column interconnect routes signals between rows and routes signals from I/O pins to rows.

LEs 1 through 5 of an LAB drive the local interconnect to the right, while LEs 6 through 10 drive the local interconnect to the left. The `DATA1` and `DATA3` inputs of each LE are driven by the local interconnect to the left; `DATA2` and `DATA4` are driven by the local interconnect to the right. The local interconnect also routes signals from LEs to I/O pins. Figure 9 shows an overview of the FLEX 6000 interconnect architecture. LEs in the first and last columns have drivers on both sides so that all LEs in the LAB can drive I/O pins via the local interconnect.

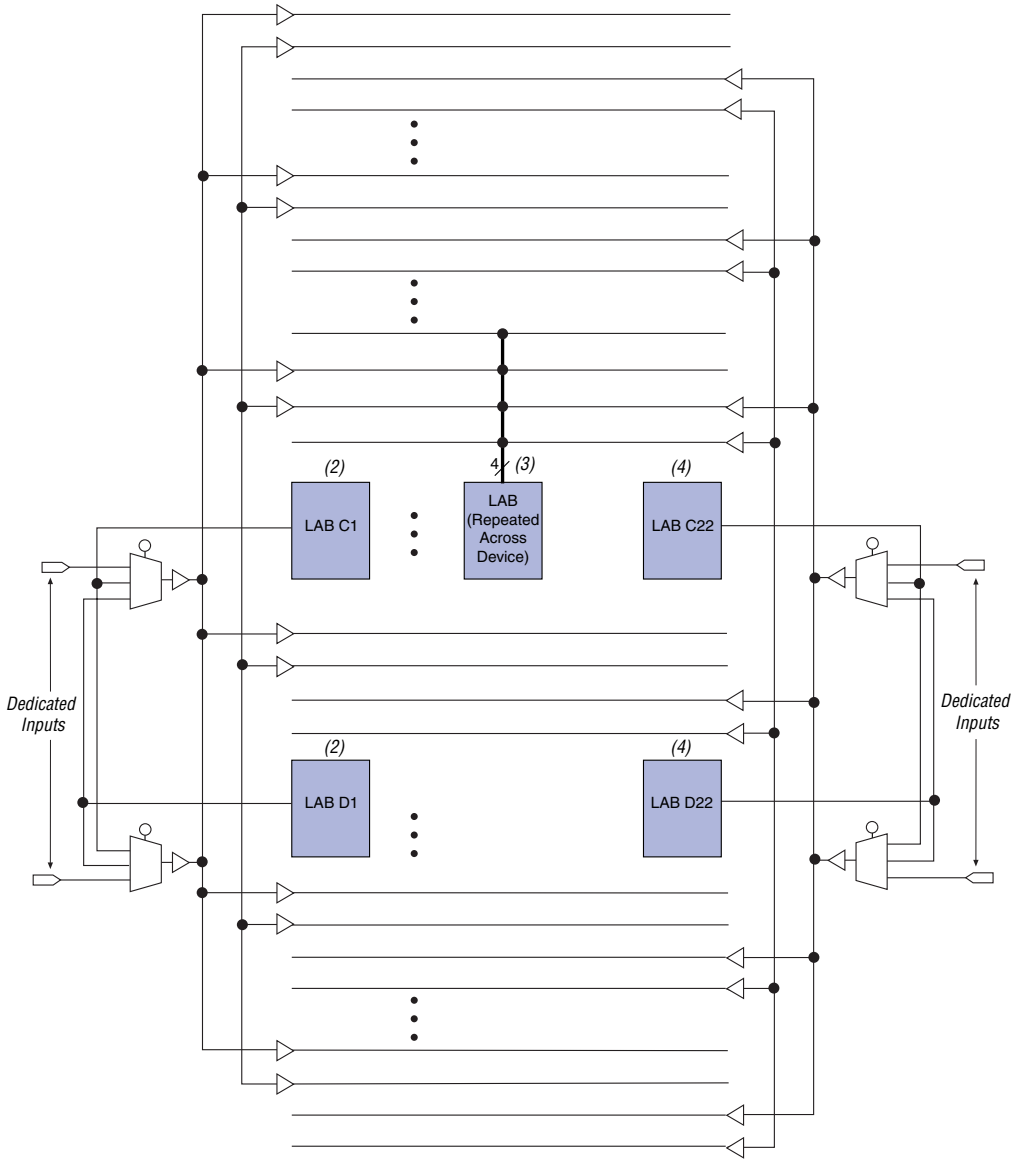
Figure 9. FastTrack Interconnect Architecture



Note:

(1) For EPF6010A, EPF6016, and EPF6016A devices, n = 144 channels and m = 20 channels; for EPF6024A devices, n = 186 channels and m = 30 channels.

Figure 11. Global Clock & Clear Distribution *Note (1)*



Notes:

(1) The global clock and clear distribution signals are shown for EPF6016 and EPF6016A devices. In EPF6010A devices, LABs in rows B and C drive global signals. In EPF6024A devices, LABs in rows C and E drive global signals.
(2) The local interconnect from LABs C1 and D1 can drive two global control signals on the left side.
(3) Global signals drive into every LAB as clock, asynchronous clear, preset, and data signals.
(4) The local interconnect from LABs C22 and D22 can drive two global control signals on the right side.

Figure 15. SameFrame Pin-Out Example

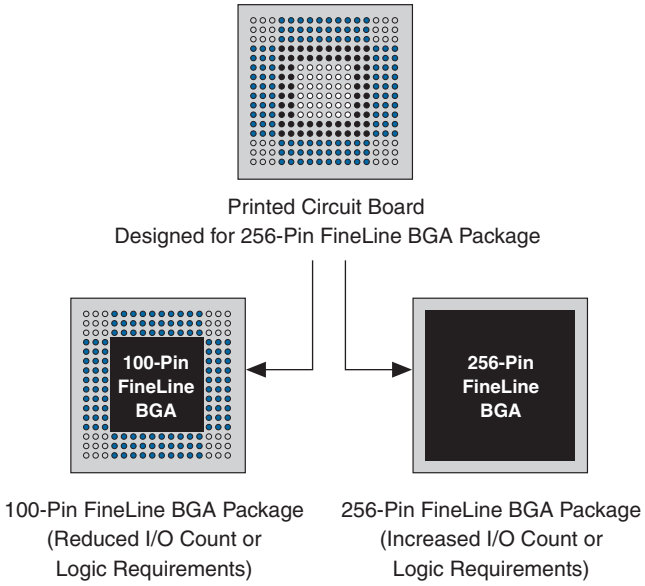


Table 6 lists the 3.3-V FLEX 6000 devices with the SameFrame pin-out feature.

Table 6. 3.3-V FLEX 6000 Devices with SameFrame Pin-Outs

Device	100-Pin FineLine BGA	256-Pin FineLine BGA
EPF6016A	v	v
EPF6024A		v

Output Configuration

This section discusses slew-rate control, the MultiVolt I/O interface, power sequencing, and hot-socketing for FLEX 6000 devices.

Slew-Rate Control

The output buffer in each IOE has an adjustable output slew-rate that can be configured for low-noise or high-speed performance. A slower slew-rate reduces system noise and adds a maximum delay of 6.8 ns. The fast slew-rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew-rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a device-wide basis. The slew-rate setting affects only the falling edge of the output.

MultiVolt I/O Interface

The FLEX 6000 device architecture supports the MultiVolt I/O interface feature, which allows FLEX 6000 devices to interface with systems of differing supply voltages. The EPF6016 device can be set for 3.3-V or 5.0-V I/O pin operation. This device has one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for output drivers (VCCIO).

The VCCINT pins on 5.0-V FLEX 6000 devices must always be connected to a 5.0-V power supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The VCCIO pins on 5.0-V FLEX 6000 devices can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}.

On 3.3-V FLEX 6000 devices, the VCCINT pins must be connected to a 3.3-V power supply. Additionally, 3.3-V FLEX 6000A devices can interface with 2.5-V, 3.3-V, or 5.0-V systems when the VCCIO pins are tied to 2.5 V. The output can drive 2.5-V systems, and the inputs can be driven by 2.5-V, 3.3-V, or 5.0-V systems. When the VCCIO pins are tied to 3.3 V, the output can drive 3.3-V or 5.0-V systems. MultiVolt I/Os are not supported on 100-pin TQFP or 100-pin FineLine BGA packages.

Table 7 describes FLEX 6000 MultiVolt I/O support.

Table 7. FLEX 6000 MultiVolt I/O Support

V_{CCINT} (V)	V_{CCIO} (V)	Input Signal (V)			Output Signal (V)		
		2.5	3.3	5.0	2.5	3.3	5.0
3.3	2.5	v	v	v	v		
3.3	3.3	v	v	v	v *(1)*	v	v
5.0	3.3		v	v		v	v
5.0	5.0		v	v			v

Note:

(1) When V_{CCIO} = 3.3 V, a FLEX 6000 device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V or 3.3-V FLEX 6000 devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Output pins on 5.0-V FLEX 6000 devices with V_{CCIO} = 3.3 V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

Power Sequencing & Hot-Socketing

Because FLEX 6000 family devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into 3.3-V FLEX 6000 devices before and during power up without damaging the device. Additionally, FLEX 6000 devices do not drive out during power up. Once operating conditions are reached, FLEX 6000 devices operate as specified by the user.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 6000 devices provide JTAG BST circuitry that comply with the IEEE Std. 1149.1-1990 specification. Table 8 shows JTAG instructions for FLEX 6000 devices. JTAG BST can be performed before or after configuration, but not during configuration (except when you disable JTAG support in user mode).

1 See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG BST circuitry.

Table 8. FLEX 6000 JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test result at the input pins.
BYPASS	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.

The instruction register length for FLEX 6000 devices is three bits. Table 9 shows the boundary-scan register length for FLEX 6000 devices.

Table 9. FLEX 6000 Device Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPF6010A	522
EPF6016	621
EPF6016A	522
EPF6024A	666

FLEX 6000 devices include a weak pull-up on JTAG pins.

f See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information.

Figure 16 shows the timing requirements for the JTAG signals.

Figure 16. JTAG Waveforms

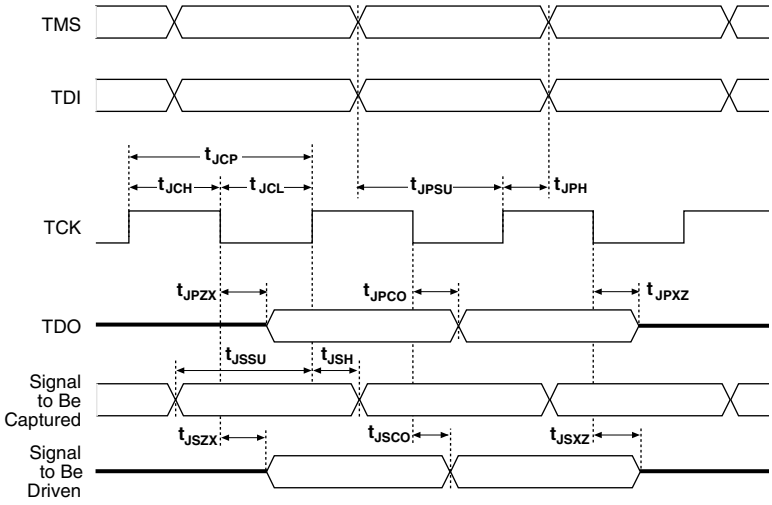


Table 10 shows the JTAG timing parameters and values for FLEX 6000 devices.

Table 15. FLEX 6000 3.3-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–0.5	4.6	V
V_I	DC input voltage		–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, PLCC, and BGA packages		135	° C

Table 16. FLEX 6000 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.30 (2.30)	2.70 (2.70)	V
V_I	Input voltage		–0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row can be calculated by adding the following parameters:

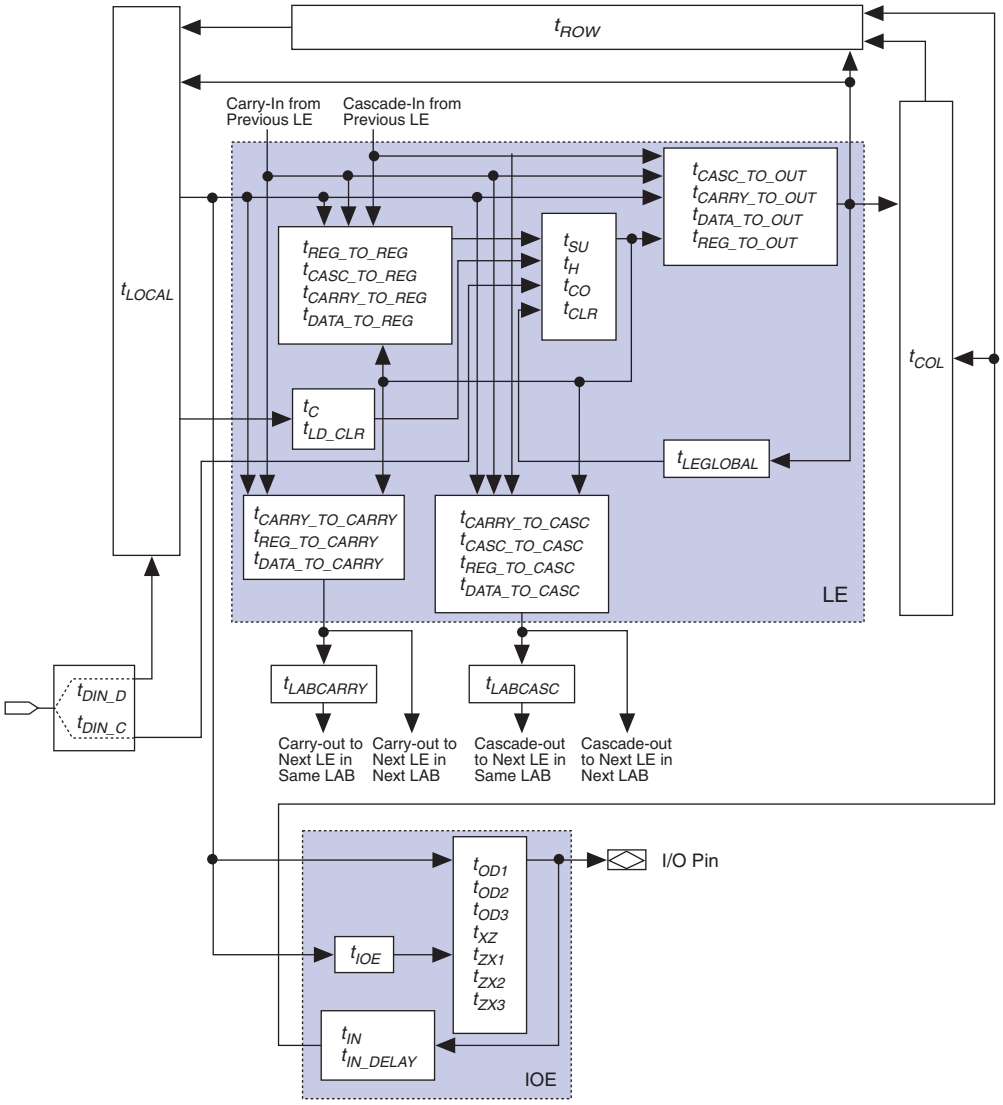
- LE register clock-to-output delay (t_{CO} + $t_{REG\_TO\_OUT}$)
- Routing delay (t_{ROW} + t_{LOCAL})
- LE LUT delay ($t_{DATA\_TO\_REG}$)
- LE register setup time (t_{SU})

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

Timing simulation and delay prediction are available with the Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 19 shows the overall timing model, which maps the possible routing paths to and from the various elements of the FLEX 6000 device.

Figure 19. FLEX 6000 Timing Model



Tables 19 through 21 describe the FLEX 6000 internal timing microparameters, which are expressed as worst-case values. Using hand calculations, these parameters can be used to estimate design performance. However, before committing designs to silicon, actual worst-case performance should be modeled using timing simulation and timing analysis. Tables 22 and 23 describe FLEX 6000 external timing parameters.

Table 19. LE Timing Microparameters *Note (1)*

Symbol	Parameter	Conditions
$t_{REG\_TO\_REG}$	LUT delay for LE register feedback in carry chain	
$t_{CASC\_TO\_REG}$	Cascade-in to register delay	
$t_{CARRY\_TO\_REG}$	Carry-in to register delay	
$t_{DATA\_TO\_REG}$	LE input to register delay	
$t_{CASC\_TO\_OUT}$	Cascade-in to LE output delay	
$t_{CARRY\_TO\_OUT}$	Carry-in to LE output delay	
$t_{DATA\_TO\_OUT}$	LE input to LE output delay	
$t_{REG\_TO\_OUT}$	Register output to LE output delay	
t_{SU}	LE register setup time before clock; LE register recovery time after asynchronous clear	
t_{H}	LE register hold time after clock	
t_{CO}	LE register clock-to-output delay	
t_{CLR}	LE register clear delay	
t_{C}	LE register control signal delay	
t_{LD_CLR}	Synchronous load or clear delay in counter mode	
$t_{CARRY\_TO\_CARRY}$	Carry-in to carry-out delay	
$t_{REG\_TO\_CARRY}$	Register output to carry-out delay	
$t_{DATA\_TO\_CARRY}$	LE input to carry-out delay	
$t_{CARRY\_TO\_CASC}$	Carry-in to cascade-out delay	
$t_{CASC\_TO\_CASC}$	Cascade-in to cascade-out delay	
$t_{REG\_TO\_CASC}$	Register-out to cascade-out delay	
$t_{DATA\_TO\_CASC}$	LE input to cascade-out delay	
t_{CH}	LE register clock high time	
t_{CL}	LE register clock low time	

Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 2 of 2)

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{CO}		0.3		0.4		0.4	ns
t_{CLR}		0.4		0.4		0.5	ns
t_{C}		1.8		2.1		2.6	ns
t_{LD_CLR}		1.8		2.1		2.6	ns
$t_{CARRY\_TO\_CARRY}$		0.1		0.1		0.1	ns
$t_{REG\_TO\_CARRY}$		1.6		1.9		2.3	ns
$t_{DATA\_TO\_CARRY}$		2.1		2.5		3.0	ns
$t_{CARRY\_TO\_CASC}$		1.0		1.1		1.4	ns
$t_{CASC\_TO\_CASC}$		0.5		0.6		0.7	ns
$t_{REG\_TO\_CASC}$		1.4		1.7		2.1	ns
$t_{DATA\_TO\_CASC}$		1.1		1.2		1.5	ns
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

Table 25. IOE Timing Microparameters for EPF6010A & EPF6016A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{OD1}		1.9		2.2		2.7	ns
t_{OD2}		4.1		4.8		5.8	ns
t_{OD3}		5.8		6.8		8.3	ns
t_{XZ}		1.4		1.7		2.1	ns
t_{XZ1}		1.4		1.7		2.1	ns
t_{XZ2}		3.6		4.3		5.2	ns
t_{XZ3}		5.3		6.3		7.7	ns
t_{IOE}		0.5		0.6		0.7	ns
t_{IN}		3.6		4.1		5.1	ns
t_{IN_DELAY}		4.8		5.4		6.7	ns

Tables 29 through 33 show the timing information for EPF6016 devices.

Table 29. LE Timing Microparameters for EPF6016 Devices

Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
$t_{REG\_TO\_REG}$		2.2		2.8	ns
$t_{CASC\_TO\_REG}$		0.9		1.2	ns
$t_{CARRY\_TO\_REG}$		1.6		2.1	ns
$t_{DATA\_TO\_REG}$		2.4		3.0	ns
$t_{CASC\_TO\_OUT}$		1.3		1.7	ns
$t_{CARRY\_TO\_OUT}$		2.4		3.0	ns
$t_{DATA\_TO\_OUT}$		2.7		3.4	ns
$t_{REG\_TO\_OUT}$		0.3		0.5	ns
t_{SU}	1.1		1.6		ns
t_{H}	1.8		2.3		ns
t_{CO}		0.3		0.4	ns
t_{CLR}		0.5		0.6	ns
t_{C}		1.2		1.5	ns
t_{LD_CLR}		1.2		1.5	ns
$t_{CARRY\_TO\_CARRY}$		0.2		0.4	ns
$t_{REG\_TO\_CARRY}$		0.8		1.1	ns
$t_{DATA\_TO\_CARRY}$		1.7		2.2	ns
$t_{CARRY\_TO\_CASC}$		1.7		2.2	ns
$t_{CASC\_TO\_CASC}$		0.9		1.2	ns
$t_{REG\_TO\_CASC}$		1.6		2.0	ns
$t_{DATA\_TO\_CASC}$		1.7		2.1	ns
t_{CH}	4.0		4.0		ns
t_{CL}	4.0		4.0		ns

Table 30. IOE Timing Microparameters for EPF6016 Devices

Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
t_{OD1}		2.3		2.8	ns
t_{OD2}		4.6		5.1	ns

Table 33. External Timing Parameters for EPF6016 Devices

Parameter	Speed Grade				Unit
	-2		-3		
	Min	Max	Min	Max	
t_{INSU}	3.2		4.1		ns
t_{INH}	0.0		0.0		ns
t_{OUTCO}	2.0	7.9	2.0	9.9	ns

Tables 34 through 38 show the timing information for EPF6024A devices.

Table 34. LE Timing Microparameters for EPF6024A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
$t_{REG\_TO\_REG}$		1.2		1.3		1.6	ns
$t_{CASC\_TO\_REG}$		0.7		0.8		1.0	ns
$t_{CARRY\_TO\_REG}$		1.6		1.8		2.2	ns
$t_{DATA\_TO\_REG}$		1.3		1.4		1.7	ns
$t_{CASC\_TO\_OUT}$		1.2		1.3		1.6	ns
$t_{CARRY\_TO\_OUT}$		2.0		2.2		2.6	ns
$t_{DATA\_TO\_OUT}$		1.8		2.1		2.6	ns
$t_{REG\_TO\_OUT}$		0.3		0.3		0.4	ns
t_{SU}	0.9		1.0		1.2		ns
t_{H}	1.3		1.4		1.7		ns
t_{CO}		0.2		0.3		0.3	ns
t_{CLR}		0.3		0.3		0.4	ns
t_{C}		1.9		2.1		2.5	ns
t_{LD_CLR}		1.9		2.1		2.5	ns
$t_{CARRY\_TO\_CARRY}$		0.2		0.2		0.3	ns
$t_{REG\_TO\_CARRY}$		1.4		1.6		1.9	ns
$t_{DATA\_TO\_CARRY}$		1.3		1.4		1.7	ns
$t_{CARRY\_TO\_CASC}$		1.1		1.2		1.4	ns
$t_{CASC\_TO\_CASC}$		0.7		0.8		1.0	ns
$t_{REG\_TO\_CASC}$		1.4		1.6		1.9	ns
$t_{DATA\_TO\_CASC}$		1.0		1.1		1.3	ns
t_{CH}	2.5		3.0		3.5		ns
t_{CL}	2.5		3.0		3.5		ns

Table 38. External Timing Parameters for EPF6024A Devices

Parameter	Speed Grade						Unit
	-1		-2		-3		
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.0 *(1)*		2.2 *(1)*		2.6 *(1)*		ns
t_{INH}	0.2 *(2)*		0.2 *(2)*		0.3 *(2)*		ns
t_{OUTCO}	2.0	7.4	2.0	8.2	2.0	9.9	ns

Notes:
(1) Setup times are longer when the *Increase Input Delay* option is turned on. The setup time values are shown with the *Increase Input Delay* option turned off.
(2) Hold time is zero when the *Increase Input Delay* option is turned on.

Power Consumption

The supply power (P) for FLEX 6000 devices can be calculated with the following equations:

$$P = P_{INT} + P_{IO}$$
$$P = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in the "FLEX 6000 Device DC Operating Conditions" table on pages 31 and 33 of this data sheet. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is based on the amount of current that each LE typically consumes. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The $I_{CCACTIVE}$ value can be calculated with the following equation:

$$I_{CCACTIVE} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

Where:
$\mathbf{f_{MAX}}$ = Maximum operating frequency in MHz
N = Total number of LEs used in a FLEX 6000 device
$\mathbf{tog_{LC}}$ = Average percentage of LEs toggling at each clock (typically 12.5%)
K = Constant, shown in Table 39

Table 39. K Constant Values

Device	K Value
EPF6010A	14
EPF6016	88
EPF6016A	14
EPF6024A	14