# Intel - EPF6024ATC144-3N Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 196 |
| Number of Logic Elements/Cells | 1960 |
| Total RAM Bits | - |
| Number of I/O | 117 |
| Number of Gates | 24000 |
| Voltage - Supply | 3V ~ 3.6V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf6024atc144-3n |

Table 4 shows FLEX 6000 performance for more complex designs.

*Table 4. FLEX 6000 Device Performance for Complex Designs* *Note (1)*

| Application | LEs Used | Performance | | | Units |
|---|---|---|---|---|---|
| | | -1 Speed Grade | -2 Speed Grade | -3 Speed Grade | |
| 8-bit, 16-tap parallel finite impulse response (FIR) filter | 599 | 94 | 80 | 72 | MSPS |
| 8-bit, 512-point fast Fourier transform (FFT) function | 1,182 | 75<br>63 | 89<br>53 | 109<br>43 | µS<br>MHz |
| a16450 universal asynchronous receiver/transmitter (UART) | 487 | 36 | 30 | 25 | MHz |
| PCI bus target with zero wait states | 609 | 56 | 49 | 42 | MHz |

*Note:*
(1) The applications in this table were created using Altera MegaCore™ functions.

FLEX 6000 devices are supported by Altera development systems; a single, integrated package that offers schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development systems include DesignWare functions that are optimized for the FLEX 6000 architecture.

The Altera development system runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800.

f See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet* for more information.

## Functional Description

The FLEX 6000 OptiFLEX architecture consists of logic elements (LEs). Each LE includes a 4-input look-up table (LUT), which can implement any 4-input function, a register, and dedicated paths for carry and cascade chain functions. Because each LE contains a register, a design can be easily pipelined without consuming more LEs. The specified gate count for FLEX 6000 devices includes all LUTs and registers.

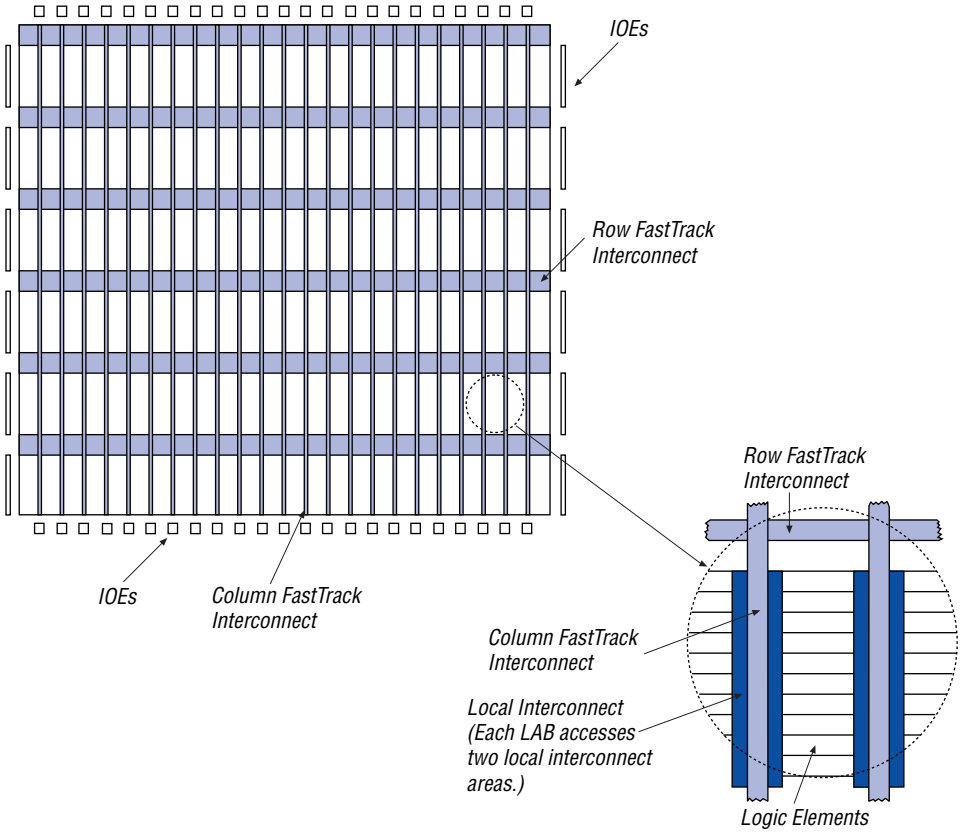
LEs are combined into groups called logic array blocks (LABs); each LAB contains 10 LEs. The Altera software automatically places related LEs into the same LAB, minimizing the number of required interconnects. Each LAB can implement a medium-sized block of logic, such as a counter or multiplexer.

Signal interconnections within FLEX 6000 devices—and to and from device pins—are provided via the routing structure of the FastTrack Interconnect. The routing structure is a series of fast, continuous row and column channels that run the entire length and width of the device. Any LE or pin can feed or be fed by any other LE or pin via the FastTrack Interconnect. See "FastTrack Interconnect" on page 17 of this data sheet for more information.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer. Each IOE is placed next to an LAB, where it can be driven by the local interconnect of that LAB. This feature allows fast clock-to-output times of less than 8 ns when a pin is driven by any of the 10 LEs in the adjacent LAB. Also, any LE can drive any pin via the row and column interconnect. I/O pins can drive the LE registers via the row and column interconnect, providing setup times as low as 2 ns and hold times of 0 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, and tri-state buffers.

Figure 1 shows a block diagram of the FLEX 6000 OptiFLEX architecture. Each group of ten LEs is combined into an LAB, and the LABs are arranged into rows and columns. The LABs are interconnected by the FastTrack Interconnect. IOEs are located at the end of each FastTrack Interconnect row and column.

*Figure 1. OptiFLEX Architecture Block Diagram*

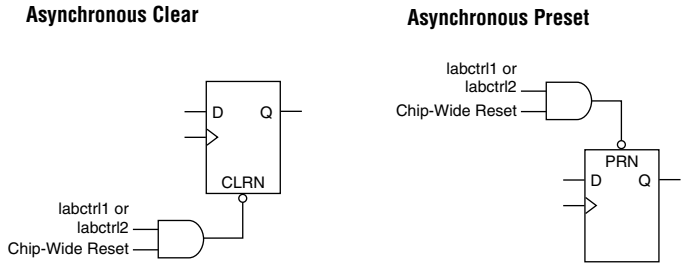



FLEX 6000 devices provide four dedicated, global inputs that drive the control inputs of the flipflops to ensure efficient distribution of high-speed, low-skew control signals. These inputs use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect. These inputs can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device. The dedicated global routing structure is built into the device, eliminating the need to create a clock tree.

## Logic Array Block

An LAB consists of ten LEs, their associated carry and cascade chains, the LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 6000 architecture, and facilitates efficient routing with optimum device utilization and high performance.

*Figure 8. LE Clear & Preset Modes*




**Asynchronous Clear**

The flipflop can be cleared by either LABCTRL1 or LABCTRL2.

**Asynchronous Preset**

An asynchronous preset is implemented with an asynchronous clear. The Altera software provides preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, this technique can be used when a register drives logic or drives a pin.

In addition to the two clear and preset modes, FLEX 6000 devices provide a chip-wide reset pin (DEV_CLRn) that can reset all registers in the device. The option to use this pin is set in the Altera software before compilation. The chip-wide reset overrides all other control signals. Any register with an asynchronous preset will be preset when the chip-wide reset is asserted because of the inversion technique used to implement the asynchronous preset.

The Altera software can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses an additional three LEs per register.

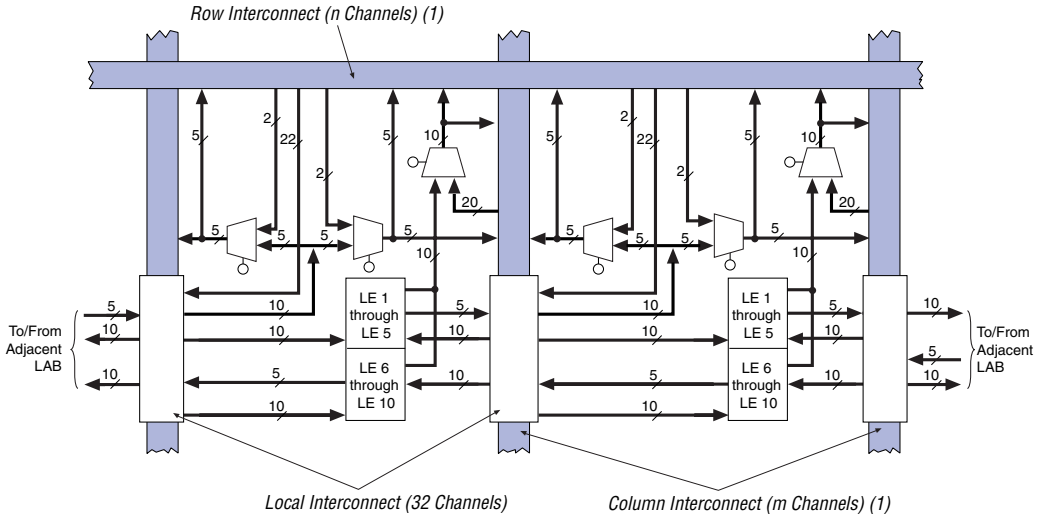
## FastTrack Interconnect

In the FLEX 6000 OptiFLEX architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even for complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of column and row interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect, which routes signals between LABs in the same row, and also routes signals from I/O pins to LABs. Additionally, the local interconnect routes signals between LEs in the same LAB and in adjacent LABs. The column interconnect routes signals between rows and routes signals from I/O pins to rows.

LEs 1 through 5 of an LAB drive the local interconnect to the right, while LEs 6 through 10 drive the local interconnect to the left. The `DATA1` and `DATA3` inputs of each LE are driven by the local interconnect to the left; `DATA2` and `DATA4` are driven by the local interconnect to the right. The local interconnect also routes signals from LEs to I/O pins. Figure 9 shows an overview of the FLEX 6000 interconnect architecture. LEs in the first and last columns have drivers on both sides so that all LEs in the LAB can drive I/O pins via the local interconnect.

***Figure 9. FastTrack Interconnect Architecture***




*Note:*

(1) For EPF6010A, EPF6016, and EPF6016A devices, $n$ = 144 channels and $m$ = 20 channels; for EPF6024A devices, $n$ = 186 channels and $m$ = 30 channels.

A row channel can be driven by an LE or by one of two column channels. These three signals feed a 3-to-1 multiplexer that connects to six specific row channels. Row channels drive into the local interconnect via multiplexers.

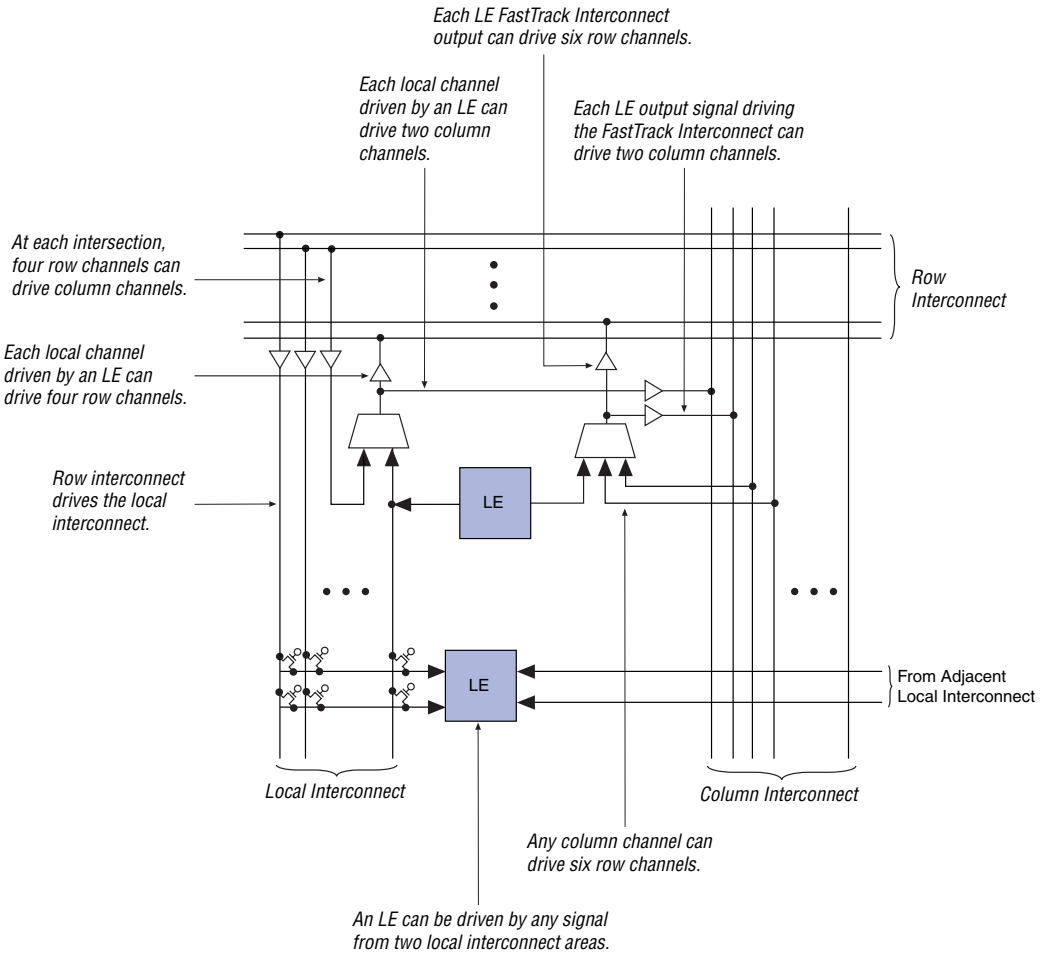
Each column of LABs is served by a dedicated column interconnect. The LEs in an LAB can drive the column interconnect. The LEs in an LAB, a column IOE, or a row interconnect can drive the column interconnect. The column interconnect can then drive another row's interconnect to route the signals to other LABs in the device. A signal from the column interconnect must be routed to the row interconnect before it can enter an LAB.

Each LE has a FastTrack Interconnect output and a local output. The FastTrack interconnect output can drive six row and two column lines directly; the local output drives the local interconnect. Each local interconnect channel driven by an LE can drive four row and two column channels. This feature provides additional flexibility, because each LE can drive any of ten row lines and four column lines.

In addition, LEs can drive global control signals. This feature is useful for distributing internally generated clock, asynchronous clear, and asynchronous preset signals. A pin-driven global signal can also drive data signals, which is useful for high-fan-out data signals.

Each LAB drives two groups of local interconnects, which allows an LE to drive two LABs, or 20 LEs, via the local interconnect. The row-to-local multiplexers are used more efficiently, because the multiplexers can now drive two LABs. Figure 10 shows how an LAB connects to row and column interconnects.

*Figure 10. LAB Connections to Row & Column Interconnects*




For improved routability, the row interconnect consists of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-length channel, which saves the other half of the channel for the other half of the row. One-third of the row channels are half-length channels.

Table 5 summarizes the FastTrack Interconnect resources available in each FLEX 6000 device.

*Table 5. FLEX 6000 FastTrack Interconnect Resources*

| Device | Rows | Channels per Row | Columns | Channels per Column |
|---|---|---|---|---|
| EPF6010A | 4 | 144 | 22 | 20 |
| EPF6016<br>EPF6016A | 6 | 144 | 22 | 20 |
| EPF6024A | 7 | 186 | 28 | 30 |

In addition to general-purpose I/O pins, FLEX 6000 devices have four dedicated input pins that provide low-skew signal distribution across the device. These four inputs can be used for global clock and asynchronous clear control signals. These signals are available as control signals for all LEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device. Using dedicated inputs to route data signals provides a fast path for high fan-out signals.

The local interconnect from LABs located at either end of two rows can drive a global control signal. For instance, in an EPF6016 device, LABs C1, D1, C22, and D22 can all drive global control signals. When an LE drives a global control signal, the dedicated input pin that drives that signal cannot be used. Any LE in the device can drive a global control signal by driving the FastTrack Interconnect into the appropriate LAB. To minimize delay, however, the Altera software places the driving LE in the appropriate LAB. The LE-driving-global signal feature is optimized for speed for control signals; regular data signals are better routed on the FastTrack Interconnect and do not receive any advantage from being routed on global signals. This LE-driving-global control signal feature is controlled by the designer and is not used automatically by the Altera software. See Figure 11.

*Figure 15. SameFrame Pin-Out Example*

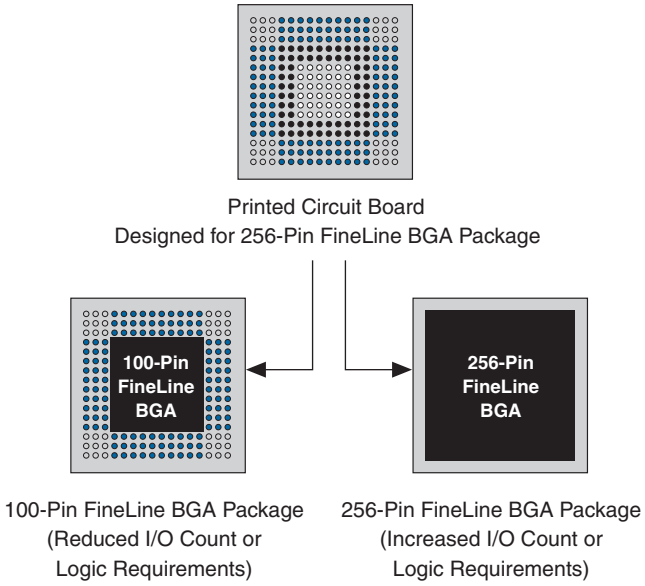



Table 6 lists the 3.3-V FLEX 6000 devices with the SameFrame pin-out feature.

*Table 6. 3.3-V FLEX 6000 Devices with SameFrame Pin-Outs*

| Device | 100-Pin FineLine BGA | 256-Pin FineLine BGA |
|---|---|---|
| EPF6016A | v | v |
| EPF6024A | | v |

# Output Configuration

This section discusses slew-rate control, the MultiVolt I/O interface, power sequencing, and hot-socketing for FLEX 6000 devices.

## Slew-Rate Control

The output buffer in each IOE has an adjustable output slew-rate that can be configured for low-noise or high-speed performance. A slower slew-rate reduces system noise and adds a maximum delay of 6.8 ns. The fast slew-rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew-rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a device-wide basis. The slew-rate setting affects only the falling edge of the output.

Open-drain output pins on 5.0-V or 3.3-V FLEX 6000 devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a $V_{IH}$ of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The $I_{OL}$ current specification should be considered when selecting a pull-up resistor.

Output pins on 5.0-V FLEX 6000 devices with $V_{CCIO}$ = 3.3 V or 5.0 V (with a pull-up resistor to the 5.0-V supply) can also drive 5.0-V CMOS input pins. In this case, the pull-up transistor will turn off when the pin voltage exceeds 3.3 V. Therefore, the pin does not have to be open-drain.

### Power Sequencing & Hot-Socketing

Because FLEX 6000 family devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The $V_{CCIO}$ and $V_{CCINT}$ power planes can be powered in any order.

Signals can be driven into 3.3-V FLEX 6000 devices before and during power up without damaging the device. Additionally, FLEX 6000 devices do not drive out during power up. Once operating conditions are reached, FLEX 6000 devices operate as specified by the user.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 6000 devices provide JTAG BST circuitry that comply with the IEEE Std. 1149.1-1990 specification. Table 8 shows JTAG instructions for FLEX 6000 devices. JTAG BST can be performed before or after configuration, but not during configuration (except when you disable JTAG support in user mode).

1 See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG BST circuitry.

*Table 8. FLEX 6000 JTAG Instructions*

| JTAG Instruction | Description |
|---|---|
| SAMPLE/PRELOAD | Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. |
| EXTEST | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test result at the input pins. |
| BYPASS | Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation. |

The instruction register length for FLEX 6000 devices is three bits. Table 9 shows the boundary-scan register length for FLEX 6000 devices.

*Table 9. FLEX 6000 Device Boundary-Scan Register Length*

| Device | Boundary-Scan Register Length |
|---|---|
| EPF6010A | 522 |
| EPF6016 | 621 |
| EPF6016A | 522 |
| EPF6024A | 666 |

FLEX 6000 devices include a weak pull-up on JTAG pins.

f See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information.

Figure 16 shows the timing requirements for the JTAG signals.

*Figure 16. JTAG Waveforms*

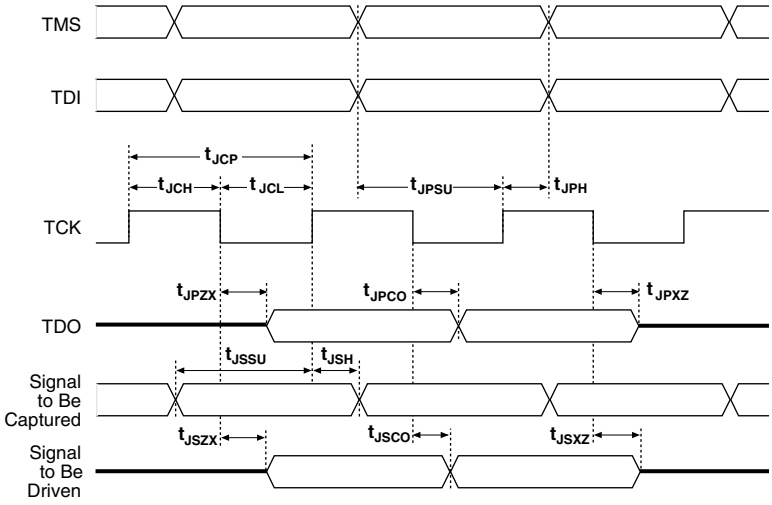



Table 10 shows the JTAG timing parameters and values for FLEX 6000 devices.

**Table 13. FLEX 6000 5.0-V Device DC Operating Conditions** *Notes (5), (6)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | | $V_{CCINT}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8 | V |
| $V_{OH}$ | 5.0-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 4.75 V *(7)* | 2.4 | | | V |
| | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(7)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(7)* | $V_{CCIO}$ – 0.2 | | | V |
| $V_{OL}$ | 5.0-V low-level TTL output voltage | $I_{OL}$ = 8 mA DC, $V_{CCIO}$ = 4.75 V *(8)* | | | 0.45 | V |
| | 3.3-V low-level TTL output voltage | $I_{OL}$ = 8 mA DC, $V_{CCIO}$ = 3.00 V *(8)* | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(8)* | | | 0.2 | V |
| $I_I$ | Input pin leakage current | $V_I$ = $V_{CC}$ or ground *(8)* | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = $V_{CC}$ or ground *(8)* | –40 | | 40 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = ground, no load | | 0.5 | 5 | mA |

**Table 14. FLEX 6000 5.0-V Device Capacitance** *Note (9)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance for I/O pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance for dedicated input | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

*Notes to tables:*

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum $V_{CC}$ rise time to 100 ms. $V_{CC}$ must rise monotonically.
(5) Typical values are for $T_A$ = 25° C and $V_{CC}$ = 5.0 V.
(6) These values are specified under the FLEX 6000 Recommended Operating Conditions shown in Table 12 on page 31.
(7) The $I_{OH}$ parameter refers to high-level TTL or CMOS output current.
(8) The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(9) Capacitance is sample-tested only.

Figure 18 shows the typical output drive characteristics of 5.0-V and 3.3-V FLEX 6000 devices with 5.0-V, 3.3-V, and 2.5-V $V_{CCIO}$. When $V_{CCIO}$ = 5.0 V on EPF6016 devices, the output driver is compliant with the ***PCI Local Bus Specification, Revision 2.2*** for 5.0-V operation. When $V_{CCIO}$ = 3.3 V on the EPF6010A and EPF6016A devices, the output driver is compliant with the ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation.

***Figure 18. Output Drive Characteristics***

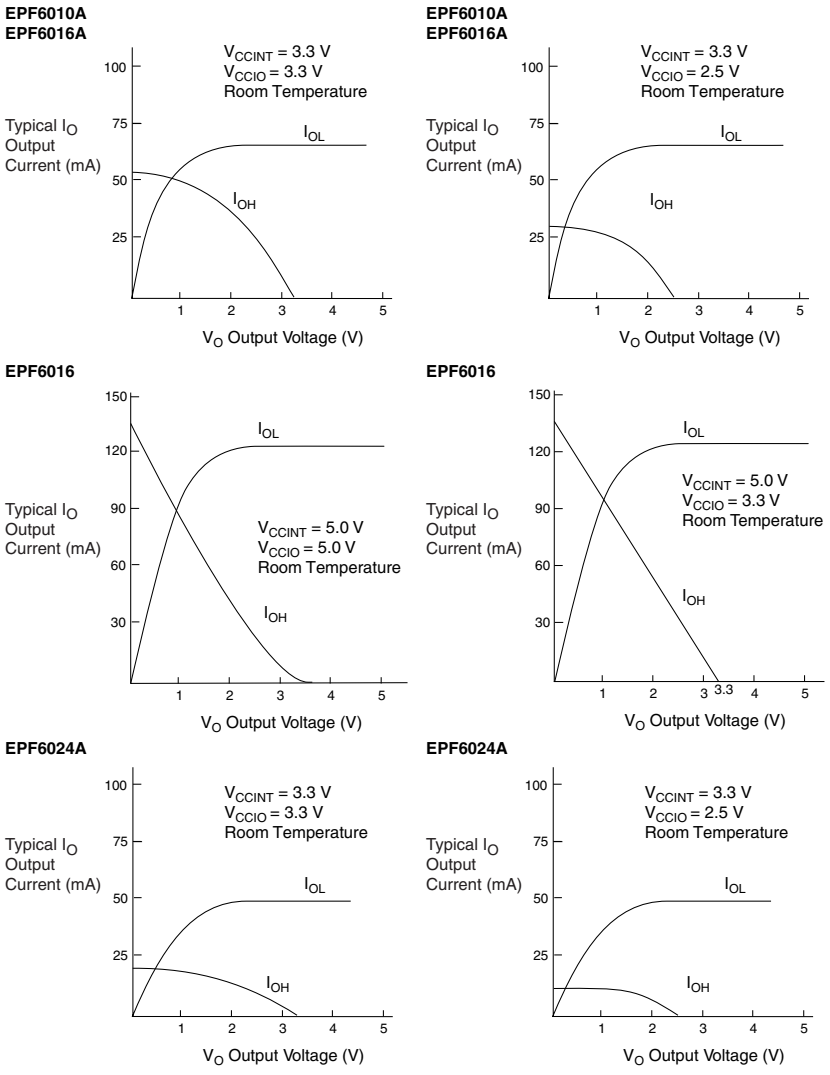


*Figure 19. FLEX 6000 Timing Model*

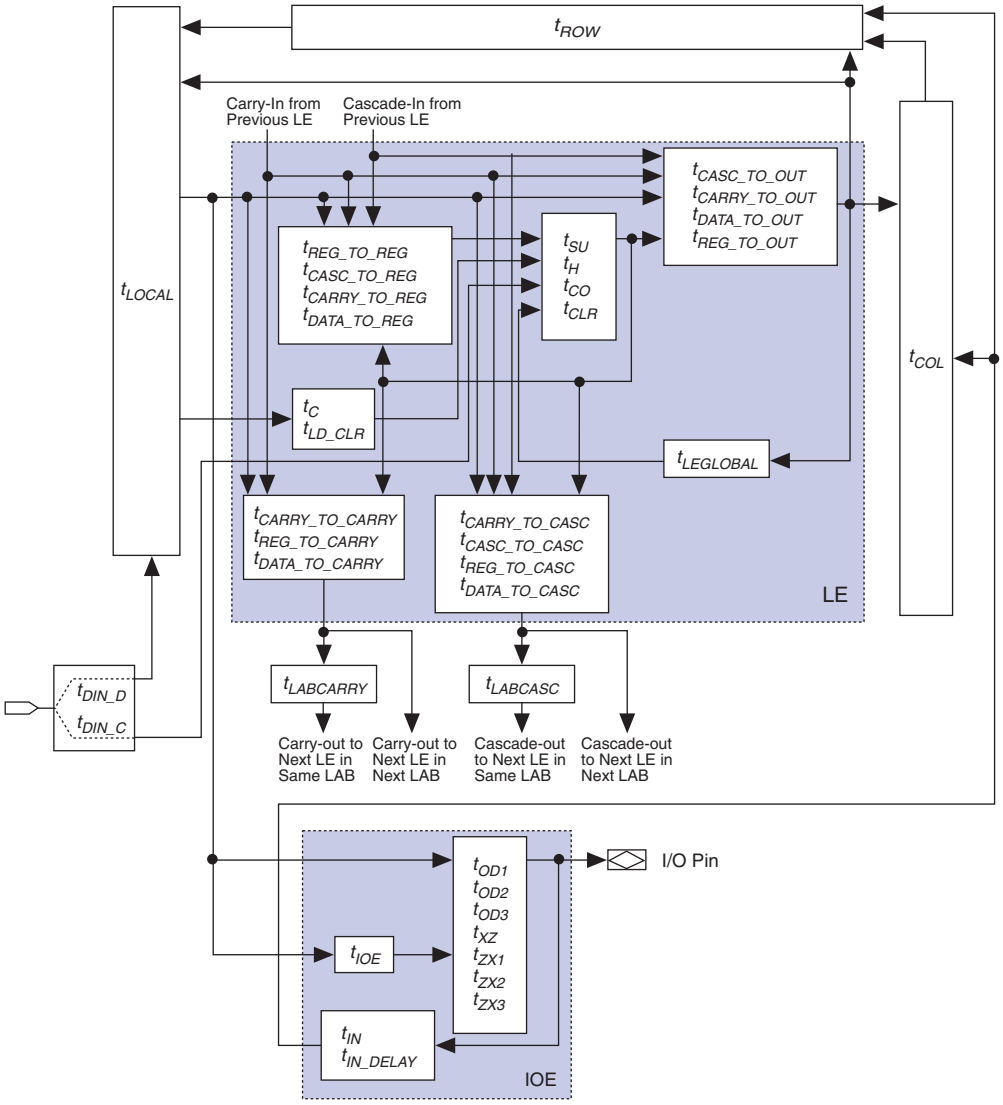


*Table 24. LE Timing Microparameters for EPF6010A & EPF6016A Devices (Part 2 of 2)*

| Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{CO}$ | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{CLR}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{C}$ | | 1.8 | | 2.1 | | 2.6 | ns |
| $t_{LD\_CLR}$ | | 1.8 | | 2.1 | | 2.6 | ns |
| $t_{CARRY\_TO\_CARRY}$ | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{REG\_TO\_CARRY}$ | | 1.6 | | 1.9 | | 2.3 | ns |
| $t_{DATA\_TO\_CARRY}$ | | 2.1 | | 2.5 | | 3.0 | ns |
| $t_{CARRY\_TO\_CASC}$ | | 1.0 | | 1.1 | | 1.4 | ns |
| $t_{CASC\_TO\_CASC}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{REG\_TO\_CASC}$ | | 1.4 | | 1.7 | | 2.1 | ns |
| $t_{DATA\_TO\_CASC}$ | | 1.1 | | 1.2 | | 1.5 | ns |
| $t_{CH}$ | 2.5 | | 3.0 | | 3.5 | | ns |
| $t_{CL}$ | 2.5 | | 3.0 | | 3.5 | | ns |

*Table 25. IOE Timing Microparameters for EPF6010A & EPF6016A Devices*

| Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{OD1}$ | | 1.9 | | 2.2 | | 2.7 | ns |
| $t_{OD2}$ | | 4.1 | | 4.8 | | 5.8 | ns |
| $t_{OD3}$ | | 5.8 | | 6.8 | | 8.3 | ns |
| $t_{XZ}$ | | 1.4 | | 1.7 | | 2.1 | ns |
| $t_{XZ1}$ | | 1.4 | | 1.7 | | 2.1 | ns |
| $t_{XZ2}$ | | 3.6 | | 4.3 | | 5.2 | ns |
| $t_{XZ3}$ | | 5.3 | | 6.3 | | 7.7 | ns |
| $t_{IOE}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{IN}$ | | 3.6 | | 4.1 | | 5.1 | ns |
| $t_{IN\_DELAY}$ | | 4.8 | | 5.4 | | 6.7 | ns |

Tables 29 through 33 show the timing information for EPF6016 devices.

*Table 29. LE Timing Microparameters for EPF6016 Devices*

| Parameter | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | -2 | | -3 | | |
| | Min | Max | Min | Max | |
| $t_{REG\_TO\_REG}$ | | 2.2 | | 2.8 | ns |
| $t_{CASC\_TO\_REG}$ | | 0.9 | | 1.2 | ns |
| $t_{CARRY\_TO\_REG}$ | | 1.6 | | 2.1 | ns |
| $t_{DATA\_TO\_REG}$ | | 2.4 | | 3.0 | ns |
| $t_{CASC\_TO\_OUT}$ | | 1.3 | | 1.7 | ns |
| $t_{CARRY\_TO\_OUT}$ | | 2.4 | | 3.0 | ns |
| $t_{DATA\_TO\_OUT}$ | | 2.7 | | 3.4 | ns |
| $t_{REG\_TO\_OUT}$ | | 0.3 | | 0.5 | ns |
| $t_{SU}$ | 1.1 | | 1.6 | | ns |
| $t_{H}$ | 1.8 | | 2.3 | | ns |
| $t_{CO}$ | | 0.3 | | 0.4 | ns |
| $t_{CLR}$ | | 0.5 | | 0.6 | ns |
| $t_{C}$ | | 1.2 | | 1.5 | ns |
| $t_{LD\_CLR}$ | | 1.2 | | 1.5 | ns |
| $t_{CARRY\_TO\_CARRY}$ | | 0.2 | | 0.4 | ns |
| $t_{REG\_TO\_CARRY}$ | | 0.8 | | 1.1 | ns |
| $t_{DATA\_TO\_CARRY}$ | | 1.7 | | 2.2 | ns |
| $t_{CARRY\_TO\_CASC}$ | | 1.7 | | 2.2 | ns |
| $t_{CASC\_TO\_CASC}$ | | 0.9 | | 1.2 | ns |
| $t_{REG\_TO\_CASC}$ | | 1.6 | | 2.0 | ns |
| $t_{DATA\_TO\_CASC}$ | | 1.7 | | 2.1 | ns |
| $t_{CH}$ | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 4.0 | | 4.0 | | ns |

*Table 30. IOE Timing Microparameters for EPF6016 Devices*

| Parameter | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | -2 | | -3 | | |
| | Min | Max | Min | Max | |
| $t_{OD1}$ | | 2.3 | | 2.8 | ns |
| $t_{OD2}$ | | 4.6 | | 5.1 | ns |

*Table 33. External Timing Parameters for EPF6016 Devices*

| Parameter | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | -2 | | -3 | | |
| | Min | Max | Min | Max | |
| $t_{INSU}$ | 3.2 | | 4.1 | | ns |
| $t_{INH}$ | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ | 2.0 | 7.9 | 2.0 | 9.9 | ns |

Tables 34 through 38 show the timing information for EPF6024A devices.

*Table 34. LE Timing Microparameters for EPF6024A Devices*

| Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{REG\_TO\_REG}$ | | 1.2 | | 1.3 | | 1.6 | ns |
| $t_{CASC\_TO\_REG}$ | | 0.7 | | 0.8 | | 1.0 | ns |
| $t_{CARRY\_TO\_REG}$ | | 1.6 | | 1.8 | | 2.2 | ns |
| $t_{DATA\_TO\_REG}$ | | 1.3 | | 1.4 | | 1.7 | ns |
| $t_{CASC\_TO\_OUT}$ | | 1.2 | | 1.3 | | 1.6 | ns |
| $t_{CARRY\_TO\_OUT}$ | | 2.0 | | 2.2 | | 2.6 | ns |
| $t_{DATA\_TO\_OUT}$ | | 1.8 | | 2.1 | | 2.6 | ns |
| $t_{REG\_TO\_OUT}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{SU}$ | 0.9 | | 1.0 | | 1.2 | | ns |
| $t_{H}$ | 1.3 | | 1.4 | | 1.7 | | ns |
| $t_{CO}$ | | 0.2 | | 0.3 | | 0.3 | ns |
| $t_{CLR}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{C}$ | | 1.9 | | 2.1 | | 2.5 | ns |
| $t_{LD\_CLR}$ | | 1.9 | | 2.1 | | 2.5 | ns |
| $t_{CARRY\_TO\_CARRY}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{REG\_TO\_CARRY}$ | | 1.4 | | 1.6 | | 1.9 | ns |
| $t_{DATA\_TO\_CARRY}$ | | 1.3 | | 1.4 | | 1.7 | ns |
| $t_{CARRY\_TO\_CASC}$ | | 1.1 | | 1.2 | | 1.4 | ns |
| $t_{CASC\_TO\_CASC}$ | | 0.7 | | 0.8 | | 1.0 | ns |
| $t_{REG\_TO\_CASC}$ | | 1.4 | | 1.6 | | 1.9 | ns |
| $t_{DATA\_TO\_CASC}$ | | 1.0 | | 1.1 | | 1.3 | ns |
| $t_{CH}$ | 2.5 | | 3.0 | | 3.5 | | ns |
| $t_{CL}$ | 2.5 | | 3.0 | | 3.5 | | ns |

*Table 35. IOE Timing Microparameters for EPF6024A Devices*

| Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{OD1}$ | | 1.9 | | 2.1 | | 2.5 | ns |
| $t_{OD2}$ | | 4.0 | | 4.4 | | 5.3 | ns |
| $t_{OD3}$ | | 7.0 | | 7.8 | | 9.3 | ns |
| $t_{XZ}$ | | 4.3 | | 4.8 | | 5.8 | ns |
| $t_{XZ1}$ | | 4.3 | | 4.8 | | 5.8 | ns |
| $t_{XZ2}$ | | 6.4 | | 7.1 | | 8.6 | ns |
| $t_{XZ3}$ | | 9.4 | | 10.5 | | 12.6 | ns |
| $t_{IOE}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{IN}$ | | 3.3 | | 3.7 | | 4.4 | ns |
| $t_{IN\_DELAY}$ | | 5.3 | | 5.9 | | 7.0 | ns |

*Table 36. Interconnect Timing Microparameters for EPF6024A Devices*

| Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LOCAL}$ | | 0.8 | | 0.8 | | 1.1 | ns |
| $t_{ROW}$ | | 3.0 | | 3.1 | | 3.3 | ns |
| $t_{COL}$ | | 3.0 | | 3.2 | | 3.4 | ns |
| $t_{DIN\_D}$ | | 5.4 | | 5.6 | | 6.2 | ns |
| $t_{DIN\_C}$ | | 4.6 | | 5.1 | | 6.1 | ns |
| $t_{LEGLOBAL}$ | | 3.1 | | 3.5 | | 4.3 | ns |
| $t_{LABCARRY}$ | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{LABCASC}$ | | 0.3 | | 0.3 | | 0.4 | ns |

*Table 37. External Reference Timing Parameters for EPF6024A Devices*

| Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_1$ | | 45.0 | | 50.0 | | 60.0 | ns |

*Table 38. External Timing Parameters for EPF6024A Devices*

| Parameter | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | -1 | | -2 | | -3 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.0 *(1)* | | 2.2 *(1)* | | 2.6 *(1)* | | ns |
| $t_{INH}$ | 0.2 *(2)* | | 0.2 *(2)* | | 0.3 *(2)* | | ns |
| $t_{OUTCO}$ | 2.0 | 7.4 | 2.0 | 8.2 | 2.0 | 9.9 | ns |

*Notes:*
(1) Setup times are longer when the *Increase Input Delay* option is turned on. The setup time values are shown with the *Increase Input Delay* option turned off.
(2) Hold time is zero when the *Increase Input Delay* option is turned on.

## Power Consumption

The supply power (P) for FLEX 6000 devices can be calculated with the following equations:

$$P = P_{INT} + P_{IO}$$
$$P = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as $I_{CC0}$ in the "FLEX 6000 Device DC Operating Conditions" table on pages 31 and 33 of this data sheet. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is based on the amount of current that each LE typically consumes. The $P_{IO}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The $I_{CCACTIVE}$ value can be calculated with the following equation:

$$I_{CCACTIVE} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

Where:
$\mathbf{f_{MAX}}$ = Maximum operating frequency in MHz
$N$ = Total number of LEs used in a FLEX 6000 device
$\mathbf{tog_{LC}}$ = Average percentage of LEs toggling at each clock (typically 12.5%)
K = Constant, shown in Table 39

*Table 39. K Constant Values*

| Device | K Value |
|---|---|
| EPF6010A | 14 |
| EPF6016 | 88 |
| EPF6016A | 14 |
| EPF6024A | 14 |

## Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* for pin-out information.