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#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc857dslzq66b

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



#### Features



\*The MPC862T contains 4-Kbyte instruction cache and 4-Kbyte data cache.

Figure 1. MPC862P/862T Block Diagram



Die Revision	Frequency	Typical <sup>1</sup>	Maximum <sup>2</sup>	Unit
A.1, B.0	66 MHz	910	1060	mW
(2:1 Mode)	80 MHz	1.06	1.20	W
B.0 (2:1 Mode)	100 MHz	1.35	1.54	W

Table 4. Power Dissipation (P<sub>D</sub>) (continued)

<sup>1</sup> Typical power dissipation is measured at 3.3 V.

<sup>2</sup> Maximum power dissipation is measured at 3.5 V.

### NOTE

Values in Table 4 represent VDDL based power dissipation and do not include I/O power dissipation over VDDH. I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

## 6 DC Characteristics

Table 5 provides the DC electrical characteristics for the MPC862/857T/857DSL.

Characteristic	Symbol	Min	Мах	Unit
Operating voltage	VDDH, VDDL, KAPWR, VDDSYN	3.135	3.465	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	VDDH – 0.4	VDDH	V
Input High Voltage (all inputs except EXTAL and EXTCLK)	VIH	2.0	5.5	V
Input Low Voltage <sup>1</sup>	VIL	GND	0.8	V
EXTAL, EXTCLK Input High Voltage	VIHC	0.7*(VCC)	VCC+0.3	V
Input Leakage Current, Vin = 5.5 V (Except TMS, TRST, DSCK and DSDI pins)	l <sub>in</sub>	—	100	μA
Input Leakage Current, Vin = 3.6 V (Except TMS, TRST, DSCK, and DSDI)	I <sub>In</sub>	—	10	μA
Input Leakage Current, Vin = 0 V (Except TMS, $\overline{\text{TRST}}$ , DSCK, and DSDI pins)	I <sub>In</sub>	—	10	μA
Input Capacitance <sup>2</sup>	C <sub>in</sub>	_	20	pF
Output High Voltage, IOH = -2.0 mA, VDDH = 3.0 V (Except XTAL, XFC, and Open drain pins)	VOH	2.4	_	V

**Table 5. DC Electrical Specifications** 





## 7.6 References

Semiconductor Equipment and Materials International	(415) 964-5111
805 East Middlefield Rd.	
Mountain View, CA 94043	
MIL-SPEC and EIA/JESD (JEDEC) Specifications	800-854-7179 or
(Available from Global Engineering Documents)	303-397-7956
JEDEC Specifications	http://www.jedec.org

1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

# 8 Layout Practices

Each  $V_{CC}$  pin on the MPC862/857T/857DSL should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The  $V_{CC}$  power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip  $V_{CC}$  and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as  $V_{CC}$  and GND planes.

All output pins on the MPC862/857T/857DSL have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the  $V_{CC}$  and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

# 9 Bus Signal Timing

The maximum bus speed supported by the MPC862/857T/857DSL is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC862/857T/857DSL used at 80MHz must be configured for a 40 MHz bus). Table 6 shows the period ranges for standard part frequencies.

Erog	50 N	50 MHz		66 MHz		lHz	100	MHz
Freq	Min	Max	Min	Max	Min	Мах	Min	Max
Period	20.00	30.30	15.15	30.30	25.00	30.30	20.00	30.30

Table 6. Period Range for Standard Part Frequencies



Nume	Charaotariatia	33 MHz		40 MHz		50 MHz		66 MHz		11
NUM	Characteristic	Min	Max	Min	Max	Min	Мах	Min	Max	Unit
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 x B1 - 2.00)	35.90		29.30		23.00		16.90		ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	_	20.70	_	ns
B28	CLKOUT rising edge to $\overline{WE}(0:3)$ negated GPCM write access CSNT = 0 (MAX = 0.00 x B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, 1, CSNT = 1, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	_	14.30	_	13.00	_	11.80	_	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0,1, CSNT = 1, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	_	18.00	_	18.00	_	14.30	_	12.30	ns
B29	WE(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	_	1.80	—	ns
B29a	WE(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	_	10.50	_	8.00	_	5.60	_	ns
B29b	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3), High Z GPCM write access, ACS = 00, TRLX = 0,1 & CSNT = 0 (MIN = 0.25 x B1 - 2.00)	5.60	_	4.30	_	3.00	—	1.80	_	ns
B29c	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	_	10.50	_	8.00	_	5.60	_	ns

Table 7. Bus Operation	i Timings	(continued)
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**Bus Signal Timing** 

Num	Characteristic	33	MHz	40 MHz		50 MHz		66 MHz		l l m it
NUM	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B29d	$\overline{\text{WE}}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 x B1 - 2.00)	43.50	_	35.50	_	28.00	_	20.70	_	ns
B29e	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 1.50 x B1 - 2.00)	43.50	_	35.50	_	28.00	_	20.70	_	ns
B29f	WE(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 6.30)	5.00	_	3.00	_	1.10	_	0.00	_	ns
B29g	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 - 6.30)	5.00		3.00	_	1.10	_	0.00	_	ns
B29h	WE(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 3.30)	38.40	_	31.10	_	24.20	_	17.50	_	ns
B29i	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 - 3.30)	38.40	_	31.10	_	24.20	_	17.50	_	ns
B30	$\overline{CS}$ , $\overline{WE}$ (0:3) negated to A(0:31), BADDR(28:30) Invalid GPCM write access <sup>11</sup> (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	_	3.00	_	1.80	—	ns
B30a	$\label{eq:weighted} \begin{array}{l} \overline{\text{WE}}(0:3) \text{ negated to A}(0:31),\\ \text{BADDR}(28:30) \text{ Invalid GPCM}, \text{ write}\\ \text{access, TRLX} = 0, \text{ CSNT} = 1, \overline{\text{CS}}\\ \text{negated to A}(0:31) \text{ invalid GPCM write}\\ \text{access TRLX} = 0, \text{ CSNT} = 1 \text{ ACS} = 10,\\ \text{or ACS} == 11, \text{ EBDF} = 0 (\text{MIN} = 0.50)\\ \text{x B1} - 2.00) \end{array}$	13.20	_	10.50		8.00		5.60	_	ns
B30b	$\overline{WE}(0:3) \text{ negated to } A(0:31) \text{ Invalid} \\ \text{GPCM BADDR}(28:30) \text{ invalid GPCM} \\ \text{write access, TRLX = 1, CSNT = 1.} \\ \overline{CS} \text{ negated to } A(0:31) \text{ Invalid GPCM} \\ \text{write access TRLX = 1, CSNT = 1,} \\ \text{ACS = 10, or ACS == 11 EBDF = 0} \\ (\text{MIN = 1.50 x B1 - 2.00)} \\ \end{array}$	43.50		35.50		28.00	_	20.70		ns

## Table 7. Bus Operation Timings (continued)



Figure 10 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)



Memory Controller and DLT3 = 1

Figure 11 through Figure 14 provide the timing for the external bus read controlled by various GPCM factors.





**Bus Signal Timing** 







Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)





ACS = 10, ACS = 11)



**Bus Signal Timing** 

Figure 19 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.



Cycles Timing

Figure 20 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.











**CPM Electrical Characteristics** 



Figure 44. Parallel I/O Data-In/Data-Out Timing Diagram

## **11.2 Port C Interrupt AC Electrical Specifications**

Table 15 provides the timings for port C interrupts.

## Table 15. Port C Interrupt Timing

Num	Characteristic	33.34	Unit	
Num	Characteristic	Min	Мах	Unit
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	_	ns

Figure 45 shows the port C interrupt detection timing.



Figure 45. Port C Interrupt Detection Timing

## **11.3 IDMA Controller AC Electrical Specifications**

Table 16 provides the IDMA controller timings as shown in Figure 46 though Figure 49.

## Table 16. IDMA Controller Timing

Num	Characteristic	All Freq	Unit	
Num	onaracteristic		Max	Onit
40	DREQ setup time to clock high	7	_	ns
41	DREQ hold time from clock high	3	_	ns
42	SDACK assertion delay from clock high	—	12	ns



**CPM Electrical Characteristics** 



Figure 49. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA



#### **CPM Electrical Characteristics**

Num	Charactariatia	All Freq	Unit	
Num	Characteristic	Min	Мах	Onit
83a	L1RCLK, L1TCLK width high (DSC = $1$ ) <sup>3</sup>	P + 10	—	ns
84	L1CLK edge to L1CLKO valid (DSC = 1)	_	30.00	ns
85	L1RQ valid before falling edge of L1TSYNC <sup>4</sup>	1.00	—	L1TCL K
86	L1GR setup time <sup>2</sup>	42.00	_	ns
87	L1GR hold time	42.00	—	ns
88	L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

#### Table 19. SI Timing (continued)

<sup>1</sup> The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

<sup>2</sup> These specs are valid for IDL mode only.

<sup>3</sup> Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

<sup>4</sup> These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.



Figure 52. SI Receive Timing Diagram with Normal Clocking (DSC = 0)



**CPM Electrical Characteristics** 

Figure 57 through Figure 59 show the NMSI timings.





#### **FEC Electrical Characteristics**

Num	Characteristic	Min	Max	Unit
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Table 30. MII Transmit Signal Timing (continued)

Figure 74 shows the MII transmit signal timing diagram.



Figure 74. MII Transmit Signal Timing Diagram

## 13.3 MII Async Inputs Signal Timing (MII\_CRS, MII\_COL)

Table 31 provides information on the MII async inputs signal timing.

Table 31. MII Async Inputs Signal Timing

Num	Characteristic	Min	Мах	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5		MII_TX_CLK period

Figure 75 shows the MII asynchronous inputs signal timing diagram.



Figure 75. MII Async Inputs Timing Diagram

## 13.4 MII Serial Management Channel Timing (MII\_MDIO, MII\_MDC)

Table 32 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.





Figure 77. Pinout of the PBGA Package



Name	Pin Number	Туре
PA15 RXD1 RXD4	C18	Bidirectional
PA14 TXD1 TXD4	D17	Bidirectional (Optional: Open-drain)
PA13 RXD2	E17	Bidirectional
PA12 TXD2	F17	Bidirectional (Optional: Open-drain)
PA11 L1TXDB RXD3	G16	Bidirectional (Optional: Open-drain)
PA10 L1RXDB TXD3	J17	Bidirectional (Optional: Open-drain)
PA9 L1TXDA	К18	Bidirectional (Optional: Open-drain)
RXD4		
PA8 L1RXDA TXD4	L17	Bidirectional (Optional: Open-drain)
PA7 CLK1 L1RCLKA BRGO1 TIN1	M19	Bidirectional
PA6 CLK2 TOUT1	M17	Bidirectional
PA5 CLK3 L1TCLKA BRGO2 TIN2	N18	Bidirectional
PA4 CLK4 TOUT2	P19	Bidirectional
PA3 CLK5 BRGO3 TIN3	P17	Bidirectional

## Table 35. Pin Assignments (continued)



Name	Pin Number	Туре
PB21 SMTXD2 L1CLKOB PHSEL1 <sup>1</sup> TXADDR1 <sup>2</sup>	К16	Bidirectional (Optional: Open-drain)
PB20 SMRXD2 L1CLKOA PHSEL0 <sup>1</sup> TXADDR0 <sup>2</sup>	L16	Bidirectional (Optional: Open-drain)
PB19 RTS1 L1ST1	N19	Bidirectional (Optional: Open-drain)
PB18 RXADDR4 <sup>2</sup> RTS2 L1ST2	N17	Bidirectional (Optional: Open-drain)
PB17 L1RQb L1ST3 RTS3 PHREQ1 <sup>1</sup> RXADDR1 <sup>2</sup>	P18	Bidirectional (Optional: Open-drain)
PB16 L1RQa L1ST4 RTS4 PHREQ0 <sup>1</sup> RXADDR0 <sup>2</sup>	N16	Bidirectional (Optional: Open-drain)
PB15 BRGO3 TxClav	R17	Bidirectional
PB14 RXADDR2 <sup>2</sup> RSTRT1	U18	Bidirectional
PC15 DREQ0 RTS1 L1ST1 RxClav	D16	Bidirectional
PC14 DREQ1 RTS2 L1ST2	D18	Bidirectional



Table 35. Pin Assignment	ts (continued)
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Name	Pin Number	Туре
PD12 L1RSYNCB MII-MDC UTPB3	R16	Bidirectional
PD11 RXD3 MII-TXERR RXENB	T16	Bidirectional
PD10 TXD3 MII-RXD0 TXENB	W18	Bidirectional
PD9 RXD4 MII-TXD0 UTPCLK	V17	Bidirectional
PD8 TXD4 MII-MDC MII-RXCLK	W17	Bidirectional
PD7 RTS3 MII-RXERR UTPB4	T15	Bidirectional
PD6 RTS4 MII-RXDV UTPB5	V16	Bidirectional
PD5 REJECT2 MII-TXD3 UTPB6	U15	Bidirectional
PD4 REJECT3 MII-TXD2 UTPB7	U16	Bidirectional
PD3 REJECT4 MII-TXD1 SOC	W16	Bidirectional
TMS	G18	Input
TDI DSDI	H17	Input
TCK DSCK	H16	Input

Name	Pin Number	Туре
TRST	G19	Input
TDO DSDO	G17	Output
M_CRS	B7	Input
M_MDIO	H18	Bidirectional
M_TXEN	V15	Output
M_COL	H4	Input
KAPWR	R1	Power
GND	F6, F7, F8, F9, F10, F11, F12, F13, F14, G6, G7, G8, G9, G10, G11, G12, G13, G14, H6, H7, H8, H9, H10, H11, H12, H13, H14, J6, J7, J8, J9, J10, J11, J12, J13, J14, K6, K7, K8, K9, K10, K11, K12, K13, K14, L6, L7, L8, L9, L10, L11, L12, L13, L14, M6, M7, M8, M9, M10, M11, M12, M13, M14, N6, N7, N8, N9, N10, N11, N12, N13, N14, P6, P7, P8, P9, P10, P11, P12, P13, P14	Power
VDDL	A8, M1, W8, H19, F4, F16, P4, P16	Power
VDDH	E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P5, P15, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, T14	Power
N/C	D6, D13, D14, U2, V2	No-connect

### Table 35. Pin Assignments (continued)

<sup>1</sup> Classic SAR mode only

<sup>2</sup> ESAR mode only

## 14.2 Mechanical Dimensions of the PBGA Package

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to *Plastic Ball Grid Array Application Note* (order number: AN1231/D) available from your local Freescale sales office. Figure 78 shows the mechanical dimensions of the PBGA package.