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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

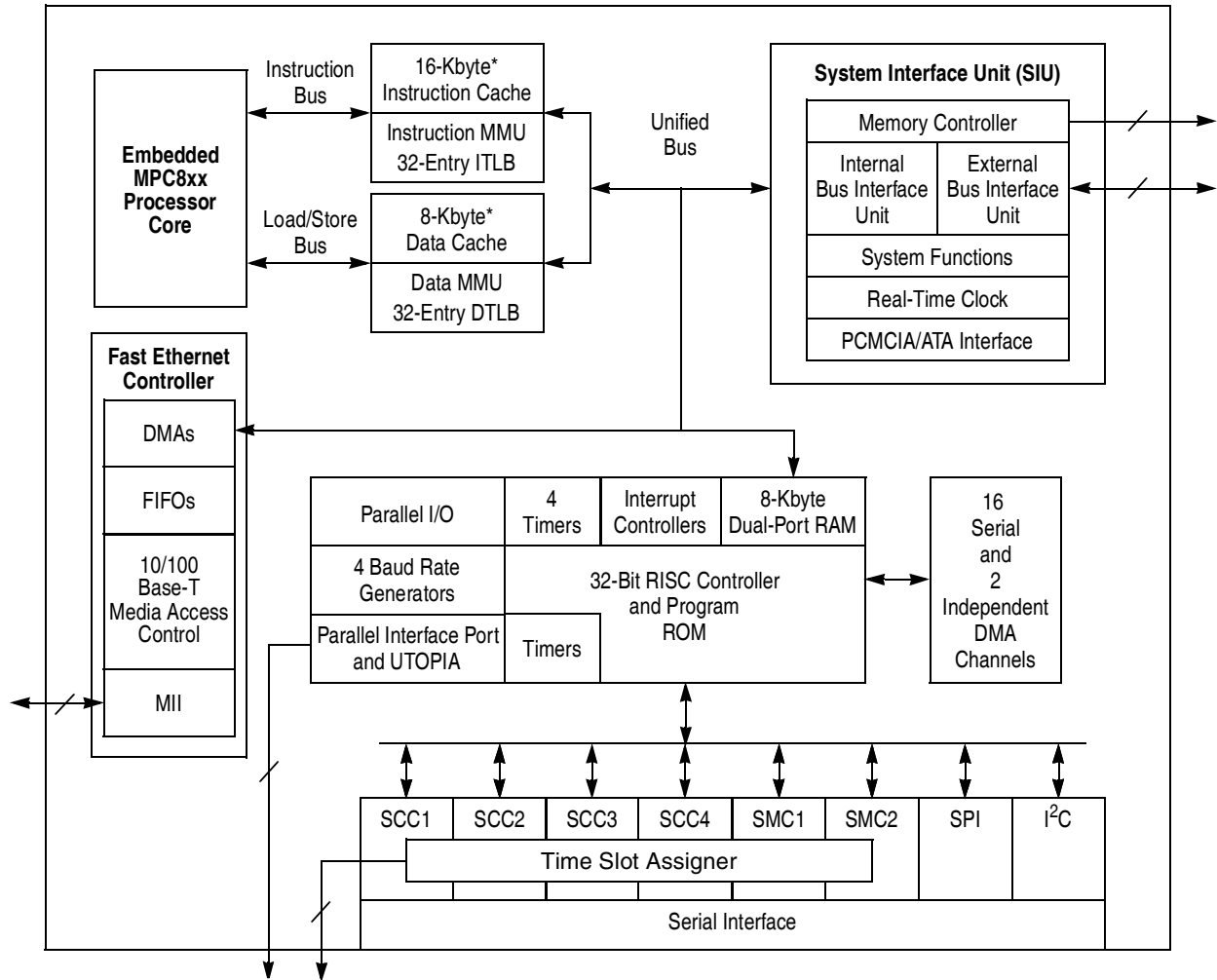
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc862pcvr80b

- Universal asynchronous receiver transmitter (UART)
- Synchronous UART
- Serial infrared (IrDA)
- Binary synchronous communication (BISYNC)
- Totally transparent (bit streams)
- Totally transparent (frame based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels) (The MPC857DSL has one SMC, SMC1 for UART)
 - UART
 - Transparent
 - General circuit interface (GCI) controller
 - Can be connected to the time-division multiplexed (TDM) channels
- One serial peripheral interface (SPI)
 - Supports master and slave modes
 - Supports multiple-master operation on the same bus
- One inter-integrated circuit (I²C) port
 - Supports master and slave modes
 - Multiple-master environment support
- Time-slot assigner (TSA) (The MPC857DSL does not have the TSA)
 - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame synchronization, clocking
 - Allows dynamic changes
 - On the MPC862P and MPC862T, can be internally connected to six serial channels (four SCCs and two SMCs); on the MPC857T, can be connected to three serial channels (one SCC and two SMCs)
- Parallel interface port (PIP)
 - Centronics interface support
 - Supports fast connection between compatible ports on MPC862/857T/857DSL or MC68360
- PCMCIA interface
 - Master (socket) interface, release 2.1 compliant
 - Supports one or two PCMCIA sockets dependent upon whether ESAR functionality is enabled
 - 8 memory or I/O windows supported
- Low power support
 - Full on—All units fully powered
 - Doze—Core functional units disabled except time base decremter, PLL, memory controller, RTC, and CPM in low-power standby

Features

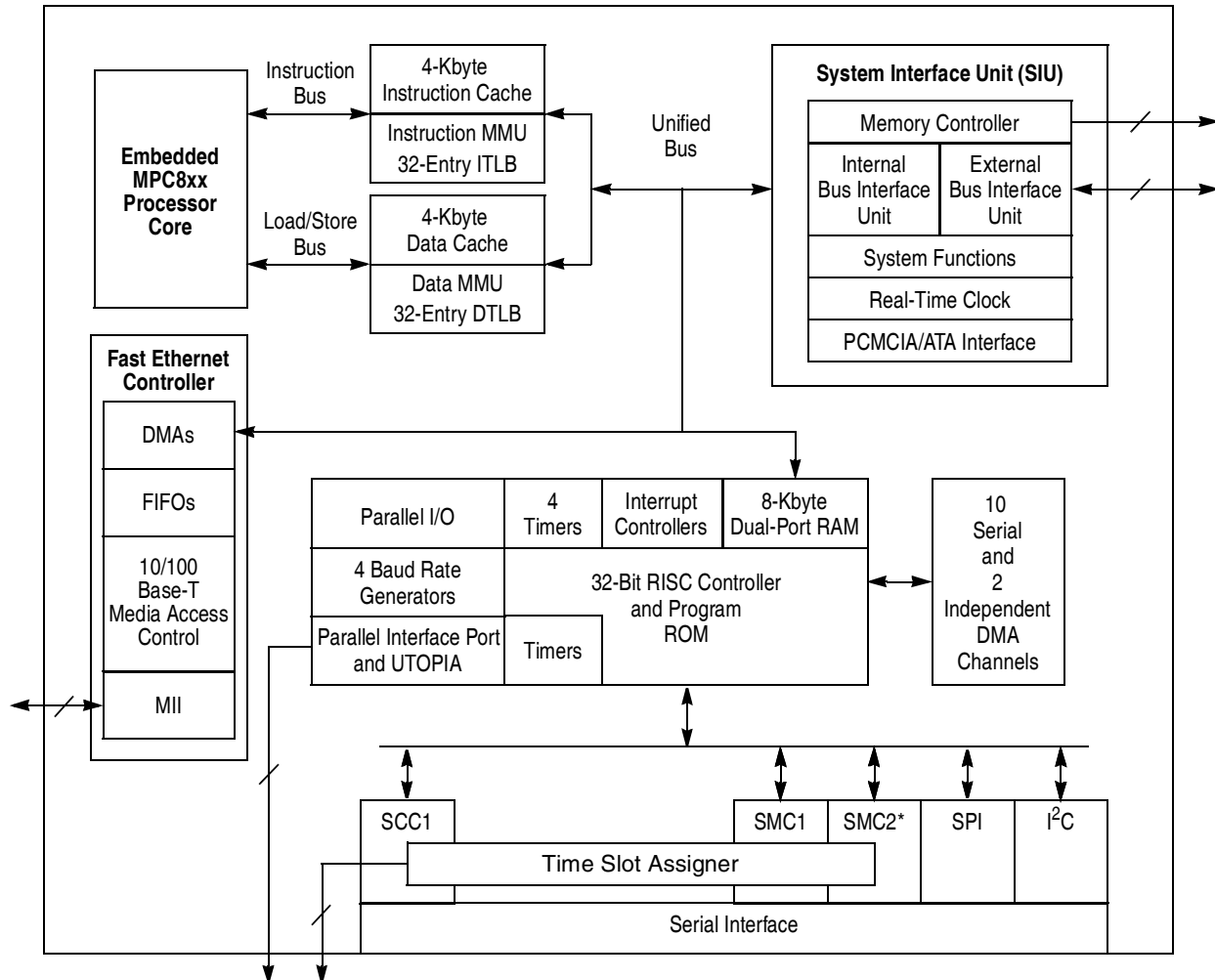
- Sleep—All units disabled except RTC, PIT, time base, and decremter with PLL active for fast wake up
- Deep sleep—All units disabled including PLL except RTC, PIT, time base, and decremter.
- Power down mode— All units powered down except PLL, RTC, PIT, time base and decremter
- Debug interface
 - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
 - Supports conditions: = ≠ < >
 - Each watchpoint can generate a break point internally
- 3.3 V operation with 5-V TTL compatibility except EXTAL and EXTCLK
- 357-pin plastic ball grid array (PBGA) package
- Operation up to 100MHz

The MPC862/857T/857DSL is comprised of three modules that each use the 32-bit internal bus: the MPC8xx core, the system integration unit (SIU), and the communication processor module (CPM). The MPC862P/862T block diagram is shown in [Figure 1](#). The MPC857T/857DSL block diagram is shown in [Figure 2](#).



*The MPC862T contains 4-Kbyte instruction cache and 4-Kbyte data cache.

Figure 1. MPC862P/862T Block Diagram



*The MPC857DSL does not contain SMC2 nor the Time Slot Assigner, and provides eight SDMA controllers.

Figure 2. MPC857T/MPC857DSL Block Diagram

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC862/857T/857DSL. [Table 2](#) provides the maximum ratings.

Table 2. Maximum Tolerated Ratings
(GND = 0 V)

Rating	Symbol	Value	Unit	Max Freq (MHz)
Supply voltage ¹	VDDH	-0.3 to 4.0	V	-
	VDDL	-0.3 to 4.0	V	-
	KAPWR	-0.3 to 4.0	V	-
	VDDSYN	-0.3 to 4.0	V	-

Table 5. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Output Low Voltage IOL = 2.0 mA (CLKOUT) IOL = 3.2 mA ³ IOL = 5.3 mA ⁴ IOL = 7.0 mA (TXD1/PA14, TXD2/PA12) IOL = 8.9 mA ($\overline{TS}$, $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{HRESET}$, $\overline{SRESET}$)	VOL	—	0.5	V

¹ $V_{IL}(\text{max})$ for the I²C interface is 0.8 V rather than the 1.5 V as specified in the I²C standard.

² Input capacitance is periodically sampled.

³ A(0:31), $\overline{TSI0}/\overline{REG}$, $\overline{TSI1}$, D(0:31), DP(0:3)/ $\overline{IRQ}$ (3:6), $\overline{RD}/\overline{WR}$, $\overline{BURST}$, $\overline{RSV}/\overline{IRQ2}$, $\overline{IP_B}(0:1)/\overline{IWP}(0:1)/\overline{VFLS}(0:1)$, $\overline{IP_B2}/\overline{IOIS16_B}/\overline{AT2}$, $\overline{IP_B3}/\overline{IWP2}/\overline{VF2}$, $\overline{IP_B4}/\overline{LWP0}/\overline{VF0}$, $\overline{IP_B5}/\overline{LWP1}/\overline{VF1}$, $\overline{IP_B6}/\overline{DSDI}/\overline{AT0}$, $\overline{IP_B7}/\overline{PTR}/\overline{AT3}$, $\overline{RXD1}/\overline{PA15}$, $\overline{RXD2}/\overline{PA13}$, $\overline{L1TXDB}/\overline{PA11}$, $\overline{L1RXDB}/\overline{PA10}$, $\overline{L1TXDA}/\overline{PA9}$, $\overline{L1RXDA}/\overline{PA8}$, $\overline{TIN1}/\overline{L1RCLKA}/\overline{BRGO1}/\overline{CLK1}/\overline{PA7}$, $\overline{BRGCLK1}/\overline{TOUT1}/\overline{CLK2}/\overline{PA6}$, $\overline{TIN2}/\overline{L1TCLKA}/\overline{BRGO2}/\overline{CLK3}/\overline{PA5}$, $\overline{TOUT2}/\overline{CLK4}/\overline{PA4}$, $\overline{TIN3}/\overline{BRGO3}/\overline{CLK5}/\overline{PA3}$, $\overline{BRGCLK2}/\overline{L1RCLKB}/\overline{TOUT3}/\overline{CLK6}/\overline{PA2}$, $\overline{TIN4}/\overline{BRGO4}/\overline{CLK7}/\overline{PA1}$, $\overline{L1TCLKB}/\overline{TOUT4}/\overline{CLK8}/\overline{PA0}$, $\overline{REJECT1}/\overline{SPISEL}/\overline{PB31}$, $\overline{SPICLK}/\overline{PB30}$, $\overline{SPIMOSI}/\overline{PB29}$, $\overline{BRGO4}/\overline{SPIMISO}/\overline{PB28}$, $\overline{BRGO1}/\overline{I2CSDA}/\overline{PB27}$, $\overline{BRGO2}/\overline{I2CSCL}/\overline{PB26}$, $\overline{SMTXD1}/\overline{PB25}$, $\overline{SMRXD1}/\overline{PB24}$, $\overline{SMSYN1}/\overline{SDACK1}/\overline{PB23}$, $\overline{SMSYN2}/\overline{SDACK2}/\overline{PB22}$, $\overline{SMTXD2}/\overline{L1CLKOB}/\overline{PB21}$, $\overline{SMRXD2}/\overline{L1CLKOA}/\overline{PB20}$, $\overline{L1ST1}/\overline{RTS1}/\overline{PB19}$, $\overline{L1ST2}/\overline{RTS2}/\overline{PB18}$, $\overline{L1ST3}/\overline{L1RQB}/\overline{PB17}$, $\overline{L1ST4}/\overline{L1RQA}/\overline{PB16}$, $\overline{BRGO3}/\overline{PB15}$, $\overline{RSTR1}/\overline{PB14}$, $\overline{L1ST1}/\overline{RTS1}/\overline{DREQ0}/\overline{PC15}$, $\overline{L1ST2}/\overline{RTS2}/\overline{DREQ1}/\overline{PC14}$, $\overline{L1ST3}/\overline{L1RQB}/\overline{PC13}$, $\overline{L1ST4}/\overline{L1RQA}/\overline{PC12}$, $\overline{CTS1}/\overline{PC11}$, $\overline{TGATE1}/\overline{CD1}/\overline{PC10}$, $\overline{CTS2}/\overline{PC9}$, $\overline{TGATE2}/\overline{CD2}/\overline{PC8}$, $\overline{CTS3}/\overline{SDACK2}/\overline{L1TSYNCB}/\overline{PC7}$, $\overline{CD3}/\overline{L1RSYNCB}/\overline{PC6}$, $\overline{CTS4}/\overline{SDACK1}/\overline{L1TSYNCA}/\overline{PC5}$, $\overline{CD4}/\overline{L1RSYNCA}/\overline{PC4}$, $\overline{PD15}/\overline{L1TSYNCA}$, $\overline{PD14}/\overline{L1RSYNCA}$, $\overline{PD13}/\overline{L1TSYNCB}$, $\overline{PD12}/\overline{L1RSYNCB}$, $\overline{PD11}/\overline{RXD3}$, $\overline{PD10}/\overline{TXD3}$, $\overline{PD9}/\overline{RXD4}$, $\overline{PD8}/\overline{TXD4}$, $\overline{PD5}/\overline{REJECT2}$, $\overline{PD6}/\overline{RTS4}$, $\overline{PD7}/\overline{RTS3}$, $\overline{PD4}/\overline{REJECT3}$, $\overline{PD3}$, $\overline{MII_MDC}$, $\overline{MII_TX_ER}$, $\overline{MII_EN}$, $\overline{MII_MDIO}$, $\overline{MII_TXD}[0:3]$.

⁴ $\overline{BDIP}/\overline{GPL_B}(5)$, $\overline{BR}$, $\overline{BG}$, $\overline{FRZ}/\overline{IRQ6}$, $\overline{CS}(0:5)$, $\overline{CS}(6)/\overline{CE}(1)_B$, $\overline{CS}(7)/\overline{CE}(2)_B$, $\overline{WE0}/\overline{BS_B0}/\overline{IORD}$, $\overline{WE1}/\overline{BS_B1}/\overline{IOWR}$, $\overline{WE2}/\overline{BS_B2}/\overline{PCOE}$, $\overline{WE3}/\overline{BS_B3}/\overline{PCWE}$, $\overline{BS_A}(0:3)$, $\overline{GPL_A0}/\overline{GPL_B0}$, $\overline{OE}/\overline{GPL_A1}/\overline{GPL_B1}$, $\overline{GPL_A}(2:3)/\overline{GPL_B}(2:3)/\overline{CS}(2:3)$, $\overline{UPWAITA}/\overline{GPL_A4}$, $\overline{UPWAITB}/\overline{GPL_B4}$, $\overline{GPL_A5}$, $\overline{ALE_A}$, $\overline{CE1_A}$, $\overline{CE2_A}$, $\overline{ALE_B}/\overline{DSCK}/\overline{AT1}$, $\overline{OP}(0:1)$, $\overline{OP2}/\overline{MODCK1}/\overline{STS}$, $\overline{OP3}/\overline{MODCK2}/\overline{DSDO}$, $\overline{BADDR}(28:30)$.

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B8a	CLKOUT to TSIZ(0:1), $\overline{\text{REG}}$, $\overline{\text{RSV}}$, AT(0:3) $\overline{\text{BDIP}}$, PTR valid (MAX = $0.25 \times B1 + 6.3$)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B8b	CLKOUT to $\overline{\text{BR}}$, $\overline{\text{BG}}$, VFSL(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS Valid ⁴ (MAX = $0.25 \times B1 + 6.3$)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/ $\overline{\text{WR}}$, BURST, D(0:31), DP(0:3), TSIZ(0:1), $\overline{\text{REG}}$, $\overline{\text{RSV}}$, AT(0:3), PTR High-Z (MAX = $0.25 \times B1 + 6.3$)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B11	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ assertion (MAX = $0.25 \times B1 + 6.0$)	7.60	13.60	6.30	12.30	5.00	11.00	3.80	11.30	ns
B11a	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = $0.00 \times B1 + 9.30$ ⁵)	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.80	ns
B12	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ negation (MAX = $0.25 \times B1 + 4.8$)	7.60	12.30	6.30	11.00	5.00	9.80	3.80	8.50	ns
B12a	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = $0.00 \times B1 + 9.00$)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B13	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ High-Z (MIN = $0.25 \times B1$)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns
B13a	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = $0.00 \times B1 + 2.5$)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to $\overline{\text{TEA}}$ assertion (MAX = $0.00 \times B1 + 9.00$)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B15	CLKOUT to $\overline{\text{TEA}}$ High-Z (MIN = $0.00 \times B1 + 2.50$)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{\text{TA}}$, $\overline{\text{BI}}$ valid to CLKOUT (setup time) (MIN = $0.00 \times B1 + 6.00$)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B16a	$\overline{\text{TEA}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid to CLKOUT (setup time) (MIN = $0.00 \times B1 + 4.5$)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	$\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$, valid to CLKOUT (setup time) ⁶ (4MIN = $0.00 \times B1 + 0.00$)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$ valid (hold time) (MIN = $0.00 \times B1 + 1.00$ ⁷)	1.00	—	1.00	—	1.00	—	2.00	—	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid (hold time) (MIN = $0.00 \times B1 + 2.00$)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) ⁸ (MIN = $0.00 \times B1 + 6.00$)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) ⁸ (MIN = $0.00 \times B1 + 1.00$ ⁹)	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) ¹⁰ (MIN = $0.00 \times B1 + 4.00$)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) ¹⁰ (MIN = $0.00 \times B1 + 2.00$)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 (MAX = $0.25 \times B1 + 6.3$)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = $0.00 \times B1 + 8.00$)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = $0.25 \times B1 + 6.3$)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = $0.375 \times B1 + 6.6$)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = $0.00 \times B1 + 8.00$)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = $0.50 \times B1 - 2.00$)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$ (0:3) asserted (MAX = $0.00 \times B1 + 9.00$)	—	9.00		9.00		9.00		9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = $0.00 \times B1 + 9.00$)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 x B1 - 2.00)	35.90	—	29.30	—	23.00	—	16.90	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B28	CLKOUT rising edge to $\overline{WE}$ (0:3) negated GPCM write access CSNT = 0 (MAX = 0.00 x B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$ (0:3) negated GPCM write access TRLX = 0, 1, CSNT = 1, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	—	14.30	—	13.00	—	11.80	—	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}$ (0:3) negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0,1, CSNT = 1, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	—	18.00	—	18.00	—	14.30	—	12.30	ns
B29	$\overline{WE}$ (0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29a	$\overline{WE}$ (0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B29b	$\overline{CS}$ negated to D(0:31), DP(0:3), High Z GPCM write access, ACS = 00, TRLX = 0,1 & CSNT = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29c	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29d	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29e	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29f	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 6.30)	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29g	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 - 6.30)	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29h	$\overline{WE}(0:3)$ negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns
B29i	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 - 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns
B30	$\overline{CS}$, $\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) Invalid GPCM write access ¹¹ (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B30a	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) Invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT = 1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B30b	$\overline{WE}(0:3)$ negated to A(0:31) Invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns

Figure 6 provides the timing for the synchronous output signals.

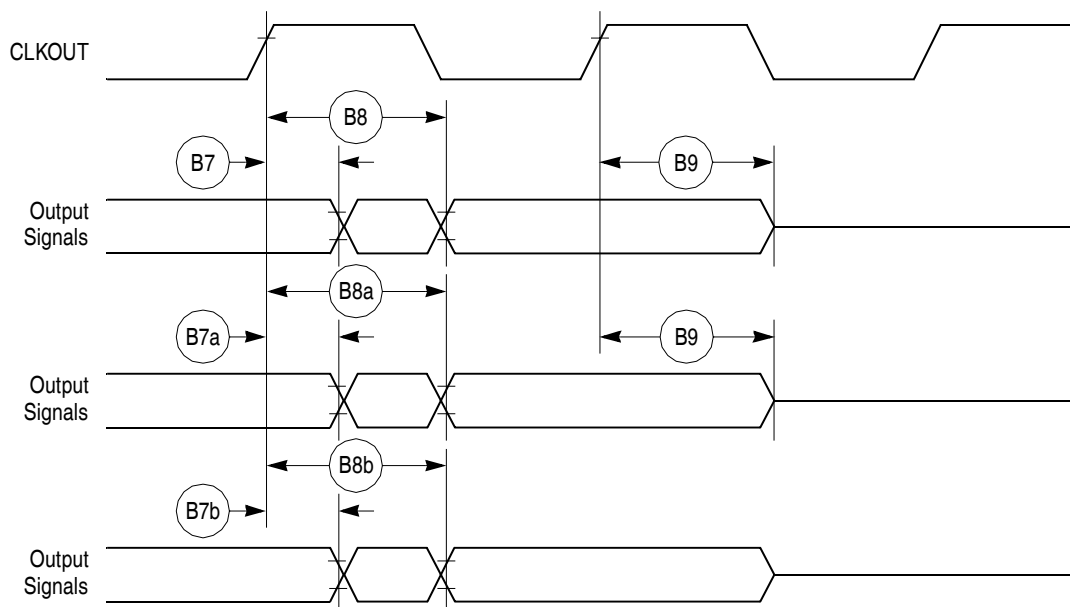


Figure 6. Synchronous Output Signals Timing

Figure 7 provides the timing for the synchronous active pull-up and open-drain output signals.

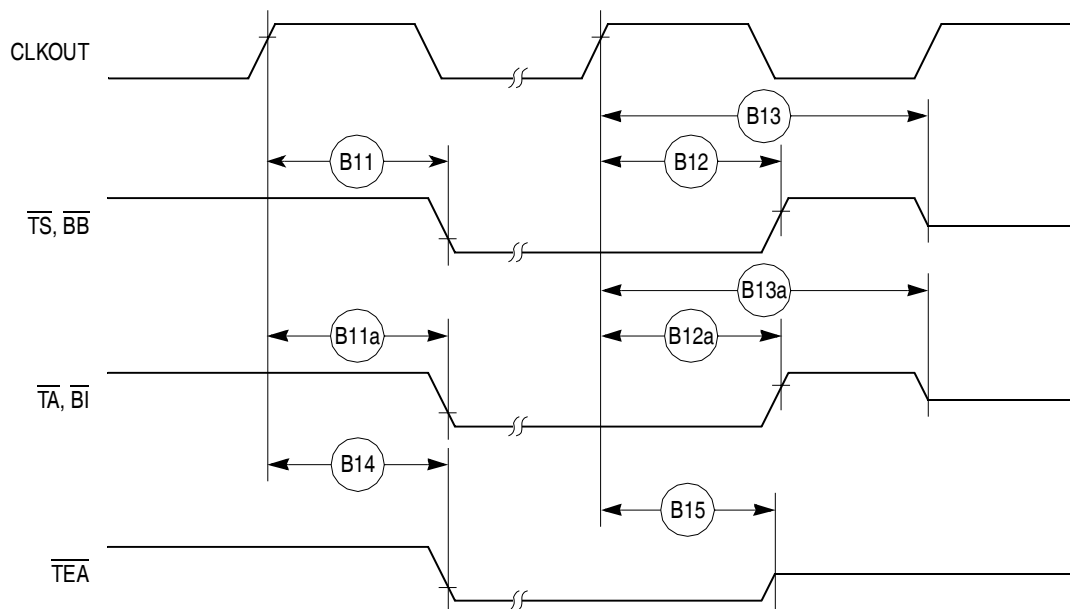


Figure 7. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

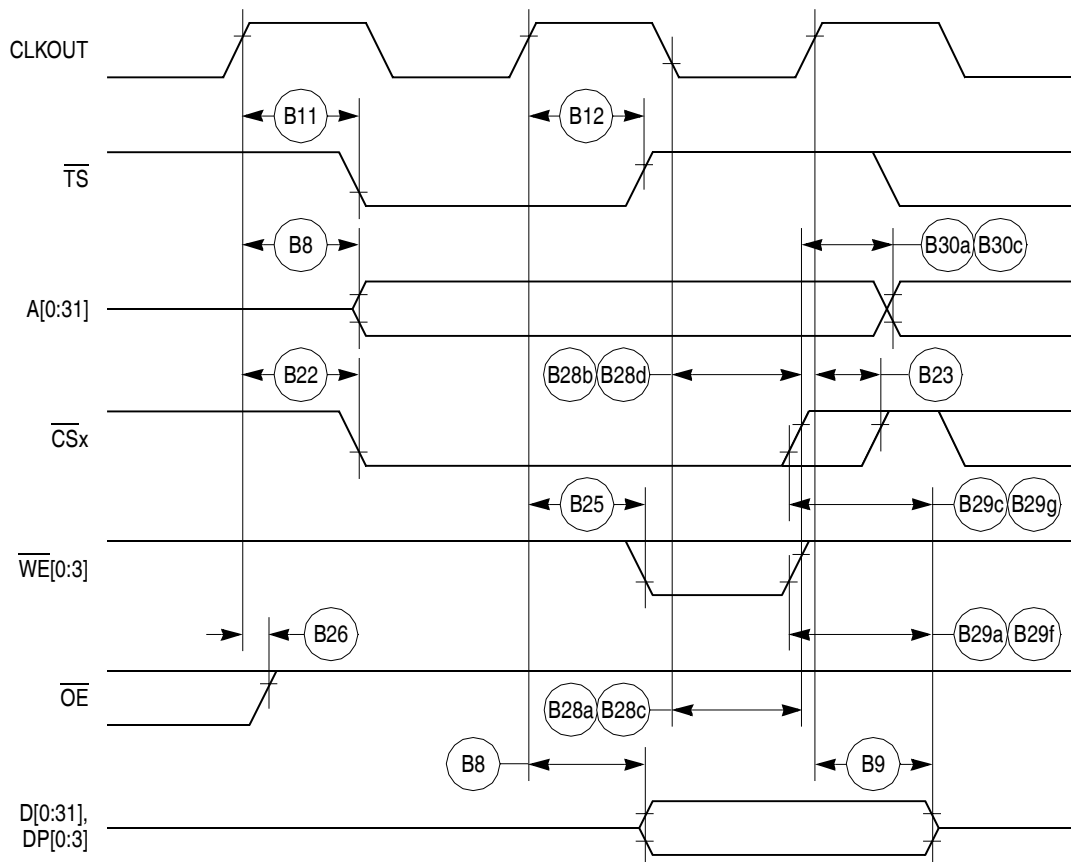


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0,1 CSNT = 1)

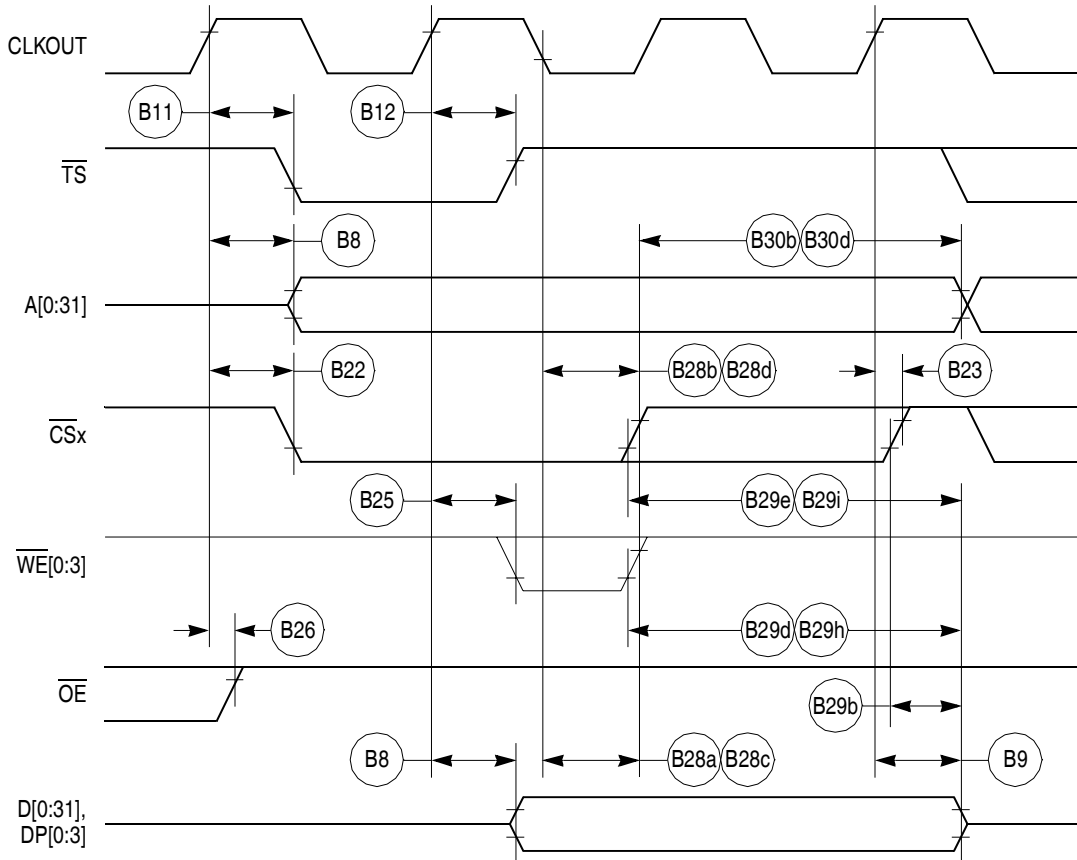


Figure 17. External Bus Write Timing (GPCM Controlled—TRLX = 0,1, CSNT = 1)

Table 12 shows the reset timing for the MPC862/857T/857DSL.

Table 12. Reset Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = $0.00 \times B1 + 20.00$)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = $0.00 \times B1 + 20.00$)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width (MIN = $17.00 \times B1$)	515.20	—	425.00	—	340.00	—	257.60	—	ns
R72	—	—	—	—	—	—	—	—	—	—
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge set up time (MIN = $15.00 \times B1 + 50.00$)	504.50	—	425.00	—	350.00	—	277.30	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time (MIN = $0.00 \times B1 + 350.00$)	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = $0.00 \times B1 + 0.00$)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = $0.00 \times B1 + 0.00$)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = $0.00 \times B1 + 25.00$)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance. (MAX = $0.00 \times B1 + 25.00$)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance. (MAX = $0.00 \times B1 + 25.00$)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK set up (MIN = $3.00 \times B1$)	90.90	—	75.00	—	60.00	—	45.50	—	ns
R81	DSDI, DSCK hold time (MIN = $0.00 \times B1 + 0.00$)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = $8.00 \times B1$)	242.40	—	200.00	—	160.00	—	121.20	—	ns

Table 19. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
83a	L1RCLK, L1TCLK width high (DSC = 1) ³	P + 10	—	ns
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC ⁴	1.00	—	L1TCLK
86	L1GR setup time ²	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

¹ The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

² These specs are valid for IDL mode only.

³ Where P = 1/CLKOUT. Thus for a 25-MHz CLKOUT rate, P = 40 ns.

⁴ These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.

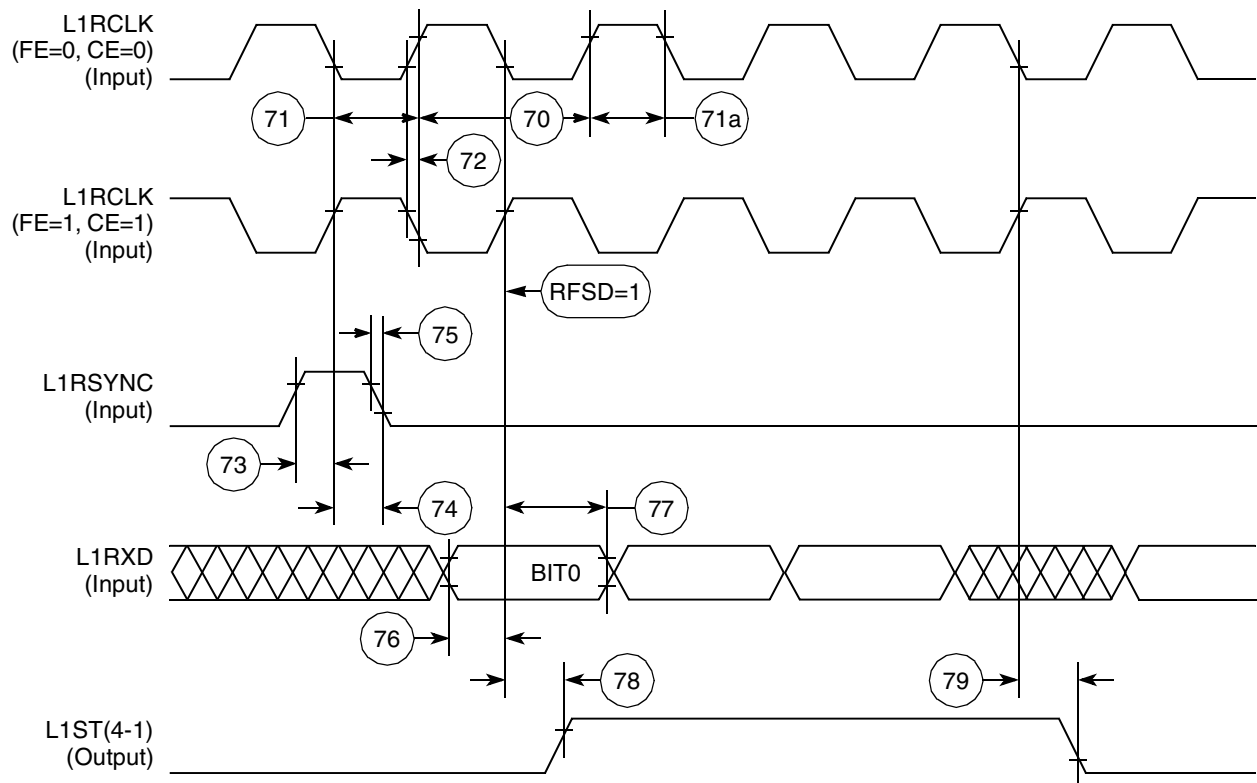


Figure 52. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

Table 22. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns
135	$\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted ²	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated ²	—	20	ns

¹ The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2/1.

² $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

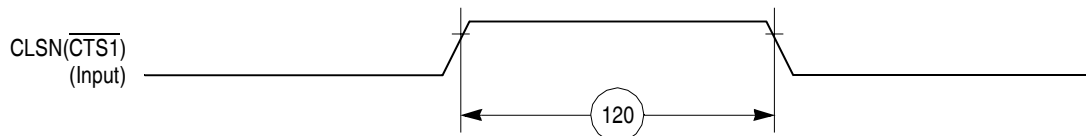


Figure 60. Ethernet Collision Timing Diagram

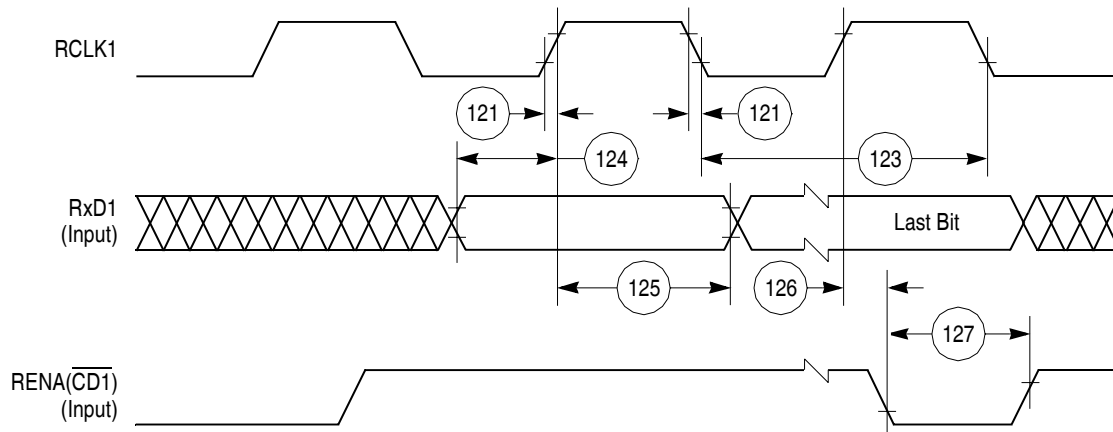


Figure 61. Ethernet Receive Timing Diagram

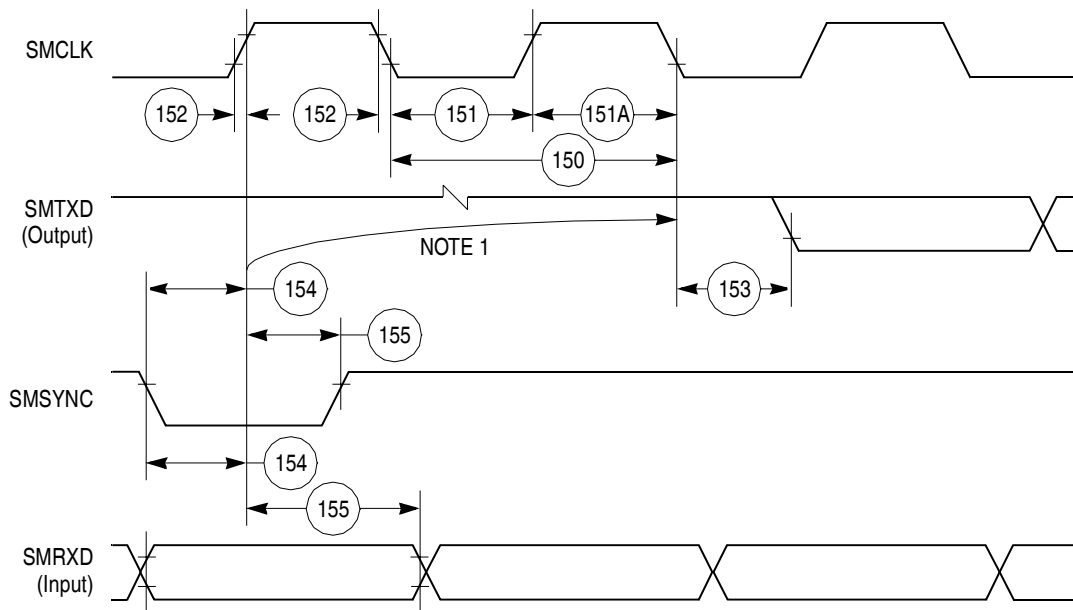
11.9 SMC Transparent AC Electrical Specifications

Table 23 provides the SMC transparent timings as shown in Figure 65.

Table 23. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period ¹	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

¹ SyncCLK must be at least twice as fast as SMCLK.



NOTE:

1. This delay is equal to an integer number of character-length clocks.

Figure 65. SMC Transparent Timing Diagram

11.12 I²C AC Electrical Specifications

Table 26 provides the I²C (SCL < 100 KHz) timings.

Table 26. I²C Timing (SCL < 100 KHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master) ¹	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	μs
203	Low period of SCL	4.7	—	μs
204	High period of SCL	4.0	—	μs
205	Start condition setup time	4.7	—	μs
206	Start condition hold time	4.0	—	μs
207	Data hold time	0	—	μs
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	μs
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	μs

¹ SCL frequency is given by $SCL = BRGCLK_frequency / ((BRG\ register + 3) * pre_scaler * 2)$.
The ratio $SyncClk/(BRGCLK/pre_scaler)$ must be greater or equal to 4/1.

Table 27 provides the I²C (SCL > 100 kHz) timings.

Table 27. I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) ¹	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	—	$1/(2.2 * fSCL)$	—	s
203	Low period of SCL	—	$1/(2.2 * fSCL)$	—	s
204	High period of SCL	—	$1/(2.2 * fSCL)$	—	s
205	Start condition setup time	—	$1/(2.2 * fSCL)$	—	s
206	Start condition hold time	—	$1/(2.2 * fSCL)$	—	s
207	Data hold time	—	0	—	s
208	Data setup time	—	$1/(40 * fSCL)$	—	s
209	SDL/SCL rise time	—	—	$1/(10 * fSCL)$	s
210	SDL/SCL fall time	—	—	$1/(33 * fSCL)$	s
211	Stop condition setup time	—	$1/2(2.2 * fSCL)$	—	s

¹ SCL frequency is given by $SCL = BrgClk_frequency / ((BRG\ register + 3) * pre_scaler * 2)$.
The ratio $SyncClk/(Brg_Clk/pre_scaler)$ must be greater or equal to 4/1.

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
IP_A6 UTPB_Split6 ² MII-TXERR	T6	Input
IP_A7 UTPB_Split7 ² MII-RXDV	T3	Input
ALE_B DSCK/AT1	J1	Bidirectional Three-state
IP_B[0:1] IWP[0:1] VFLS[0:1]	H2, J3	Bidirectional
IP_B2 IOIS16_B AT2	J2	Bidirectional Three-state
IP_B3 IWP2 VF2	G1	Bidirectional
IP_B4 LWP0 VF0	G2	Bidirectional
IP_B5 LWP1 VF1	J4	Bidirectional
IP_B6 DSDI AT0	K3	Bidirectional Three-state
IP_B7 PTR AT3	H1	Bidirectional Three-state
OP0 MII-TXD0 UtpClk_Split ²	L4	Bidirectional
OP1	L2	Output
OP2 MODCK1 STS	L1	Bidirectional
OP3 MODCK2 DSDO	M4	Bidirectional
BADDR30 REG	K4	Output
BADDR[28:29]	M3, M2	Output
AS	L3	Input

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
PC13 L1RQb L1ST3 RTS3	E18	Bidirectional
PC12 L1RQa L1ST4 RTS4	F18	Bidirectional
PC11 CTS1	J19	Bidirectional
PC10 CD1 TGATE1	K19	Bidirectional
PC9 CTS2	L18	Bidirectional
PC8 CD2 TGATE2	M18	Bidirectional
PC7 CTS3 L1TSYNCB SDACK2	M16	Bidirectional
PC6 CD3 L1RSYNCB	R19	Bidirectional
PC5 CTS4 L1TSYNCA SDACK1	T18	Bidirectional
PC4 CD4 L1RSYNCA	T17	Bidirectional
PD15 L1TSYNCA MII-RXD3 UTPB0	U17	Bidirectional
PD14 L1RSYNCA MII-RXD2 UTPB1	V19	Bidirectional
PD13 L1TSYNCB MII-RXD1 UTPB2	V18	Bidirectional

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