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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

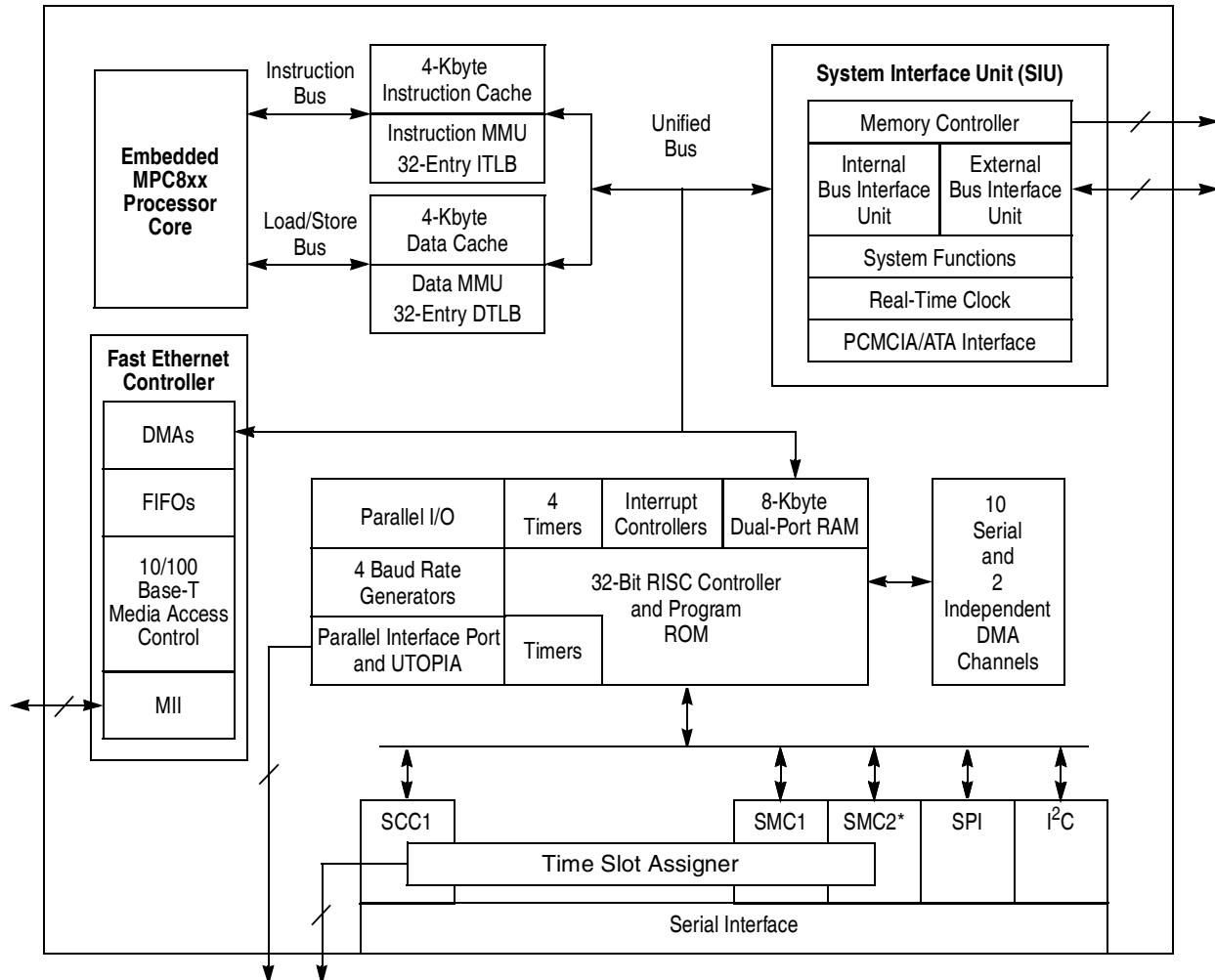
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc862pvr100b

- The MPC862/857T/857DSL provides enhanced ATM functionality over that of the MPC860SAR. The MPC862/857T/857DSL adds major new features available in “enhanced SAR” (ESAR) mode, including the following:
 - Improved operation, administration and maintenance (OAM) support
 - OAM performance monitoring (PM) support
 - Multiple APC priority levels available to support a range of traffic pace requirements
 - ATM port-to-port switching capability without the need for RAM-based microcode
 - Simultaneous MII (10/100Base-T) and UTOPIA (half-duplex) capability
 - Optional statistical cell counters per PHY
 - UTOPIA level 2 compliant interface with added FIFO buffering to reduce the total cell transmission time. (The earlier UTOPIA level 1 specification is also supported.)
 - Multi-PHY support on the MPC857T
 - Four PHY support on the MPC857DSL
 - Parameter RAM for both SPI and I²C can be relocated without RAM-based microcode
 - Supports full-duplex UTOPIA both master (ATM side) and slave (PHY side) operation using a “split” bus
 - AAL2/VBR functionality is ROM-resident
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
 - Contains complete dynamic RAM (DRAM) controller
 - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
 - Up to 30 wait states programmable per memory bank
 - Glueless interface to Page mode/EDO/SDRAM, SRAM, EPROMs, flash EPROMs, and other memory devices.
 - DRAM controller programmable to support most size and speed memory interfaces
 - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, one $\overline{\text{OE}}$ line
 - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
 - Variable block sizes (32 Kbyte–256 Mbyte)
 - Selectable write protection
 - On-chip bus arbitration logic
- General-purpose timers
 - Four 16-bit timers cascadable to be two 32-bit timers
 - Gate mode can enable/disable counting
 - Interrupt can be masked on reference match and event capture
- Fast Ethernet controller (FEC)
 - Simultaneous MII (10/100Base-T) and UTOPIA operation when using the UTOPIA multiplexed bus.

Features

- Sleep—All units disabled except RTC, PIT, time base, and decremter with PLL active for fast wake up
- Deep sleep—All units disabled including PLL except RTC, PIT, time base, and decremter.
- Power down mode— All units powered down except PLL, RTC, PIT, time base and decremter
- Debug interface
 - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
 - Supports conditions: = ≠ < >
 - Each watchpoint can generate a break point internally
- 3.3 V operation with 5-V TTL compatibility except EXTAL and EXTCLK
- 357-pin plastic ball grid array (PBGA) package
- Operation up to 100MHz

The MPC862/857T/857DSL is comprised of three modules that each use the 32-bit internal bus: the MPC8xx core, the system integration unit (SIU), and the communication processor module (CPM). The MPC862P/862T block diagram is shown in [Figure 1](#). The MPC857T/857DSL block diagram is shown in [Figure 2](#).



*The MPC857DSL does not contain SMC2 nor the Time Slot Assigner, and provides eight SDMA controllers.

Figure 2. MPC857T/MPC857DSL Block Diagram

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC862/857T/857DSL. [Table 2](#) provides the maximum ratings.

Table 2. Maximum Tolerated Ratings
(GND = 0 V)

Rating	Symbol	Value	Unit	Max Freq (MHz)
Supply voltage ¹	VDDH	-0.3 to 4.0	V	-
	VDDL	-0.3 to 4.0	V	-
	KAPWR	-0.3 to 4.0	V	-
	VDDSYN	-0.3 to 4.0	V	-

Table 5. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Output Low Voltage IOL = 2.0 mA (CLKOUT) IOL = 3.2 mA ³ IOL = 5.3 mA ⁴ IOL = 7.0 mA (TXD1/PA14, TXD2/PA12) IOL = 8.9 mA (\overline{TS} , \overline{TA} , \overline{TEA} , \overline{BI} , \overline{BB} , \overline{HRESET} , \overline{SRESET})	VOL	—	0.5	V

¹ $V_{IL}(\text{max})$ for the I²C interface is 0.8 V rather than the 1.5 V as specified in the I²C standard.

² Input capacitance is periodically sampled.

³ A(0:31), $\overline{TSI0}/\overline{REG}$, $\overline{TSI1}$, D(0:31), DP(0:3)/ \overline{IRQ} (3:6), $\overline{RD}/\overline{WR}$, \overline{BURST} , $\overline{RSV}/\overline{IRQ2}$, $\overline{IP_B}(0:1)/\overline{IWP}(0:1)/\overline{VFLS}(0:1)$, $\overline{IP_B2}/\overline{IOIS16_B}/\overline{AT2}$, $\overline{IP_B3}/\overline{IWP2}/\overline{VF2}$, $\overline{IP_B4}/\overline{LWP0}/\overline{VF0}$, $\overline{IP_B5}/\overline{LWP1}/\overline{VF1}$, $\overline{IP_B6}/\overline{DSDI}/\overline{AT0}$, $\overline{IP_B7}/\overline{PTR}/\overline{AT3}$, $\overline{RXD1}/\overline{PA15}$, $\overline{RXD2}/\overline{PA13}$, $\overline{L1TXDB}/\overline{PA11}$, $\overline{L1RXDB}/\overline{PA10}$, $\overline{L1TXDA}/\overline{PA9}$, $\overline{L1RXDA}/\overline{PA8}$, $\overline{TIN1}/\overline{L1RCLKA}/\overline{BRGO1}/\overline{CLK1}/\overline{PA7}$, $\overline{BRGCLK1}/\overline{TOUT1}/\overline{CLK2}/\overline{PA6}$, $\overline{TIN2}/\overline{L1TCLKA}/\overline{BRGO2}/\overline{CLK3}/\overline{PA5}$, $\overline{TOUT2}/\overline{CLK4}/\overline{PA4}$, $\overline{TIN3}/\overline{BRGO3}/\overline{CLK5}/\overline{PA3}$, $\overline{BRGCLK2}/\overline{L1RCLKB}/\overline{TOUT3}/\overline{CLK6}/\overline{PA2}$, $\overline{TIN4}/\overline{BRGO4}/\overline{CLK7}/\overline{PA1}$, $\overline{L1TCLKB}/\overline{TOUT4}/\overline{CLK8}/\overline{PA0}$, $\overline{REJECT1}/\overline{SPISEL}/\overline{PB31}$, $\overline{SPICLK}/\overline{PB30}$, $\overline{SPIMOSI}/\overline{PB29}$, $\overline{BRGO4}/\overline{SPIMISO}/\overline{PB28}$, $\overline{BRGO1}/\overline{I2CSDA}/\overline{PB27}$, $\overline{BRGO2}/\overline{I2CSCL}/\overline{PB26}$, $\overline{SMTXD1}/\overline{PB25}$, $\overline{SMRXD1}/\overline{PB24}$, $\overline{SMSYN1}/\overline{SDACK1}/\overline{PB23}$, $\overline{SMSYN2}/\overline{SDACK2}/\overline{PB22}$, $\overline{SMTXD2}/\overline{L1CLKOB}/\overline{PB21}$, $\overline{SMRXD2}/\overline{L1CLKOA}/\overline{PB20}$, $\overline{L1ST1}/\overline{RTS1}/\overline{PB19}$, $\overline{L1ST2}/\overline{RTS2}/\overline{PB18}$, $\overline{L1ST3}/\overline{L1RQB}/\overline{PB17}$, $\overline{L1ST4}/\overline{L1RQA}/\overline{PB16}$, $\overline{BRGO3}/\overline{PB15}$, $\overline{RSTR1}/\overline{PB14}$, $\overline{L1ST1}/\overline{RTS1}/\overline{DREQ0}/\overline{PC15}$, $\overline{L1ST2}/\overline{RTS2}/\overline{DREQ1}/\overline{PC14}$, $\overline{L1ST3}/\overline{L1RQB}/\overline{PC13}$, $\overline{L1ST4}/\overline{L1RQA}/\overline{PC12}$, $\overline{CTS1}/\overline{PC11}$, $\overline{TGATE1}/\overline{CD1}/\overline{PC10}$, $\overline{CTS2}/\overline{PC9}$, $\overline{TGATE2}/\overline{CD2}/\overline{PC8}$, $\overline{CTS3}/\overline{SDACK2}/\overline{L1TSYNCB}/\overline{PC7}$, $\overline{CD3}/\overline{L1RSYNCB}/\overline{PC6}$, $\overline{CTS4}/\overline{SDACK1}/\overline{L1TSYNCA}/\overline{PC5}$, $\overline{CD4}/\overline{L1RSYNCA}/\overline{PC4}$, $\overline{PD15}/\overline{L1TSYNCA}$, $\overline{PD14}/\overline{L1RSYNCA}$, $\overline{PD13}/\overline{L1TSYNCB}$, $\overline{PD12}/\overline{L1RSYNCB}$, $\overline{PD11}/\overline{RXD3}$, $\overline{PD10}/\overline{TXD3}$, $\overline{PD9}/\overline{RXD4}$, $\overline{PD8}/\overline{TXD4}$, $\overline{PD5}/\overline{REJECT2}$, $\overline{PD6}/\overline{RTS4}$, $\overline{PD7}/\overline{RTS3}$, $\overline{PD4}/\overline{REJECT3}$, $\overline{PD3}$, $\overline{MII_MDC}$, $\overline{MII_TX_ER}$, $\overline{MII_EN}$, $\overline{MII_MDIO}$, $\overline{MII_TXD}[0:3]$.

⁴ $\overline{BDIP}/\overline{GPL_B}(5)$, \overline{BR} , \overline{BG} , $\overline{FRZ}/\overline{IRQ6}$, $\overline{CS}(0:5)$, $\overline{CS}(6)/\overline{CE}(1)_B$, $\overline{CS}(7)/\overline{CE}(2)_B$, $\overline{WE0}/\overline{BS_B0}/\overline{IORD}$, $\overline{WE1}/\overline{BS_B1}/\overline{IOWR}$, $\overline{WE2}/\overline{BS_B2}/\overline{PCOE}$, $\overline{WE3}/\overline{BS_B3}/\overline{PCWE}$, $\overline{BS_A}(0:3)$, $\overline{GPL_A0}/\overline{GPL_B0}$, $\overline{OE}/\overline{GPL_A1}/\overline{GPL_B1}$, $\overline{GPL_A}(2:3)/\overline{GPL_B}(2:3)/\overline{CS}(2:3)$, $\overline{UPWAITA}/\overline{GPL_A4}$, $\overline{UPWAITB}/\overline{GPL_B4}$, $\overline{GPL_A5}$, $\overline{ALE_A}$, $\overline{CE1_A}$, $\overline{CE2_A}$, $\overline{ALE_B}/\overline{DSCK}/\overline{AT1}$, $\overline{OP}(0:1)$, $\overline{OP2}/\overline{MODCK1}/\overline{STS}$, $\overline{OP3}/\overline{MODCK2}/\overline{DSDO}$, $\overline{BADDR}(28:30)$.

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ = junction-to-case thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta CA}$ = case-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature; see [Figure 3](#).

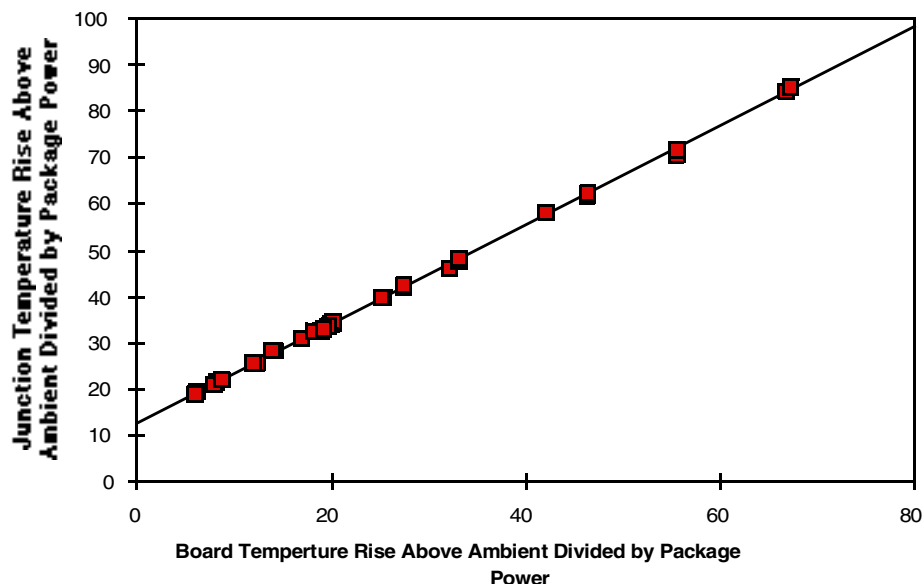


Figure 3. Effect of Board Temperature Rise on Thermal Behavior

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B17a	CLKOUT to \overline{KR} , \overline{RETRY} , \overline{CR} valid (hold time) (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) ⁸ (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) ⁸ (MIN = 0.00 x B1 + 1.00 ⁹)	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) ¹⁰ (MIN = 0.00 x B1 + 4.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) ¹⁰ (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to \overline{CS} asserted GPCM ACS = 00 (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22a	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 x B1 + 8.00)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22c	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B23	CLKOUT rising edge to \overline{CS} negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = 0.00 x B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B24a	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to \overline{OE} , \overline{WE} (0:3) asserted (MAX = 0.00 x B1 + 9.00)	—	9.00		9.00		9.00		9.00	ns
B26	CLKOUT rising edge to \overline{OE} negated (MAX = 0.00 x B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns

Figure 10 provides the timing for the input data controlled by the UPM for data beats where $DLT3 = 1$ in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

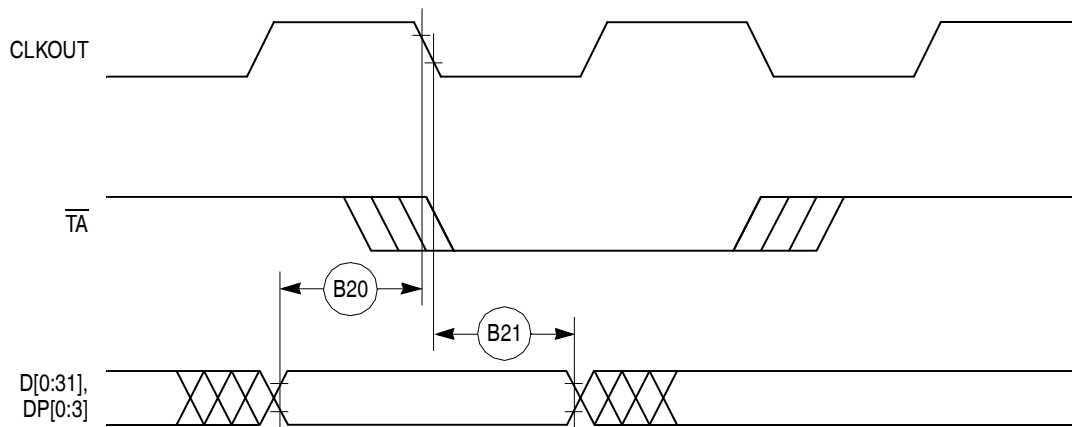


Figure 10. Input Data Timing when Controlled by UPM in the Memory Controller and $DLT3 = 1$

Figure 11 through Figure 14 provide the timing for the external bus read controlled by various GPCM factors.

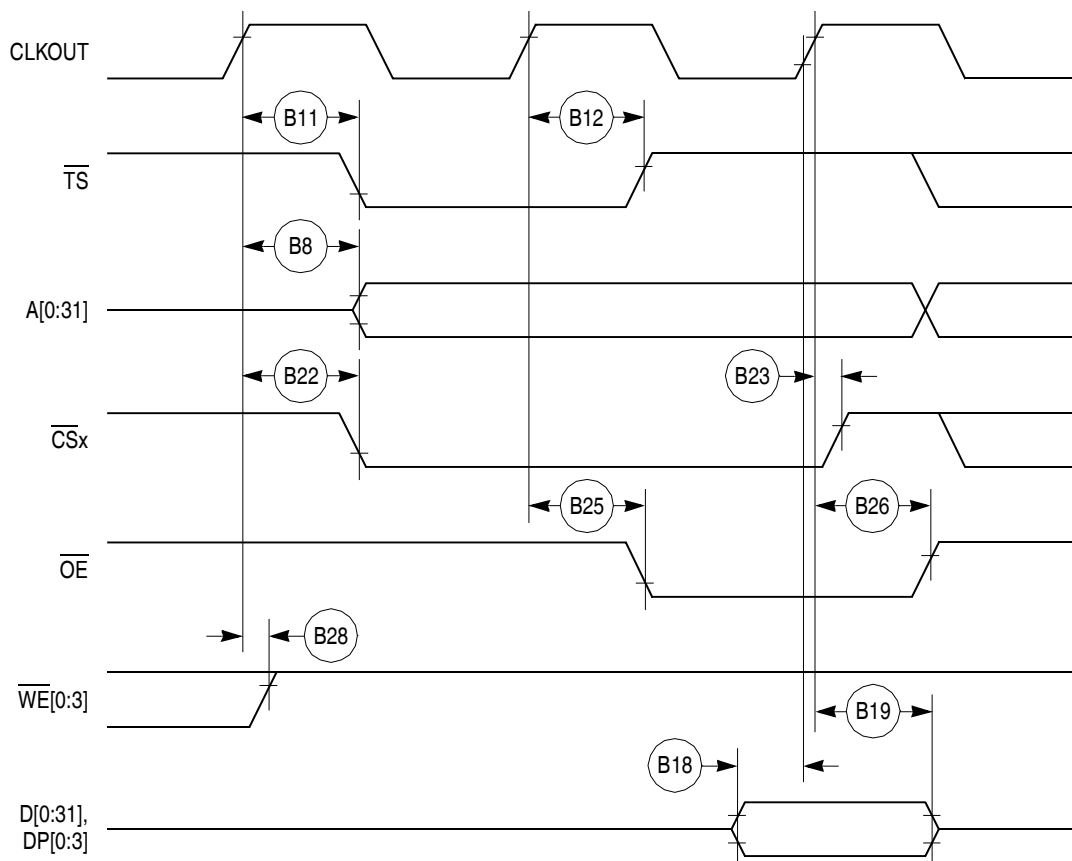
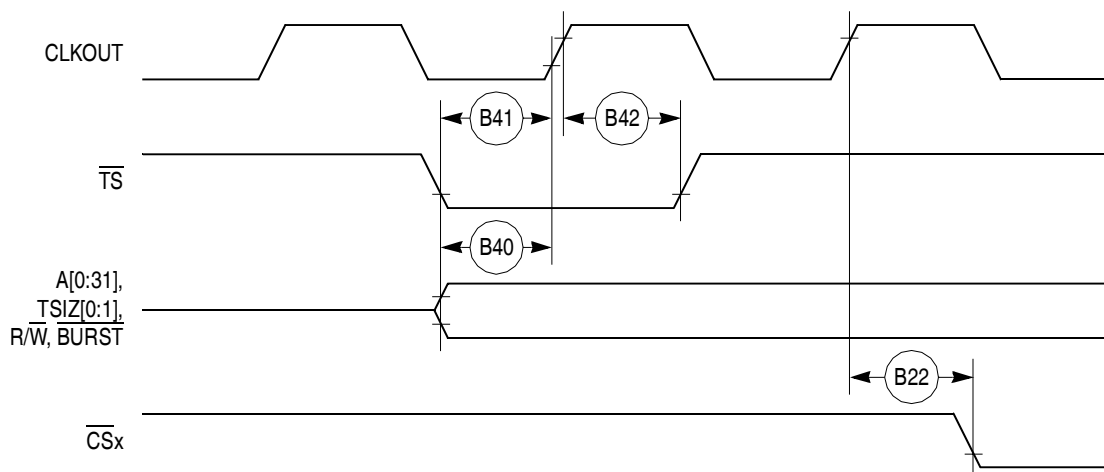


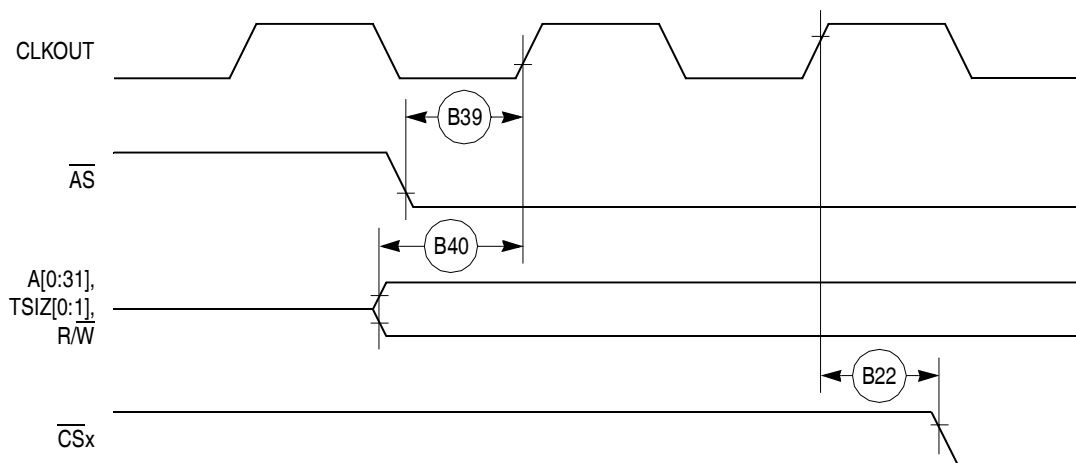
Figure 11. External Bus Read Timing (GPCM Controlled— $ACS = 00$)

Figure 21 provides the timing for the synchronous external master access controlled by the GPCM.



**Figure 21. Synchronous External Master Access Timing
(GPCM Handled ACS = 00)**

Figure 22 provides the timing for the asynchronous external master memory access controlled by the GPCM.



**Figure 22. Asynchronous External Master Memory Access Timing
(GPCM Controlled—ACS = 00)**

Figure 23 provides the timing for the asynchronous external master control signals negation.

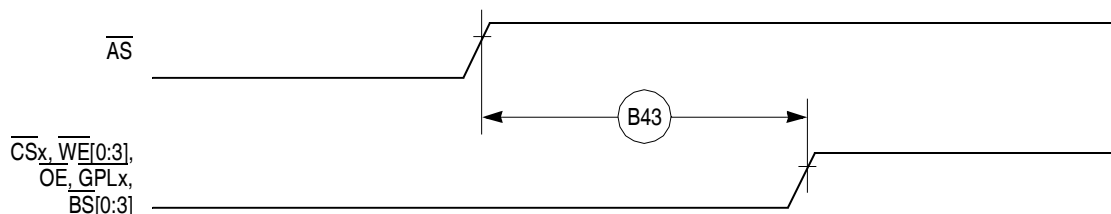


Figure 23. Asynchronous External Master—Control Signals Negation Timing

Figure 26 provides the PCMCIA access cycle timing for the external bus read.

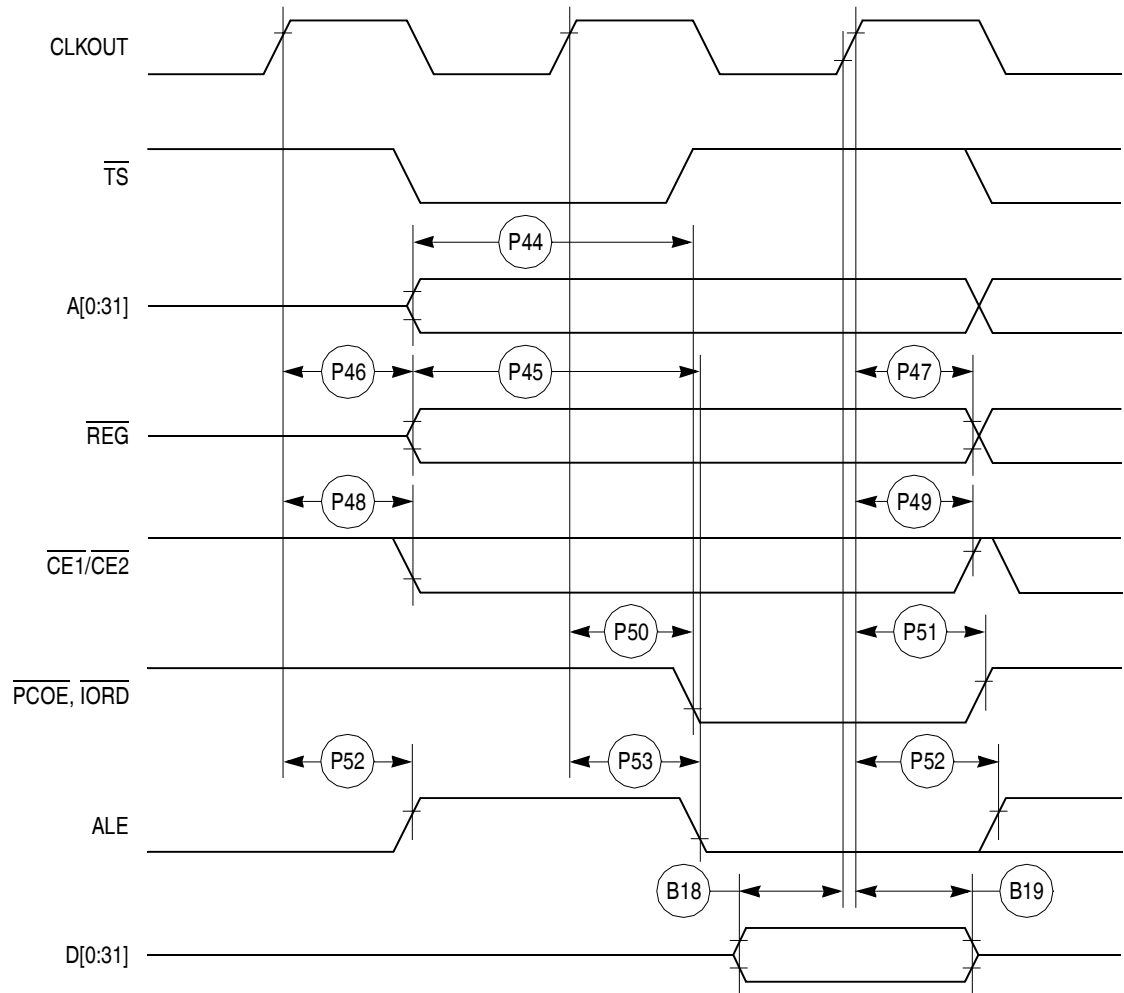


Figure 26. PCMCIA Access Cycles Timing External Bus Read

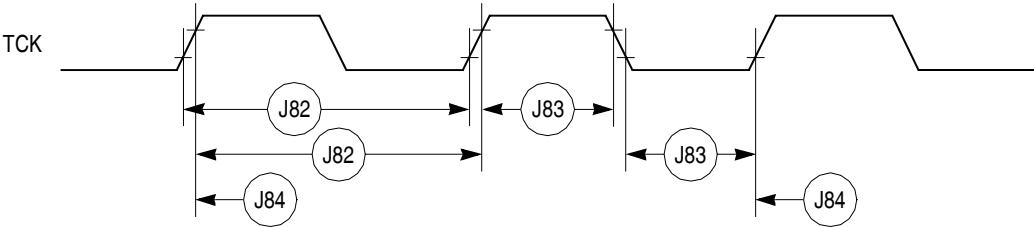


Figure 36. JTAG Test Clock Input Timing

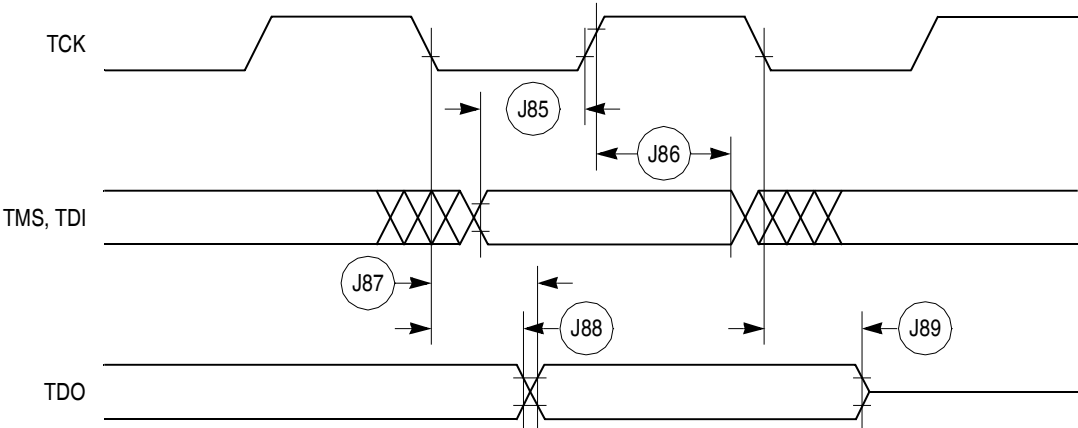


Figure 37. JTAG Test Access Port Timing Diagram

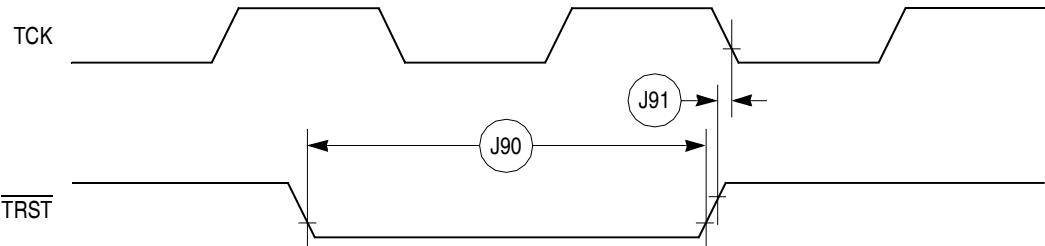


Figure 38. JTAG $\overline{\text{TRST}}$ Timing Diagram

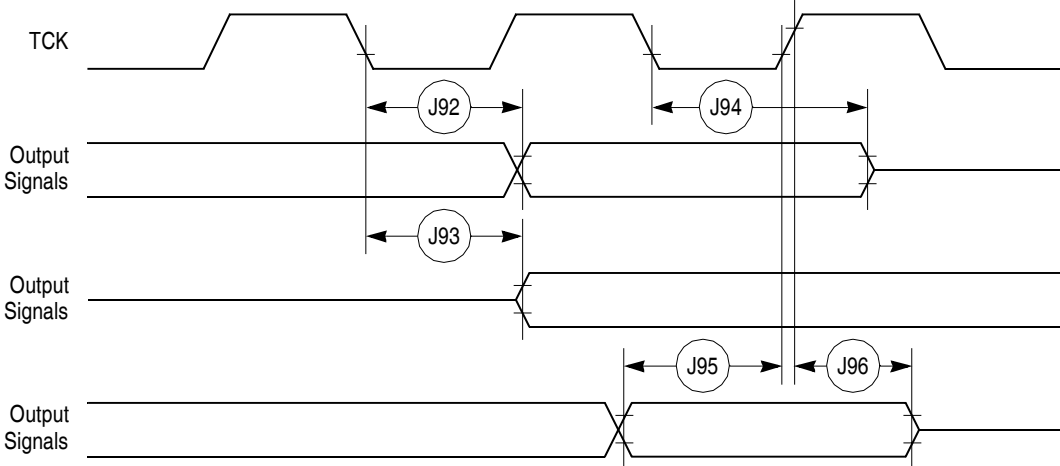


Figure 39. Boundary Scan (JTAG) Timing Diagram

11.4 Baud Rate Generator AC Electrical Specifications

Table 17 provides the baud rate generator timings as shown in Figure 50.

Table 17. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

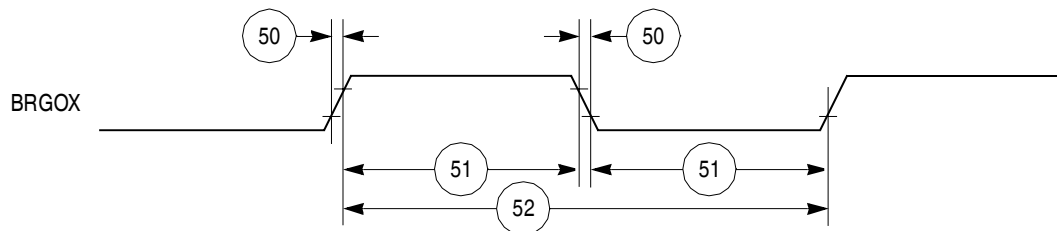


Figure 50. Baud Rate Generator Timing Diagram

11.5 Timer AC Electrical Specifications

Table 18 provides the general-purpose timer timings as shown in Figure 51.

Table 18. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/ $\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/ $\overline{\text{TGATE}}$ low time	1	—	clk
63	TIN/ $\overline{\text{TGATE}}$ high time	2	—	clk
64	TIN/ $\overline{\text{TGATE}}$ cycle time	3	—	clk
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

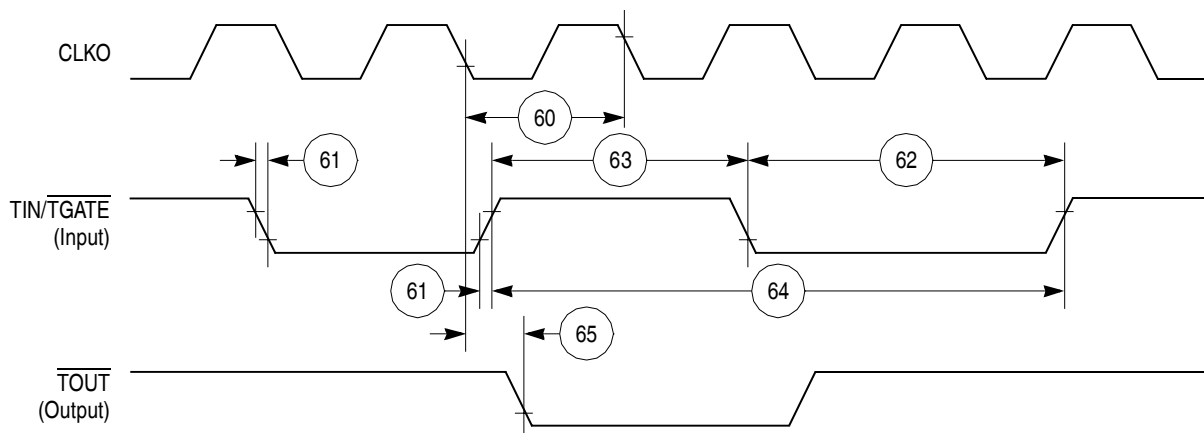


Figure 51. CPM General-Purpose Timers Timing Diagram

11.6 Serial Interface AC Electrical Specifications

Table 19 provides the serial interface timings as shown in Figure 52 through Figure 56.

Table 19. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLK, L1TCLK frequency (DSC = 0) ^{1, 2}	—	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0) ²	P + 10	—	ns
71a	L1RCLK, L1TCLK width high (DSC = 0) ³	P + 10	—	ns
72	L1TXD, L1ST(1–4), $\overline{\text{L1RQ}}$, L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20.00	—	ns
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1–4) valid ⁴	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1–4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1–4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid ⁴	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC = 1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC = 1)	P + 10	—	ns

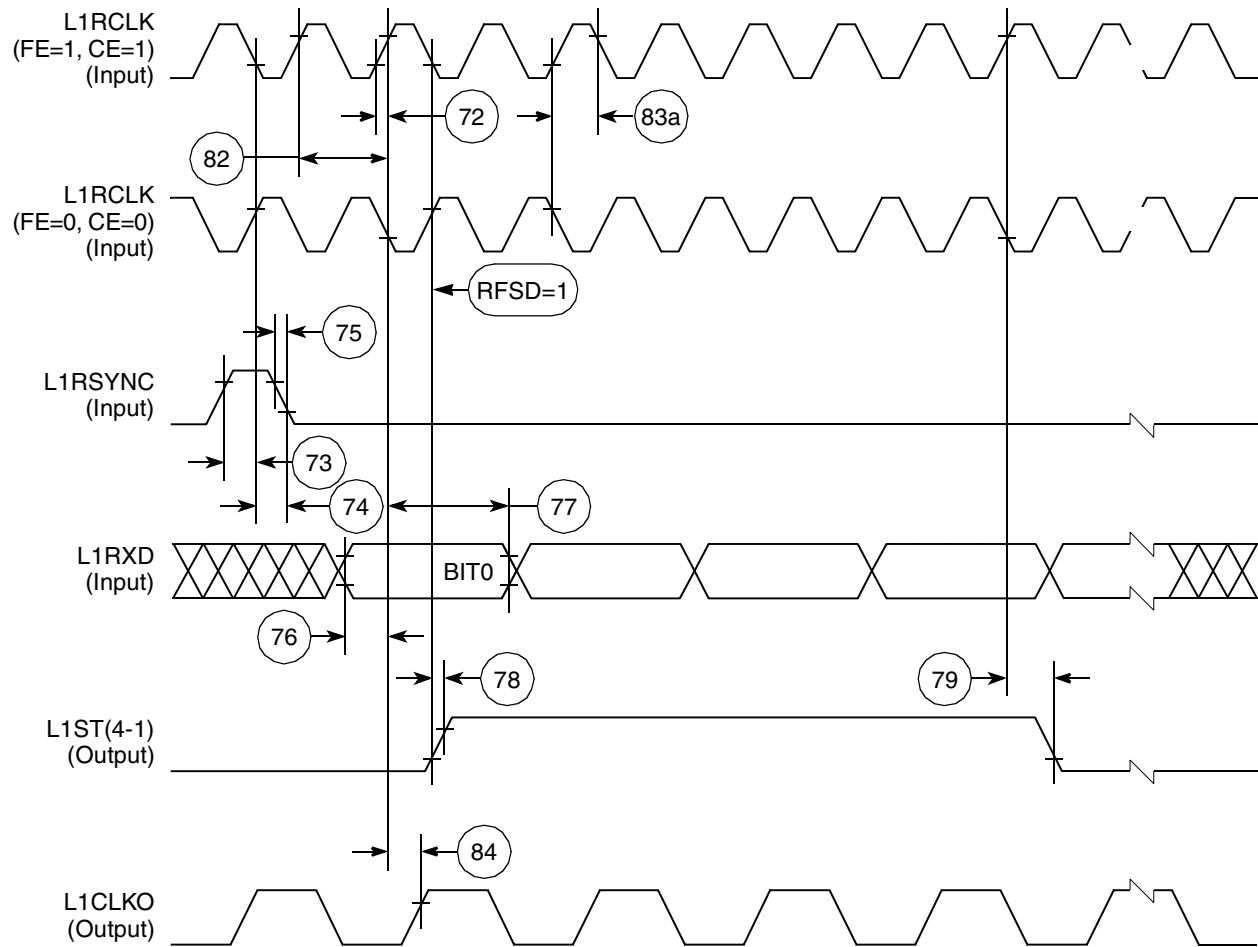


Figure 53. SI Receive Timing with Double-Speed Clocking (DSC = 1)

11.7 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

Table 20. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 width high ¹	1/SYNCCLK	—	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK +5	—	ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	—	ns
107	RXD1 hold time from RCLK1 rising edge ²	5.00	—	ns
108	$\overline{\text{CD1}}$ setup Time to RCLK1 rising edge	5.00	—	ns

¹ The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 frequency ¹	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge ²	0.00	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	40.00	—	ns

¹ The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 3/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

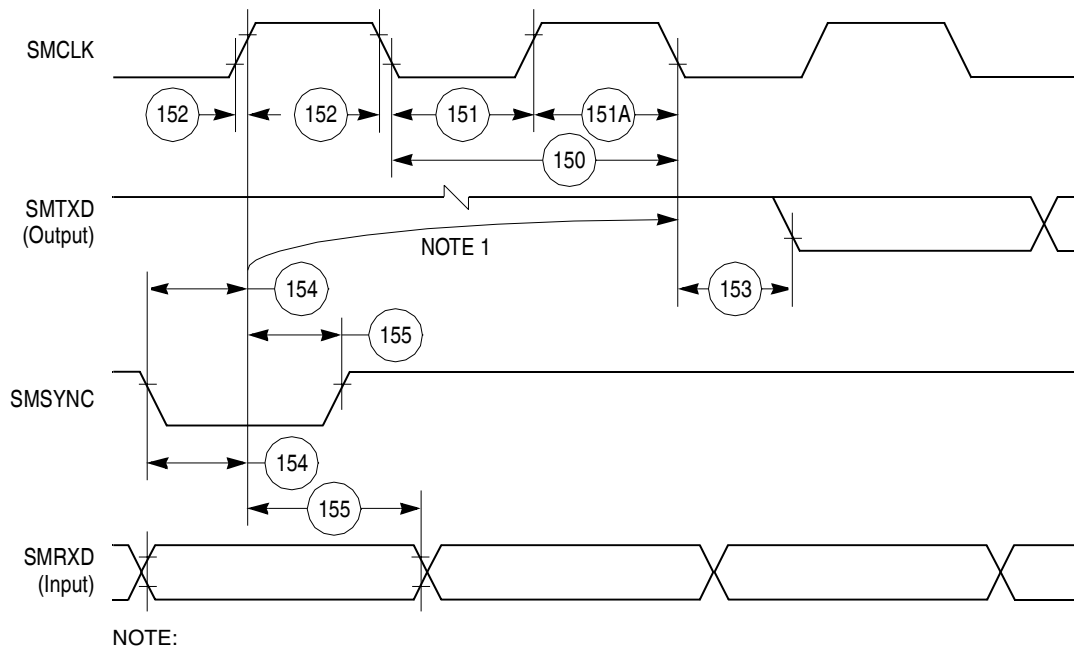
11.9 SMC Transparent AC Electrical Specifications

Table 23 provides the SMC transparent timings as shown in Figure 65.

Table 23. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period ¹	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

¹ SyncCLK must be at least twice as fast as SMCLK.



NOTE:

1. This delay is equal to an integer number of character-length clocks.

Figure 65. SMC Transparent Timing Diagram

Figure 71 shows signal timings during UTOPIA receive operations.

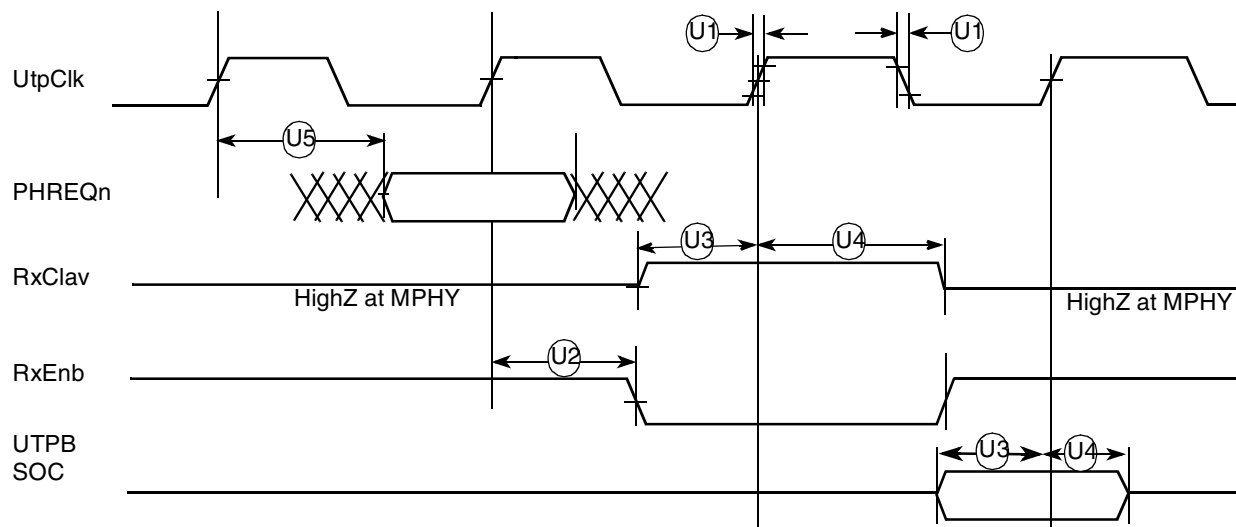


Figure 71. UTOPIA Receive Timing

Figure 72 shows signal timings during UTOPIA transmit operations.

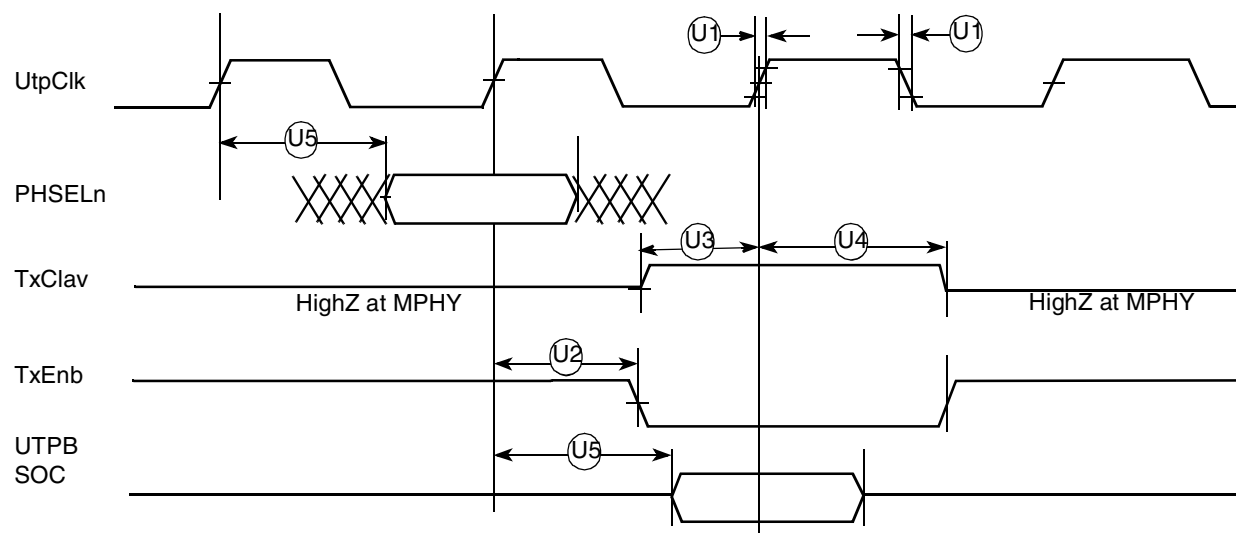


Figure 72. UTOPIA Transmit Timing

13 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Furthermore, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

Table 35 contains a list of the MPC862 input and output signals and shows multiplexing and pin assignments.

Table 35. Pin Assignments

Name	Pin Number	Type
A[0:31]	B19, B18, A18, C16, B17, A17, B16, A16, D15, C15, B15, A15, C14, B14, A14, D12, C13, B13, D9, D11, C12, B12, B10, B11, C11, D10, C10, A13, A10, A12, A11, A9	Bidirectional Three-state
TSIZ0 REG	B9	Bidirectional Three-state
TSIZ1	C9	Bidirectional Three-state
RD/WR	B2	Bidirectional Three-state
BURST	F1	Bidirectional Three-state
BDIP GPL_B5	D2	Output
TS	F3	Bidirectional Active Pull-up
TA	C2	Bidirectional Active Pull-up
TEA	D1	Open-drain
BI	E3	Bidirectional Active Pull-up
IRQ2 RSV	H3	Bidirectional Three-state
IRQ4 KR RETRY SPKROUT	K1	Bidirectional Three-state
CR IRQ3	F2	Input
D[0:31]	W14, W12, W11, W10, W13, W9, W7, W6, U13, T11, V11, U11, T13, V13, V10, T10, U10, T12, V9, U9, V8, U8, T9, U12, V7, T8, U7, V12, V6, W5, U6, T7	Bidirectional Three-state
DP0 IRQ3	V3	Bidirectional Three-state
DP1 IRQ4	V5	Bidirectional Three-state
DP2 IRQ5	W4	Bidirectional Three-state
DP3 IRQ6	V4	Bidirectional Three-state

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
$\overline{\text{BR}}$	G4	Bidirectional
$\overline{\text{BG}}$	E2	Bidirectional
$\overline{\text{BB}}$	E1	Bidirectional Active Pull-up
$\overline{\text{FRZ}}$ $\overline{\text{IRQ6}}$	G3	Bidirectional
$\overline{\text{IRQ0}}$	V14	Input
$\overline{\text{IRQ1}}$	U14	Input
$\overline{\text{M_TX_CLK}}$ $\overline{\text{IRQ7}}$	W15	Input
$\overline{\text{CS}}[0:5]$	C3, A2, D4, E4, A4, B4	Output
$\overline{\text{CS6}}$ $\overline{\text{CE1_B}}$	D5	Output
$\overline{\text{CS7}}$ $\overline{\text{CE2_B}}$	C4	Output
$\overline{\text{WE0}}$ $\overline{\text{BS_B0}}$ $\overline{\text{IORD}}$	C7	Output
$\overline{\text{WE1}}$ $\overline{\text{BS_B1}}$ $\overline{\text{IOWR}}$	A6	Output
$\overline{\text{WE2}}$ $\overline{\text{BS_B2}}$ $\overline{\text{PCOE}}$	B6	Output
$\overline{\text{WE3}}$ $\overline{\text{BS_B3}}$ $\overline{\text{PCWE}}$	A5	Output
$\overline{\text{BS_A}}[0:3]$	D8, C8, A7, B8	Output
$\overline{\text{GPL_A0}}$ $\overline{\text{GPL_B0}}$	D7	Output
$\overline{\text{OE}}$ $\overline{\text{GPL_A1}}$ $\overline{\text{GPL_B1}}$	C6	Output
$\overline{\text{GPL_A}}[2:3]$ $\overline{\text{GPL_B}}[2:3]$ $\overline{\text{CS}}[2-3]$	B5, C5	Output
$\overline{\text{UPWAITA}}$ $\overline{\text{GPL_A4}}$	C1	Bidirectional
$\overline{\text{UPWAITB}}$ $\overline{\text{GPL_B4}}$	B1	Bidirectional

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
PC13 L1RQb L1ST3 RTS3	E18	Bidirectional
PC12 L1RQa L1ST4 RTS4	F18	Bidirectional
PC11 CTS1	J19	Bidirectional
PC10 CD1 TGATE1	K19	Bidirectional
PC9 CTS2	L18	Bidirectional
PC8 CD2 TGATE2	M18	Bidirectional
PC7 CTS3 L1TSYNCB SDACK2	M16	Bidirectional
PC6 CD3 L1RSYNCB	R19	Bidirectional
PC5 CTS4 L1TSYNCA SDACK1	T18	Bidirectional
PC4 CD4 L1RSYNCA	T17	Bidirectional
PD15 L1TSYNCA MII-RXD3 UTPB0	U17	Bidirectional
PD14 L1RSYNCA MII-RXD2 UTPB1	V19	Bidirectional
PD13 L1TSYNCB MII-RXD1 UTPB2	V18	Bidirectional

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
TRST	G19	Input
TDO DSDO	G17	Output
M_CRS	B7	Input
M_MDIO	H18	Bidirectional
M_TXEN	V15	Output
M_COL	H4	Input
KAPWR	R1	Power
GND	F6, F7, F8, F9, F10, F11, F12, F13, F14, G6, G7, G8, G9, G10, G11, G12, G13, G14, H6, H7, H8, H9, H10, H11, H12, H13, H14, J6, J7, J8, J9, J10, J11, J12, J13, J14, K6, K7, K8, K9, K10, K11, K12, K13, K14, L6, L7, L8, L9, L10, L11, L12, L13, L14, M6, M7, M8, M9, M10, M11, M12, M13, M14, N6, N7, N8, N9, N10, N11, N12, N13, N14, P6, P7, P8, P9, P10, P11, P12, P13, P14	Power
VDDL	A8, M1, W8, H19, F4, F16, P4, P16	Power
VDDH	E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P5, P15, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, T14	Power
N/C	D6, D13, D14, U2, V2	No-connect

¹ Classic SAR mode only

² ESAR mode only

14.2 Mechanical Dimensions of the PBGA Package

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to *Plastic Ball Grid Array Application Note* (order number: AN1231/D) available from your local Freescale sales office. [Figure 78](#) shows the mechanical dimensions of the PBGA package.