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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc862pvr80b

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC862/857T/857DSL.

Table 3. MPC862/857T/857DSL Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction to ambient [1]	Natural Convection	Single layer board (1s)	$R_{\theta JA}$ [2]	37	°C/W
		Four layer board (2s2p)	$R_{\theta JMA}$ [3]	23	
	Air flow (200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$ [3]	30	
		Four layer board (2s2p)	$R_{\theta JMA}$ [3]	19	
Junction to board [4]			$R_{\theta JB}$	13	
Junction to case [5]			$R_{\theta JC}$	6	
Junction to package top [6]	Natural Convection		Ψ_{JT}	2	
	Air flow (200 ft/min)		Ψ_{JT}	2	

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5 Power Dissipation

Table 4 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice bus speed.

Table 4. Power Dissipation (P_D)

Die Revision	Frequency	Typical [1]	Maximum [2]	Unit
0 (1:1 Mode)	50 MHz	656	735	mW
	66 MHz	TBD	TBD	mW
A.1, B.0 (1:1 Mode)	50 MHz	630	760	mW
	66 MHz	890	1000	mW

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature; see Figure 3.

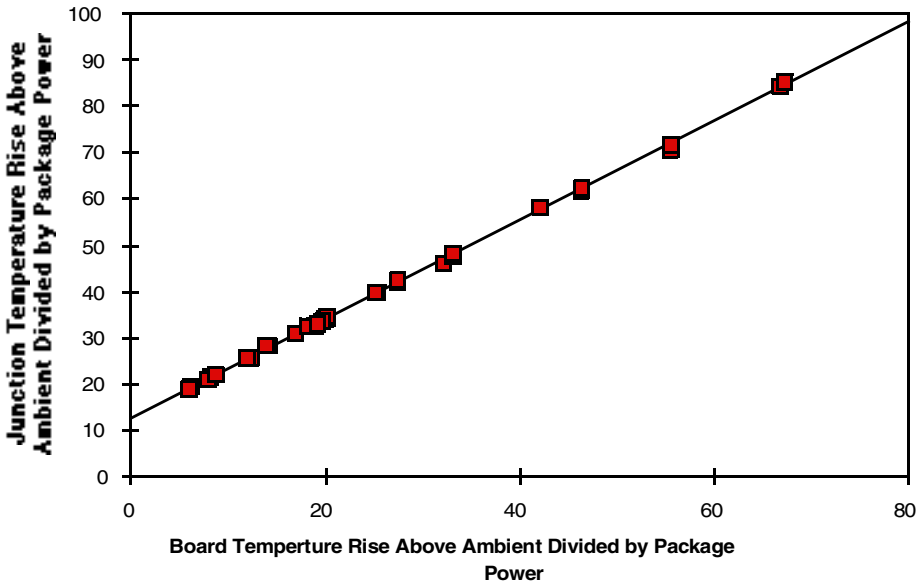


Figure 3. Effect of Board Temperature Rise on Thermal Behavior

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B8a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3) BDIP, PTR valid (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B8b	CLKOUT to BR, BG, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS Valid [4] (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3), TSIZ(0:1), REG, RSV, AT(0:3), PTR High-Z (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B11	CLKOUT to TS, BB assertion (MAX = 0.25 x B1 + 6.0)	7.60	13.60	6.30	12.30	5.00	11.00	3.80	11.30	ns
B11a	CLKOUT to TA, BI assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.30 [5])	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.80	ns
B12	CLKOUT to TS, BB negation (MAX = 0.25 x B1 + 4.8)	7.60	12.30	6.30	11.00	5.00	9.80	3.80	8.50	ns
B12a	CLKOUT to TA, BI negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B13	CLKOUT to TS, BB High-Z (MIN = 0.25 x B1)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns
B13a	CLKOUT to TA, BI High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 x B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to TEA assertion (MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B15	CLKOUT to TEA High-Z (MIN = 0.00 x B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	TA, BI valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B16a	TEA, KR, RETRY, CR valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 4.5)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	BB, BG, BR, valid to CLKOUT (setup time) [6] (4MIN = 0.00 x B1 + 0.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to TA, TEA, BI, BB, BG, BR valid (hold time) (MIN = 0.00 x B1 + 1.00 [7])	1.00	—	1.00	—	1.00	—	2.00	—	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid (hold time) (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) [8] (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) [8] (MIN = 0.00 x B1 + 1.00 [9])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) [10](MIN = 0.00 x B1 + 4.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) [10] (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 x B1 + 8.00)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = 0.00 x B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3) asserted (MAX = 0.00 x B1 + 9.00)	—	9.00		9.00		9.00		9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 x B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns

Figure 10 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

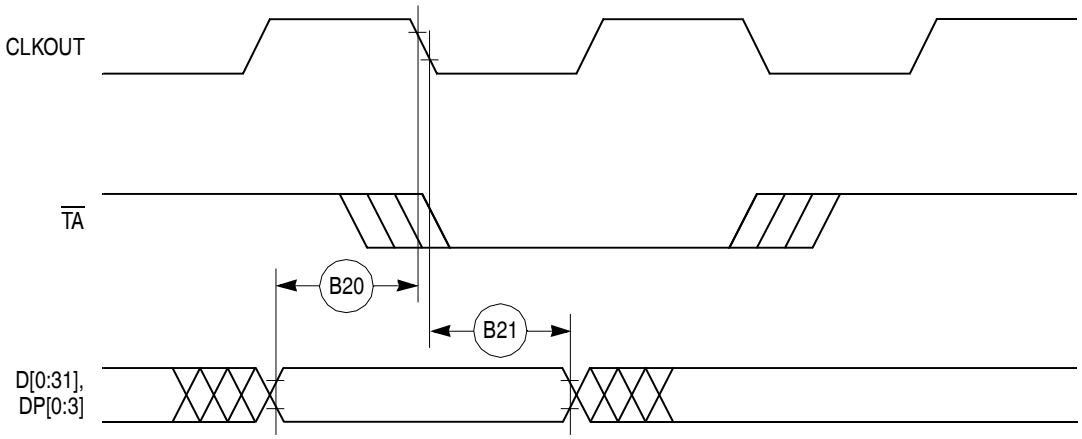


Figure 10. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 11 through Figure 14 provide the timing for the external bus read controlled by various GPCM factors.

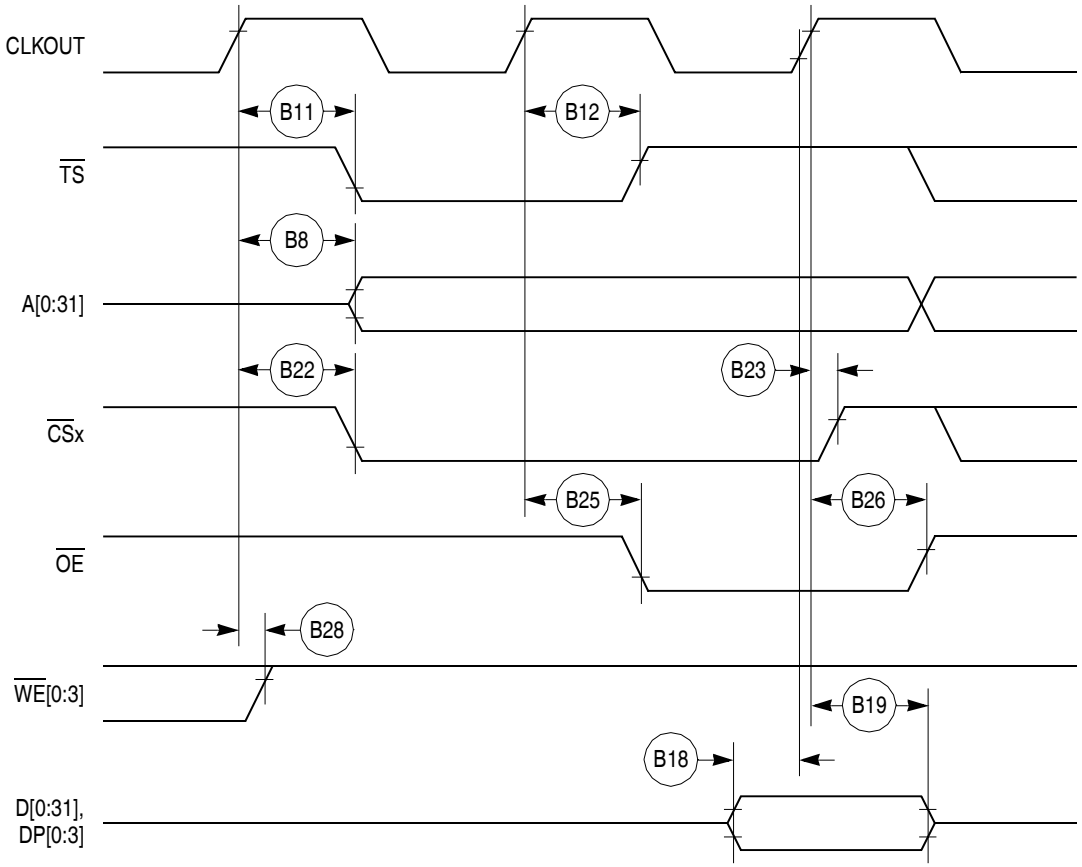


Figure 11. External Bus Read Timing (GPCM Controlled—ACS = 00)

Figure 15 through Figure 17 provide the timing for the external bus write controlled by various GPCM factors.

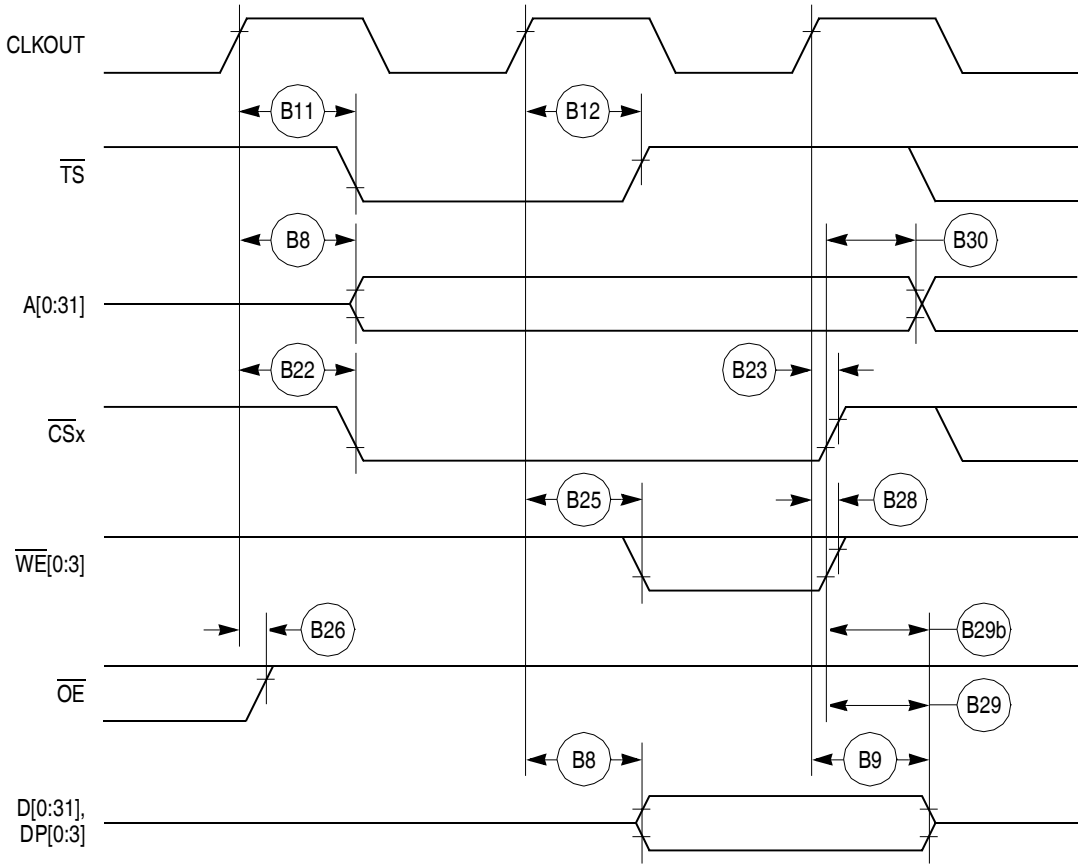


Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0,1 CSNT = 0)

Figure 21 provides the timing for the synchronous external master access controlled by the GPCM.

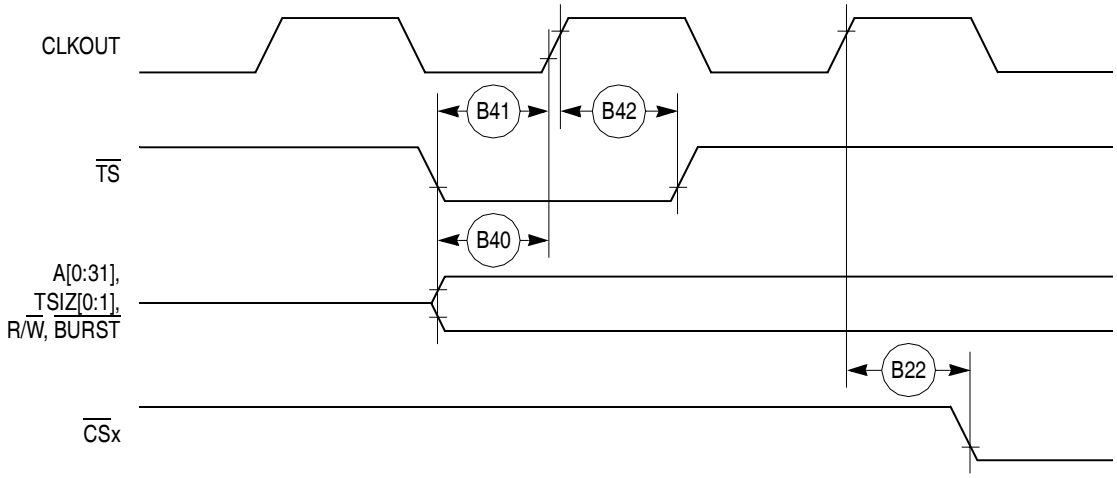


Figure 21. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 22 provides the timing for the asynchronous external master memory access controlled by the GPCM.

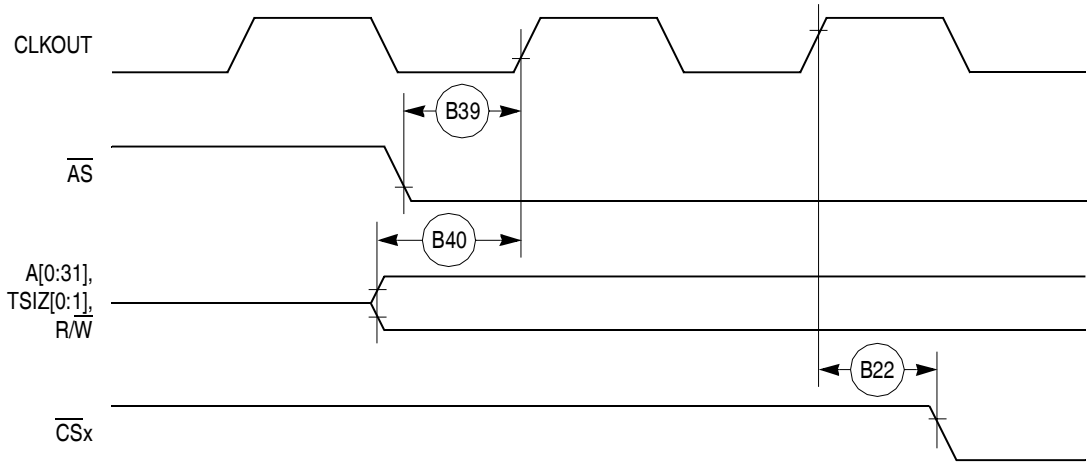


Figure 22. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 23 provides the timing for the asynchronous external master control signals negation.

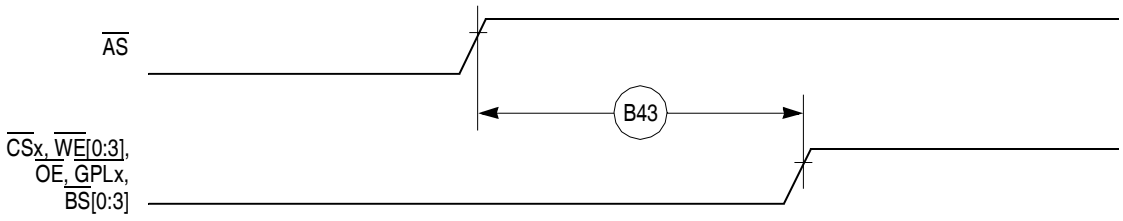


Figure 23. Asynchronous External Master—Control Signals Negation Timing

Table 9 shows the PCMCIA timing for the MPC862/857T/857DSL.

Table 9. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA Strobe asserted. [1] (MIN = 0.75 x B1 - 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation.[1] (MIN = 1.00 x B1 - 2.00)	28.30	—	23.00	—	18.00	—	13.20	—	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P47	CLKOUT to $\overline{\text{REG}}$ Invalid. (MIN = 0.25 x B1 + 1.00)	8.60	—	7.30	—	6.00	—	4.80	—	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted. (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated. (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time. (MAX = 0.00 x B1 + 11.00)	—	11.00	—	11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time. (MAX = 0.00 x B1 + 11.00)	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time (MAX = 0.25 x B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
P53	CLKOUT to ALE negate time (MAX = 0.25 x B1 + 8.00)	—	15.60	—	14.30	—	13.00	—	11.80	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid.[1] (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge.[1] (MIN = 0.00 x B1 + 8.00)	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid.[1] (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns

[1] PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAITx}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITx}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the *MPC862 PowerQUICC User s Manual*.

Figure 26 provides the PCMCIA access cycle timing for the external bus read.

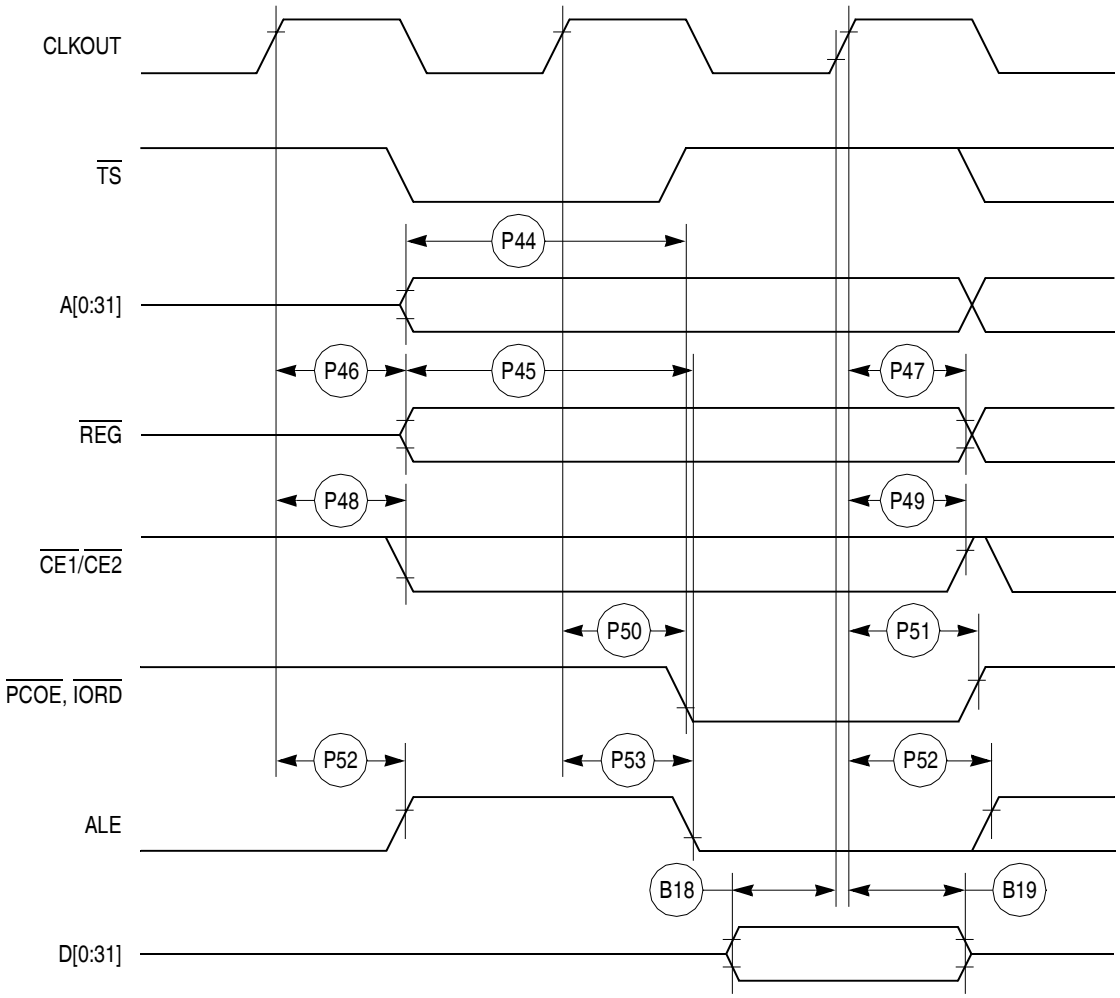


Figure 26. PCMCIA Access Cycles Timing External Bus Read

Figure 27 provides the PCMCIA access cycle timing for the external bus write.

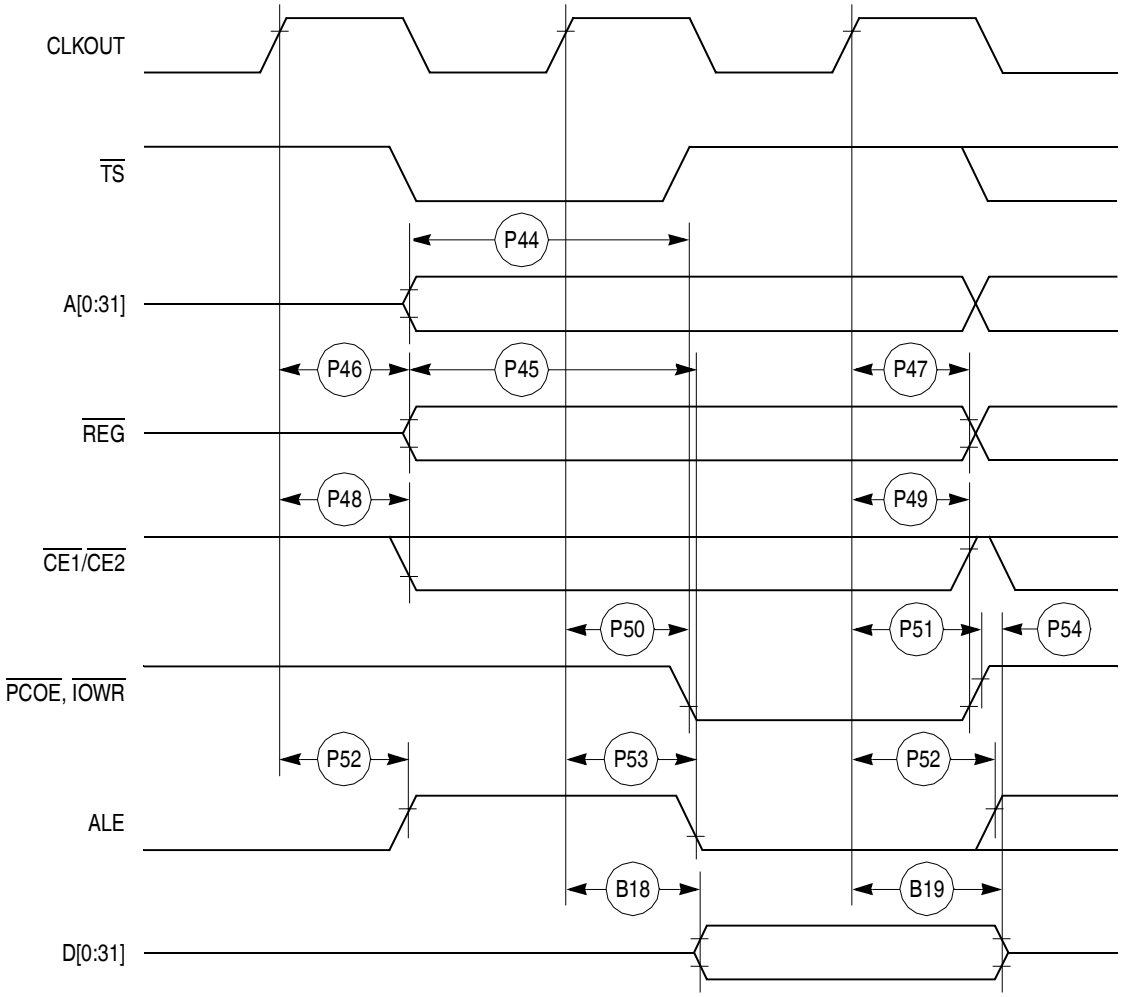


Figure 27. PCMCIA Access Cycles Timing External Bus Write

Figure 28 provides the PCMCIA $\overline{\text{WAIT}}$ signals detection timing.

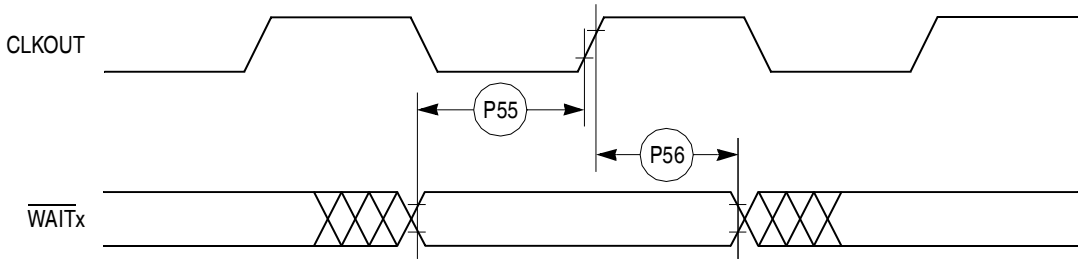


Figure 28. PCMCIA $\overline{\text{WAIT}}$ Signals Detection Timing

Table 12 shows the reset timing for the MPC862/857T/857DSL.

Table 12. Reset Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 x B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 x B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 x B1)	515.20	—	425.00	—	340.00	—	257.60	—	ns
R72	—	—	—	—	—	—	—	—	—	—
R73	Configuration data to HRESET rising edge set up time (MIN = 15.00 x B1 + 50.00)	504.50	—	425.00	—	350.00	—	277.30	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time (MIN = 0.00 x B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 x B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 x B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 x B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance. (MAX = 0.00 x B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance. (MAX = 0.00 x B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK set up (MIN = 3.00 x B1)	90.90	—	75.00	—	60.00	—	45.50	—	ns
R81	DSDI, DSCK hold time (MIN = 0.00 x B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 x B1)	242.40	—	200.00	—	160.00	—	121.20	—	ns

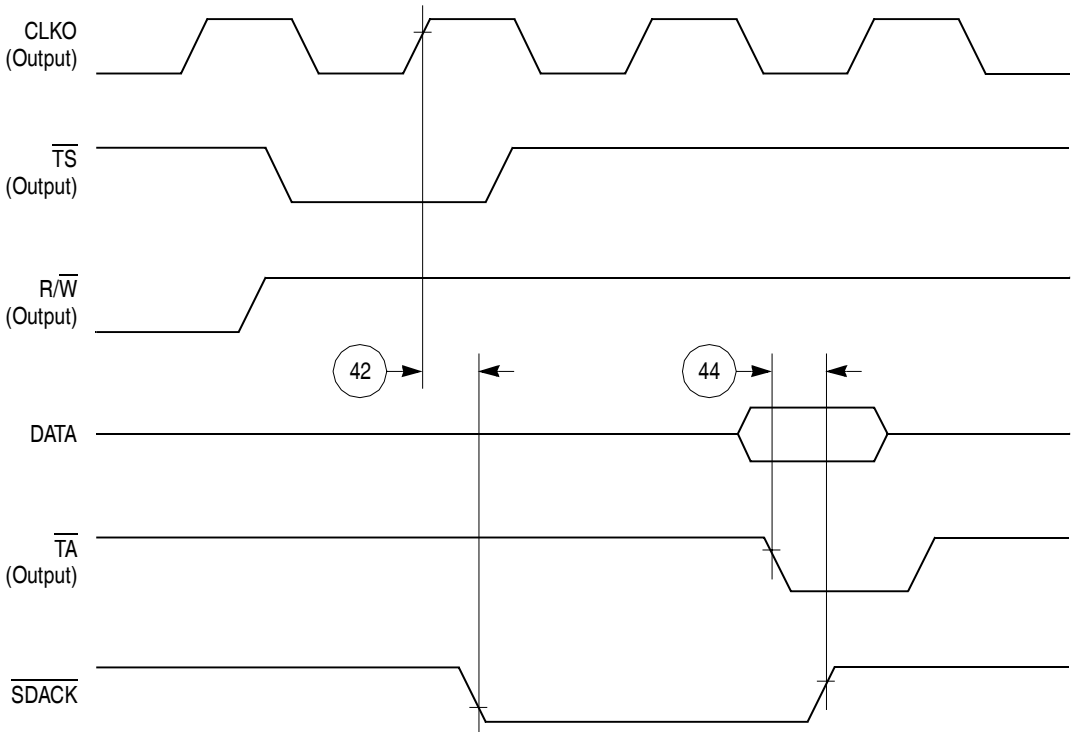


Figure 48. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA

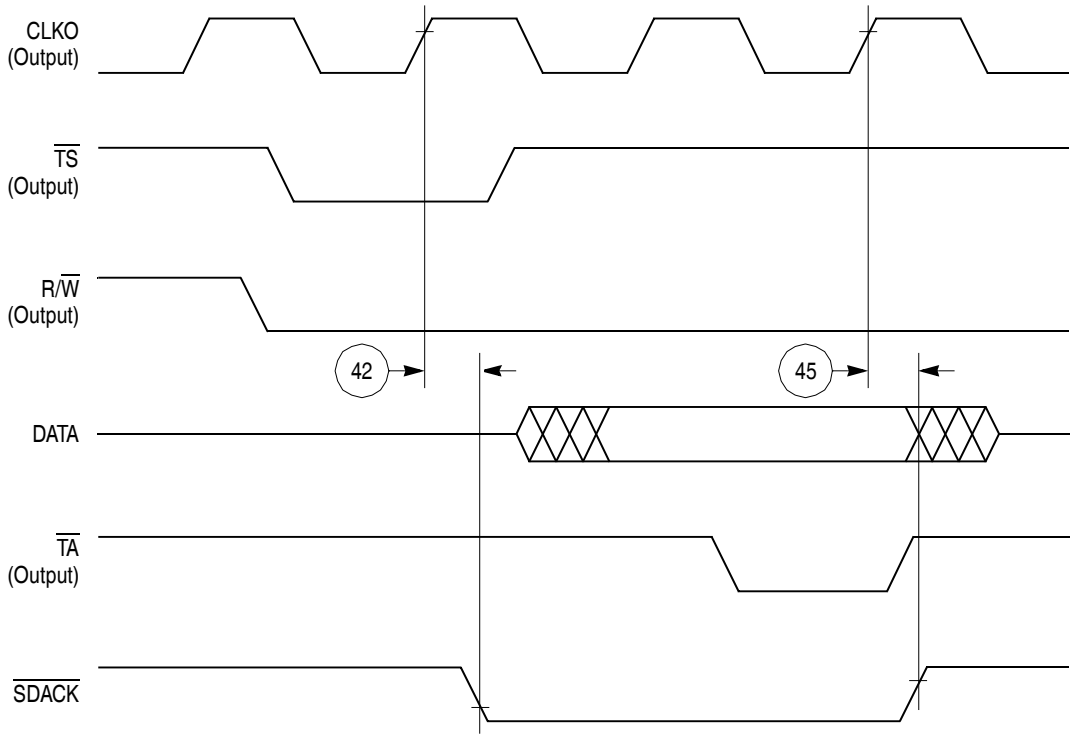


Figure 49. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

11.4 Baud Rate Generator AC Electrical Specifications

Table 17 provides the baud rate generator timings as shown in Figure 50.

Table 17. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

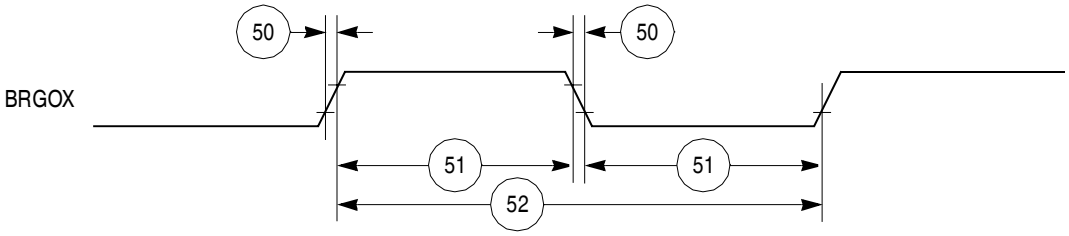


Figure 50. Baud Rate Generator Timing Diagram

11.5 Timer AC Electrical Specifications

Table 18 provides the general-purpose timer timings as shown in Figure 51.

Table 18. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1	—	clk
63	TIN/$\overline{\text{TGATE}}$ high time	2	—	clk
64	TIN/$\overline{\text{TGATE}}$ cycle time	3	—	clk
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

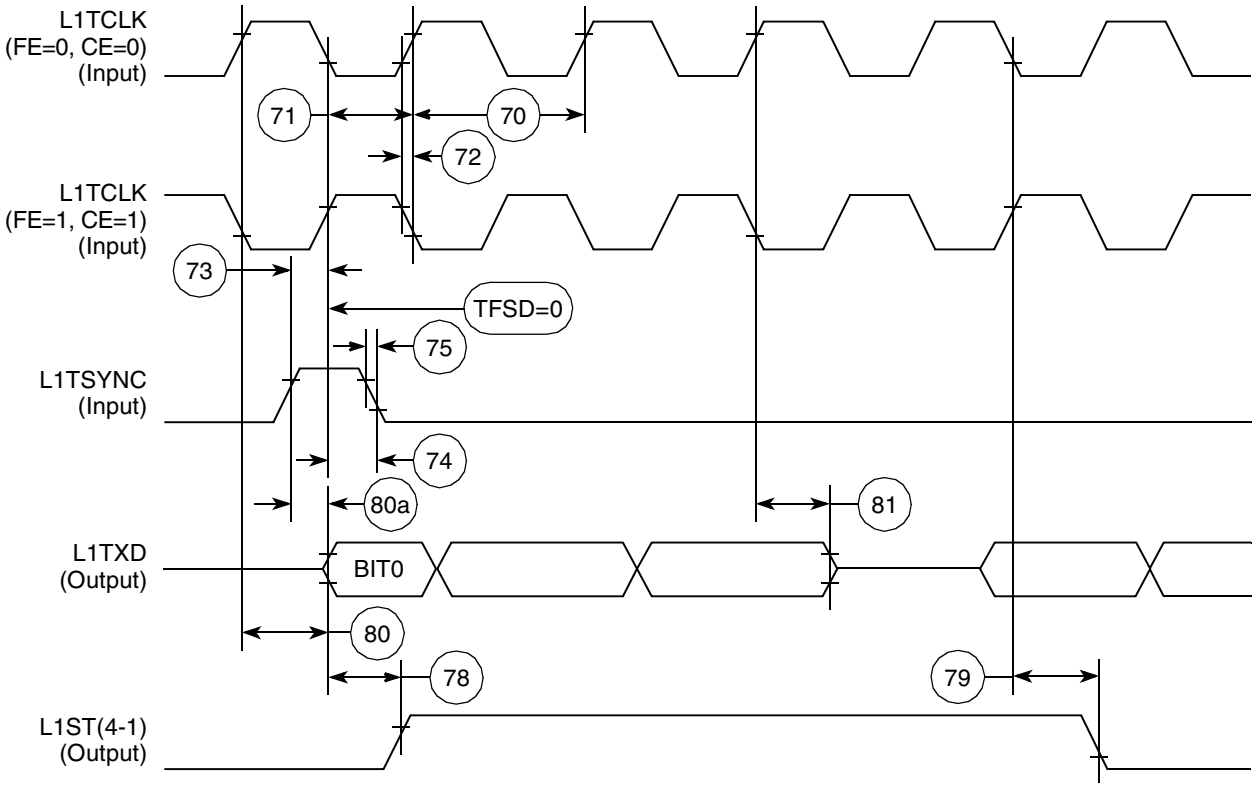


Figure 54. SI Transmit Timing Diagram (DSC = 0)

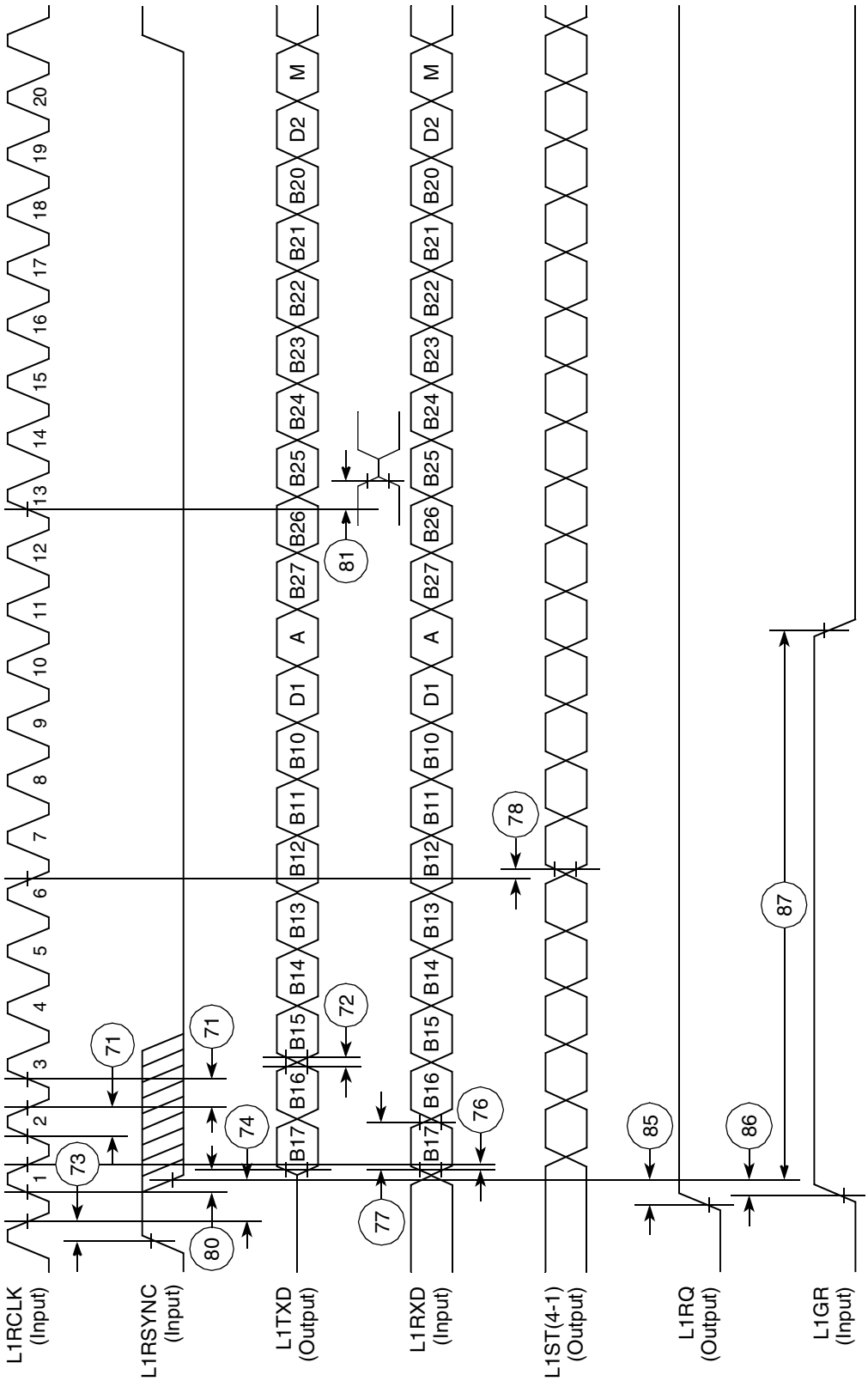
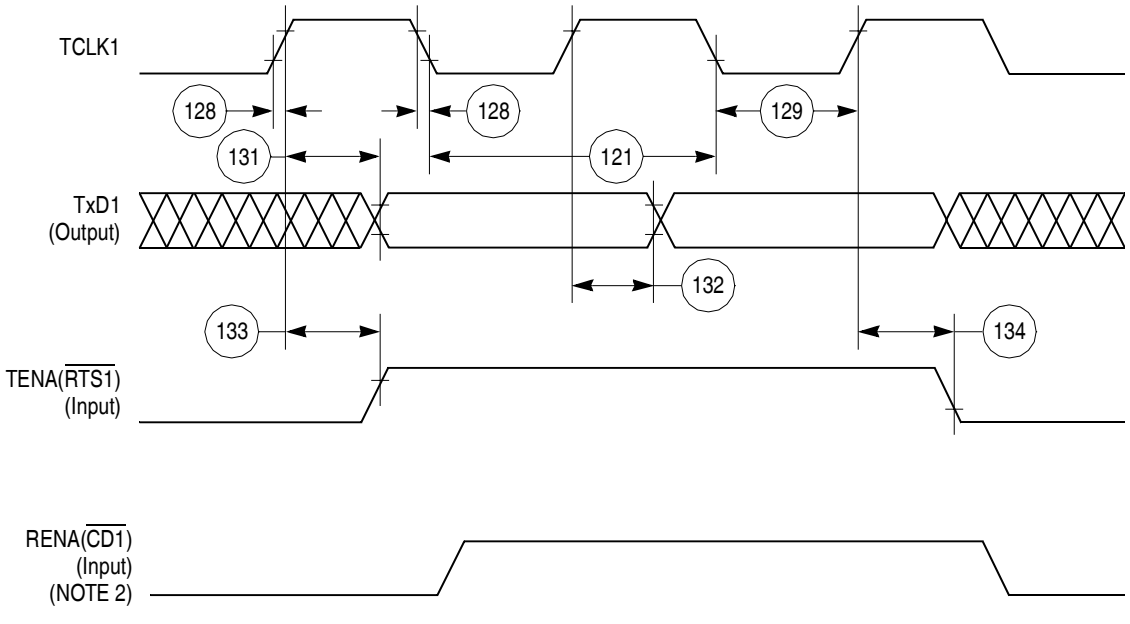


Figure 56. IDL Timing



NOTES:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 62. Ethernet Transmit Timing Diagram

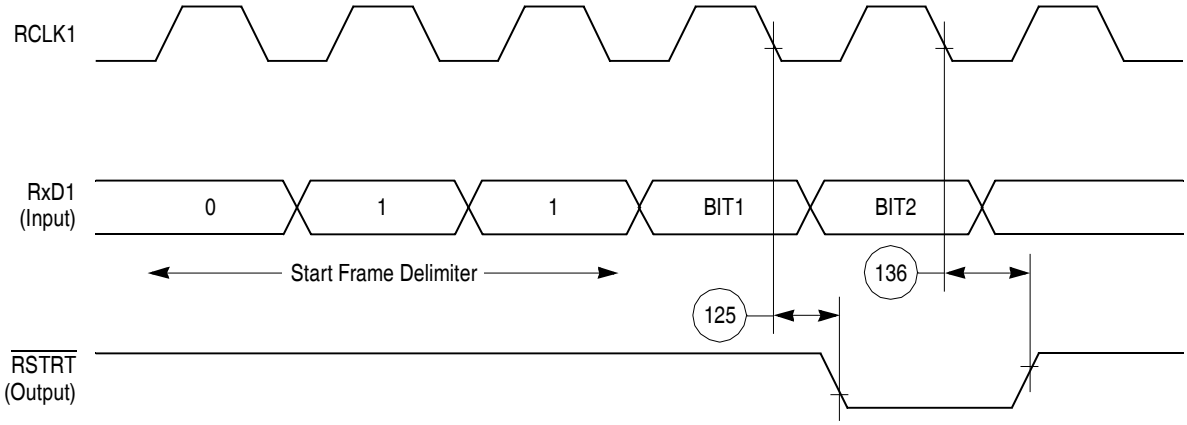


Figure 63. CAM Interface Receive Start Timing Diagram

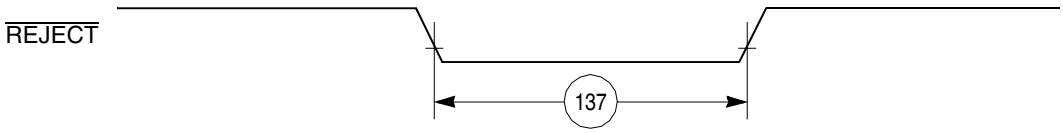


Figure 64. CAM Interface REJECT Timing Diagram

Figure 70 shows the I^{2}C bus timing.

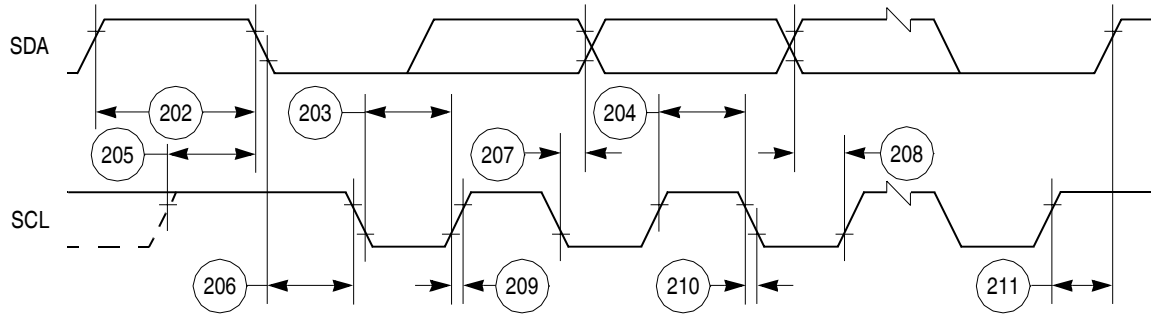


Figure 70. I^{2}C Bus Timing Diagram

12 UTOPIA AC Electrical Specifications

Table 28 shows the AC electrical specifications for the UTOPIA interface.

Table 28. UTOPIA AC Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (Internal clock option)	Output		4 ns	ns
	Duty cycle		50	50	%
	Frequency			33	MHz
U1a	UtpClk rise/fall time (external clock option)	Input		4ns	ns
	Duty cycle		40	60	%
	Frequency			33	MHz
U2	$\overline{\text{RxEnb}}$ and $\overline{\text{TxEnb}}$ active delay	Output	2 ns	16 ns	ns
U3	UTPB, SOC, Rxclav and Txclav setup time	Input	4 ns		ns
U4	UTPB, SOC, Rxclav and Txclav hold time	Input	1 ns		ns
U5	UTPB, SOC active delay (and PHREQ and PHSEL active delay in MPHY mode)	Output	2 ns	16 ns	ns

13.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency - 1%.

Table 29 provides information on the MII receive signal timing.

Table 29. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Figure 73 shows MII receive signal timing.

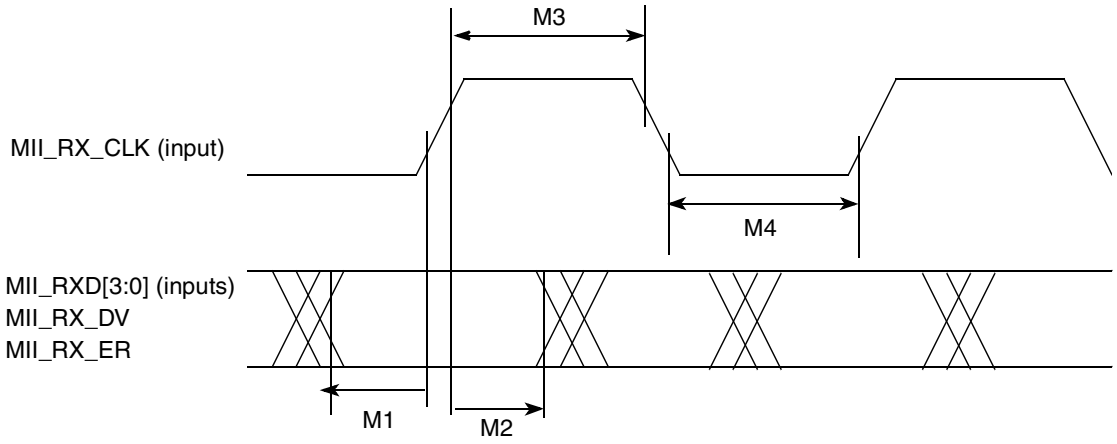


Figure 73. MII Receive Signal Timing Diagram

13.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency - 1%.

Table 30 provides information on the MII transmit signal timing.

Table 30. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
$\overline{\text{GPL\_A5}}$	D3	Output
$\overline{\text{PORESET}}$	R2	Input
$\overline{\text{RSTCONF}}$	P3	Input
$\overline{\text{HRESET}}$	N4	Open-drain
$\overline{\text{SRESET}}$	P2	Open-drain
XTAL	P1	Analog Output
EXTAL	N1	Analog Input (3.3 V only)
XFC	T2	Analog Input
CLKOUT	W3	Output
EXTCLK	N2	Input (3.3 V only)
TEXP	N3	Output
ALE_A MII-TXD1	K2	Output
$\overline{\text{CE1\_A}}$ MII-TXD2	B3	Output
$\overline{\text{CE2\_A}}$ MII-TXD3	A3	Output
$\overline{\text{WAIT\_A}}$ SOC_Split[2]	R3	Input
$\overline{\text{WAIT\_B}}$	R4	Input
IP_A0 UTPB_Split0[2] MII-RXD3	T5	Input
IP_A1 UTPB_Split1[2] MII-RXD2	T4	Input
IP_A2 $\overline{\text{IOIS16\_A}}$ UTPB_Split2[2] MII-RXD1	U3	Input
IP_A3 UTPB_Split3[2] MII-RXD0	W2	Input
IP_A4 UTPB_Split4[2] MII-RXCLK	U4	Input
IP_A5 UTPB_Split5[2] MII-RXERR	U5	Input

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
PA2 CLK6 TOUT3 L1RCLKB	R18	Bidirectional
PA1 CLK7 BRGO4 TIN4	T19	Bidirectional
PA0 CLK8 TOUT4 L1TCLKB	U19	Bidirectional
PB31 SPISEL REJECT1	C17	Bidirectional (Optional: Open-drain)
PB30 SPICLK RSTRT2	C19	Bidirectional (Optional: Open-drain)
PB29 SPIMOSI	E16	Bidirectional (Optional: Open-drain)
PB28 SPIMISO BRGO4	D19	Bidirectional (Optional: Open-drain)
PB27 I2CSDA BRGO1	E19	Bidirectional (Optional: Open-drain)
PB26 I2CSCL BRGO2	F19	Bidirectional (Optional: Open-drain)
PB25 RXADDR3[2] SMTXD1	J16	Bidirectional (Optional: Open-drain)
PB24 TXADDR3[2] SMRXD1	J18	Bidirectional (Optional: Open-drain)
PB23 TXADDR2[2] SDACK1 SMSYN1	K17	Bidirectional (Optional: Open-drain)
PB22 TXADDR4[2] SDACK2 SMSYN2	L19	Bidirectional (Optional: Open-drain)