NXP USA Inc. - KMPC862PZQ100B Datasheet



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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc862pzq100b

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- The MPC862/857T/857DSL provides enhanced ATM functionality over that of the MPC860SAR. The MPC862/857T/857DSL adds major new features available in "enhanced SAR" (ESAR) mode, including the following:
 - Improved operation, administration and maintenance (OAM) support
 - OAM performance monitoring (PM) support
 - Multiple APC priority levels available to support a range of traffic pace requirements
 - ATM port-to-port switching capability without the need for RAM-based microcode
 - Simultaneous MII (10/100Base-T) and UTOPIA (half-duplex) capability
 - Optional statistical cell counters per PHY
 - UTOPIA level 2 compliant interface with added FIFO buffering to reduce the total cell transmission time. (The earlier UTOPIA level 1 specification is also supported.)
 - Multi-PHY support on the MPC857T
 - Four PHY support on the MPC857DSL
 - Parameter RAM for both SPI and I^2C can be relocated without RAM-based microcode
 - Supports full-duplex UTOPIA both master (ATM side) and slave (PHY side) operation using a "split" bus
 - AAL2/VBR functionality is ROM-resident
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
 - Contains complete dynamic RAM (DRAM) controller
 - Each bank can be a chip select or \overline{RAS} to support a DRAM bank
 - Up to 30 wait states programmable per memory bank
 - Glueless interface to Page mode/EDO/SDRAM, SRAM, EPROMs, flash EPROMs, and other memory devices.
 - DRAM controller programmable to support most size and speed memory interfaces
 - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, one $\overline{\text{OE}}$ line
 - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
 - Variable block sizes (32 Kbyte–256 Mbyte)
 - Selectable write protection
 - On-chip bus arbitration logic
- General-purpose timers
 - Four 16-bit timers cascadable to be two 32-bit timers
 - Gate mode can enable/disable counting
 - Interrupt can be masked on reference match and event capture
- Fast Ethernet controller (FEC)
 - Simultaneous MII (10/100Base-T) and UTOPIA operation when using the UTOPIA multiplexed bus.

Features

- Universal asynchronous receiver transmitter (UART)
- Synchronous UART
- Serial infrared (IrDA)
- Binary synchronous communication (BISYNC)
- Totally transparent (bit streams)
- Totally transparent (frame based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels) (The MPC857DSL has one SMC, SMC1 for UART)
 - UART
 - Transparent
 - General circuit interface (GCI) controller
 - Can be connected to the time-division multiplexed (TDM) channels
- One serial peripheral interface (SPI)
 - Supports master and slave modes
 - Supports multiple-master operation on the same bus
- One inter-integrated circuit (I²C) port
 - Supports master and slave modes
 - Multiple-master environment support
- Time-slot assigner (TSA) (The MPC857DSL does not have the TSA)
 - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame synchronization, clocking
 - Allows dynamic changes
 - On the MPC862P and MPC862T, can be internally connected to six serial channels (four SCCs and two SMCs); on the MPC857T, can be connected to three serial channels (one SCC and two SMCs)
- Parallel interface port (PIP)
 - Centronics interface support
 - Supports fast connection between compatible ports on MPC862/857T/857DSL or MC68360
- PCMCIA interface
 - Master (socket) interface, release 2.1 compliant
 - Supports one or two PCMCIA sockets dependent upon whether ESAR functionality is enabled
 - 8 memory or I/O windows supported
- Low power support
 - Full on—All units fully powered
 - Doze—Core functional units disabled except time base decrementer, PLL, memory controller, RTC, and CPM in low-power standby

Features

- Sleep—All units disabled except RTC, PIT, time base, and decrementer with PLL active for fast wake up
- Deep sleep—All units disabled including PLL except RTC, PIT, time base, and decrementer.
- Power down mode- All units powered down except PLL, RTC, PIT, time base and
- decrementerDebug interface
 - Eight comparators: four operate on instruction address, two operate on data address, and two
 operate on data
 - Supports conditions: $= \neq < >$
 - Each watchpoint can generate a break point internally
- 3.3 V operation with 5-V TTL compatibility except EXTAL and EXTCLK
- 357-pin plastic ball grid array (PBGA) package
- Operation up to 100MHz

The MPC862/857T/857DSL is comprised of three modules that each use the 32-bit internal bus: the MPC8xx core, the system integration unit (SIU), and the communication processor module (CPM). The MPC862P/862T block diagram is shown in Figure 1. The MPC857T/857DSL block diagram is shown in Figure 2.

Features

*The MPC862T contains 4-Kbyte instruction cache and 4-Kbyte data cache.

Figure 1. MPC862P/862T Block Diagram

Maximum Tolerated Ratings

*The MPC857DSL does not contain SMC2 nor the Time Slot Assigner, and provides eight SDMA controllers.

Figure 2. MPC857T/MPC857DSL Block Diagram

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC862/857T/857DSL. Table 2 provides the maximum ratings.

Table 2. Maximum Tolerated Ratings

(GND = 0 V)

Rating	Symbol	Value	Unit	Max Freq (MHz)
Supply voltage ¹	VDDH	-0.3 to 4.0	V	-
	VDDL	-0.3 to 4.0	V	-
	KAPWR	-0.3 to 4.0	V	-
	VDDSYN	-0.3 to 4.0	V	-

Num	Charactoristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit	
NUM	Characteristic	Min	Max	Min	Max	Min	Мах	Min	Max	Unit	
B8a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3) BDIP, PTR valid (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns	
B8b	CLKOUT to \overline{BR} , \overline{BG} , VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS Valid ⁴ (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns	
B9	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3), TSIZ(0:1), REG, RSV, AT(0:3), PTR High-Z (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns	
B11	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ assertion (MAX = 0.25 x B1 + 6.0)	7.60	13.60	6.30	12.30	5.00	11.00	3.80	11.30	ns	
B11a	CLKOUT to \overline{TA} , \overline{BI} assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.30 ⁵)	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.80	ns	
B12	CLKOUT to \overline{TS} , \overline{BB} negation (MAX = 0.25 x B1 + 4.8)	7.60	12.30	6.30	11.00	5.00	9.80	3.80	8.50	ns	
B12a	CLKOUT to \overline{TA} , \overline{BI} negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns	
B13	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ High-Z (MIN = 0.25 x B1)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns	
B13a	CLKOUT to \overline{TA} , \overline{BI} High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 x B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns	
B14	CLKOUT to TEA assertion (MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns	
B15	CLKOUT to $\overline{\text{TEA}}$ High-Z (MIN = 0.00 x B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns	
B16	\overline{TA} , \overline{BI} valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns	
B16a	TEA, KR, RETRY, CR valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 4.5)	4.50	_	4.50	_	4.50	_	4.50	_	ns	
B16b	$\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$, valid to CLKOUT (setup time) ⁶ (4MIN = 0.00 x B1 + 0.00)	4.00	-	4.00	-	4.00	—	4.00	—	ns	
B17	CLKOUT to \overline{TA} , \overline{TEA} , \overline{BI} , \overline{BB} , \overline{BG} , \overline{BR} valid (hold time) (MIN = 0.00 x B1 + 1.00 ⁷)	1.00	_	1.00	_	1.00	_	2.00	_	ns	

Table 7. Bus Operation Timings (continued)

Bus Signal Timing

Nium	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		11
NUM	Characteristic	Min	Max	Min	Max	Min	Мах	Min	Max	Unit
B32c	CLKOUT rising edge to $\overline{\text{BS}}$ valid - as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32d	CLKOUT falling edge to \overline{BS} valid- as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 x B1 + 6.60)	9.40	18.00	7.60	16.00	13.30	14.10	11.30	12.30	ns
B33	CLKOUT falling edge to $\overline{\text{GPL}}$ valid - as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{\text{GPL}}$ Valid - as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid - as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	_	4.30	_	3.00	_	1.80	_	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid - as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 x B1 - 2.00)	13.20	_	10.50	_	8.00	_	5.60	_	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid - as requested by CST2 in the corresponding word in UPM (MIN = 0.75 x B1 - 2.00)	20.70	_	16.70	_	13.00	_	9.40	_	ns
B35	A(0:31), BADDR(28:30) to \overline{CS} valid - as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	_	4.30	_	3.00	_	1.80	_	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to BS valid - As Requested by BST1 in the corresponding word in the UPM (MIN = 0.50 x B1 - 2.00)	13.20	_	10.50	_	8.00	_	5.60	_	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to BS valid - as requested by control bit BST2 in the corresponding word in the UPM (MIN = $0.75 \times B1 - 2.00$)	20.70	_	16.70	_	13.00	_	9.40	_	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to \overline{GPL} valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	_	4.30	_	3.00	_	1.80	_	ns

Table 7. Bus Operation Timings (continued)

Figure 6 provides the timing for the synchronous output signals.

Figure 6. Synchronous Output Signals Timing

Figure 7 provides the timing for the synchronous active pull-up and open-drain output signals.

Figure 7. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

Bus Signal Timing

Figure 19 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

Cycles Timing

Figure 20 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

Figure 21 provides the timing for the synchronous external master access controlled by the GPCM.

Figure 22 provides the timing for the asynchronous external master memory access controlled by the GPCM.

(GPCM Controlled—ACS = 00)

Figure 23 provides the timing for the asynchronous external master control signals negation.

Figure 23. Asynchronous External Master—Control Signals Negation Timing

Figure 33. Reset Timing—Configuration from Data Bus

Figure 34 provides the reset timing for the data bus weak drive during configuration.

Figure 34. Reset Timing—Data Bus Weak Drive during Configuration

11.7 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

Table 20. NMSI External Clock Timing

Num	Characteristic	All Freq	Unit	
Num	Characteristic	Min	Мах	Om
100	RCLK1 and TCLK1 width high ¹	1/SYNCCLK	_	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK +5	_	ns
102	RCLK1 and TCLK1 rise/fall time	_	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	RTS1 active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	CTS1 setup time to TCLK1 rising edge	5.00		ns
106	RXD1 setup time to RCLK1 rising edge	5.00		ns
107	RXD1 hold time from RCLK1 rising edge ²	5.00	_	ns
108	CD1 setup Time to RCLK1 rising edge	5.00	_	ns

¹ The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Charactoristic	All Freq	Unit	
Nulli	Characteristic	Min	Мах	Onit
100	RCLK1 and TCLK1 frequency ¹	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	_	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	RTS1 active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	CTS1 setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	_	ns
107	RXD1 hold time from RCLK1 rising edge ²	0.00	—	ns
108	CD1 setup time to RCLK1 rising edge	40.00		ns

¹ The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 3/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

11.10 SPI Master AC Electrical Specifications

Table 24 provides the SPI master timings as shown in Figure 66 though Figure 67.

Table 24. SPI Master Timing

Num	Characteristic	All Freq	Unit	
Num	Characteristic	Min	Мах	Onit
160	MASTER cycle time	4	1024	t _{cyc}
161	MASTER clock (SCK) high or low time	2	512	t _{cyc}
162	MASTER data setup time (inputs)	15	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	10	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

Figure 66. SPI Master (CP = 0) Timing Diagram

11.12 I²C AC Electrical Specifications

Table 26 provides the I^2C (SCL < 100 KHz) timings.

Num	Characteristic	All Freq	Unit	
Num	Characteristic	Min	Max	Unit
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master) ¹	1.5	100	kHz
202	Bus free time between transmissions	4.7	_	μs
203	Low period of SCL	4.7	_	μs
204	High period of SCL	4.0	_	μs
205	Start condition setup time	4.7	_	μs
206	Start condition hold time	4.0	_	μs
207	Data hold time	0	_	μs
208	Data setup time	250	_	ns
209	SDL/SCL rise time	_	1	μs
210	SDL/SCL fall time	_	300	ns
211	Stop condition setup time	4.7	_	μs

SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 27 provides the I^2C (SCL > 100 kHz) timings.

Table 27. I^2C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Freq	Unit	
Nulli	Characteristic	Expression	Min	Max	Onit
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) ¹	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	_	1/(2.2 * fSCL)	_	S
203	Low period of SCL	—	1/(2.2 * fSCL)	_	S
204	High period of SCL	—	1/(2.2 * fSCL)	_	S
205	Start condition setup time	—	1/(2.2 * fSCL)	_	S
206	Start condition hold time	—	1/(2.2 * fSCL)	_	S
207	Data hold time	—	0	_	S
208	Data setup time	—	1/(40 * fSCL)	_	S
209	SDL/SCL rise time	_	_	1/(10 * fSCL)	S
210	SDL/SCL fall time	—	—	1/(33 * fSCL)	S
211	Stop condition setup time	—	1/2(2.2 * fSCL)	_	S

SCL frequency is given by SCL = BrgClk_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

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Num	Characteristic	Min	Max	Unit
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Table 30. MII Transmit Signal Timing (continued)

Figure 74 shows the MII transmit signal timing diagram.

Figure 74. MII Transmit Signal Timing Diagram

13.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 31 provides information on the MII async inputs signal timing.

Table 31. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 75 shows the MII asynchronous inputs signal timing diagram.

Figure 75. MII Async Inputs Timing Diagram

13.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 32 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Name	Pin Number	Туре
PA15 RXD1 RXD4	C18	Bidirectional
PA14 TXD1 TXD4	D17	Bidirectional (Optional: Open-drain)
PA13 RXD2	E17	Bidirectional
PA12 TXD2	F17	Bidirectional (Optional: Open-drain)
PA11 L1TXDB RXD3	G16	Bidirectional (Optional: Open-drain)
PA10 L1RXDB TXD3	J17	Bidirectional (Optional: Open-drain)
PA9 L1TXDA	К18	Bidirectional (Optional: Open-drain)
RXD4		
PA8 L1RXDA TXD4	L17	Bidirectional (Optional: Open-drain)
PA7 CLK1 L1RCLKA BRGO1 TIN1	M19	Bidirectional
PA6 CLK2 TOUT1	M17	Bidirectional
PA5 CLK3 L1TCLKA BRGO2 TIN2	N18	Bidirectional
PA4 CLK4 TOUT2	P19	Bidirectional
PA3 CLK5 BRGO3 TIN3	P17	Bidirectional

Table 35. Pin Assignments (continued)

Document Revision History

15 Document Revision History

Table 36 lists significant changes between revisions of this document.

Rev. No.	Date	Substantive Changes	
0	2001	Initial revision	
0.1	9/2001	Change extended temperature from 95 to 105	
0.2	11/2001	Revised for new template, changed Table 7 B23 max value @ 66 MHz from 2 ns to 8 ns.	
0.3	4/2002	 Timing modified and equations added, for Rev. A and B devices. Modified power numbers and temperature ranges. Added ESAR UTOPIA timing. 	
1.0	9/2002	 Specification changed to include the MPC857T and MPC857DSL. Changed maximum operating frequency from 80 MHz to 100 MHz. Removed MPC862DP, DT, and SR derivatives and part numbers. Corrected power dissipation numbers. Changed UTOPIA maximum frequency from 50 MHz to 33 MHz. Changed part number ordering information to Rev. B devices only. To maximum ratings for temperature, added frequency ranges. 	
1.1	5/2003	Changed SPI Master Timing Specs. 162 and 164	
1.2	8/2003	 Changed B28a through B28d and B29b to show that TRLX can be 0 or 1. Non-technical reformatting 	
2.0	11/2004	 Added a table footnote to Table 5 DC Electrical Specifications about meeting the VIL Max of the I2C Standard. Updated document template. 	
3.0	2/2006	Changed Tj from 95C to 105C in table 34	

Table 36. Document Revision History

Document Revision History

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