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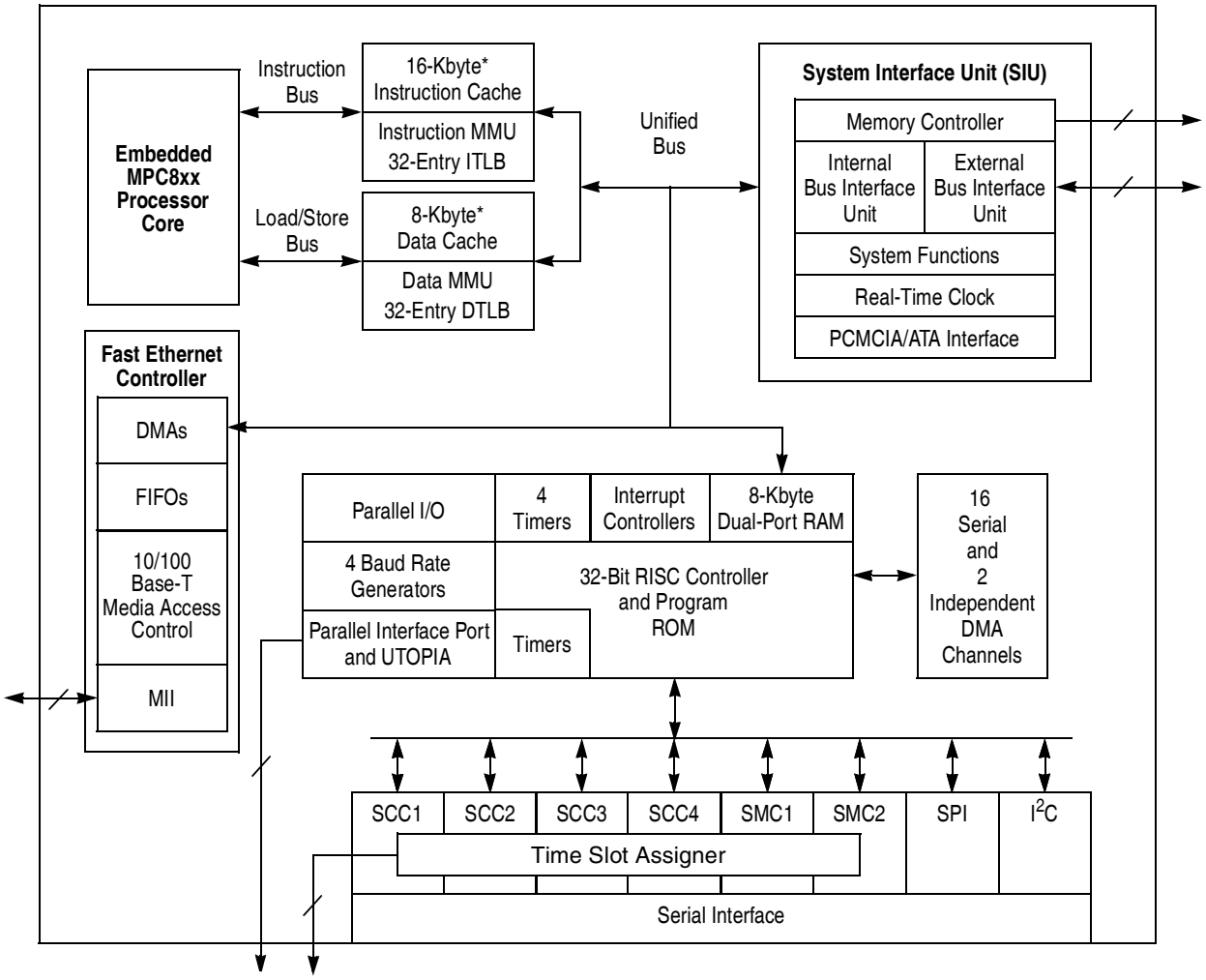
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

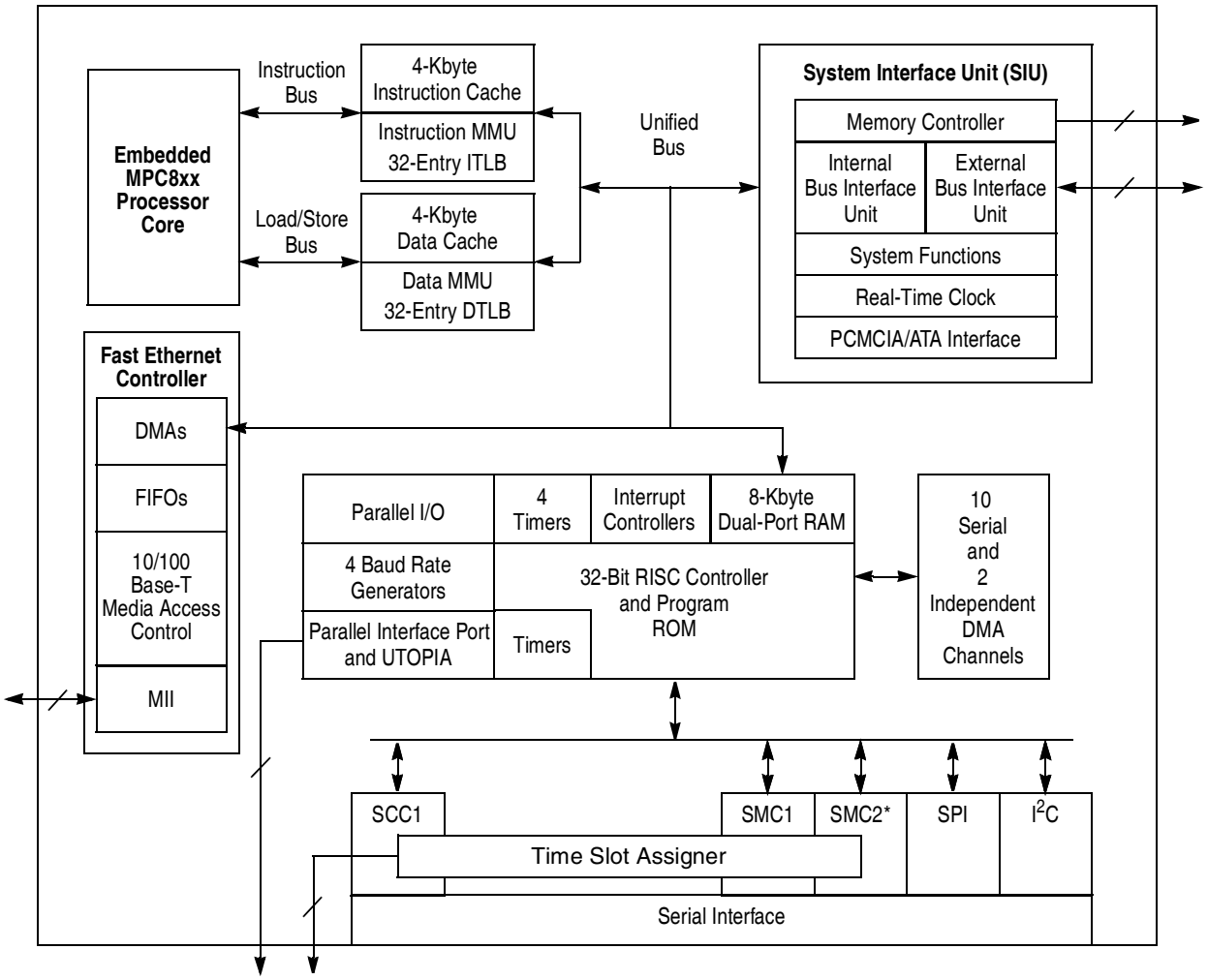
Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 115°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc862tczq80b



*The MPC862T contains 4-Kbyte instruction cache and 4-Kbyte data cache.

Figure 1. MPC862P/862T Block Diagram



*The MPC857DSL does not contain SMC2 nor the Time Slot Assigner, and provides eight SDMA controllers.

Figure 2. MPC857T/MPC857DSL Block Diagram

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC862/857T/857DSL. Table 2 provides the maximum ratings.

Table 2. Maximum Tolerated Ratings

(GND = 0 V)

Rating	Symbol	Value	Unit	Max Freq (MHz)
Supply voltage [1]	VDDH	-0.3 to 4.0	V	-
	VDDL	-0.3 to 4.0	V	-
	KAPWR	-0.3 to 4.0	V	-
	VDDSYN	-0.3 to 4.0	V	-

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC862/857T/857DSL.

Table 3. MPC862/857T/857DSL Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction to ambient [1]	Natural Convection	Single layer board (1s)	$R_{\theta JA}$ [2]	37	°C/W
		Four layer board (2s2p)	$R_{\theta JMA}$ [3]	23	
	Air flow (200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$ [3]	30	
		Four layer board (2s2p)	$R_{\theta JMA}$ [3]	19	
Junction to board [4]			$R_{\theta JB}$	13	
Junction to case [5]			$R_{\theta JC}$	6	
Junction to package top [6]	Natural Convection		Ψ_{JT}	2	
	Air flow (200 ft/min)		Ψ_{JT}	2	

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5 Power Dissipation

Table 4 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice bus speed.

Table 4. Power Dissipation (P_D)

Die Revision	Frequency	Typical [1]	Maximum [2]	Unit
0 (1:1 Mode)	50 MHz	656	735	mW
	66 MHz	TBD	TBD	mW
A.1, B.0 (1:1 Mode)	50 MHz	630	760	mW
	66 MHz	890	1000	mW

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W)

T_B = board temperature (°C)

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B8a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3) BDIP, PTR valid (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B8b	CLKOUT to BR, BG, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS Valid [4] (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3), TSIZ(0:1), REG, RSV, AT(0:3), PTR High-Z (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B11	CLKOUT to TS, BB assertion (MAX = 0.25 x B1 + 6.0)	7.60	13.60	6.30	12.30	5.00	11.00	3.80	11.30	ns
B11a	CLKOUT to TA, BI assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.30 [5])	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.80	ns
B12	CLKOUT to TS, BB negation (MAX = 0.25 x B1 + 4.8)	7.60	12.30	6.30	11.00	5.00	9.80	3.80	8.50	ns
B12a	CLKOUT to TA, BI negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B13	CLKOUT to TS, BB High-Z (MIN = 0.25 x B1)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns
B13a	CLKOUT to TA, BI High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 x B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to TEA assertion (MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B15	CLKOUT to TEA High-Z (MIN = 0.00 x B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	TA, BI valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B16a	TEA, KR, RETRY, CR valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 4.5)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	BB, BG, BR, valid to CLKOUT (setup time) [6] (4MIN = 0.00 x B1 + 0.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to TA, TEA, BI, BB, BG, BR valid (hold time) (MIN = 0.00 x B1 + 1.00 [7])	1.00	—	1.00	—	1.00	—	2.00	—	ns

Figure 8 provides the timing for the synchronous input signals.

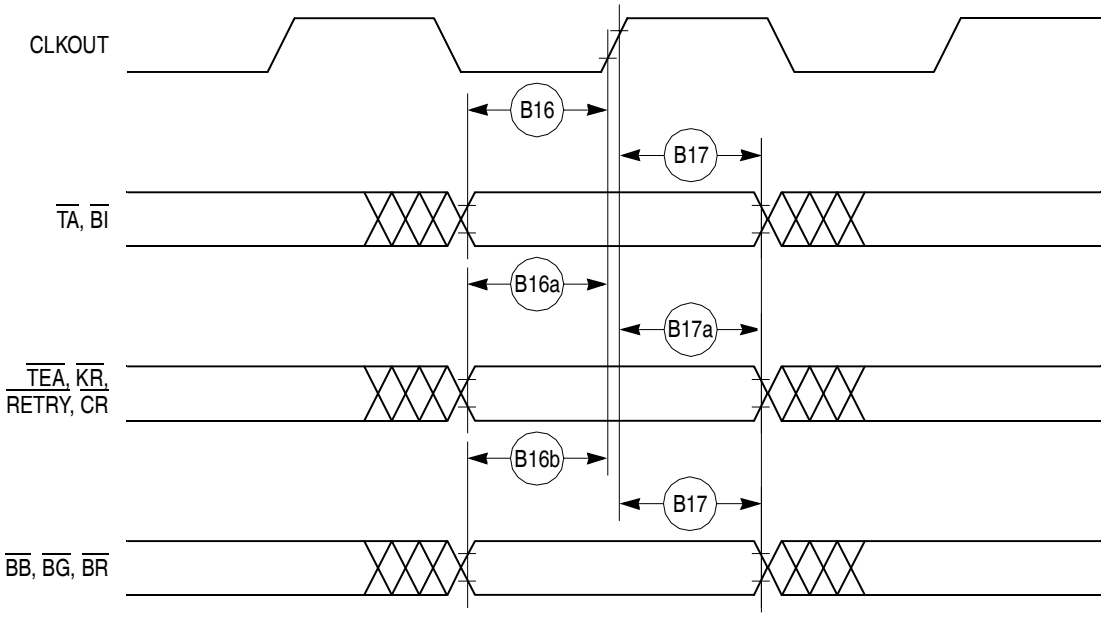


Figure 8. Synchronous Input Signals Timing

Figure 9 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

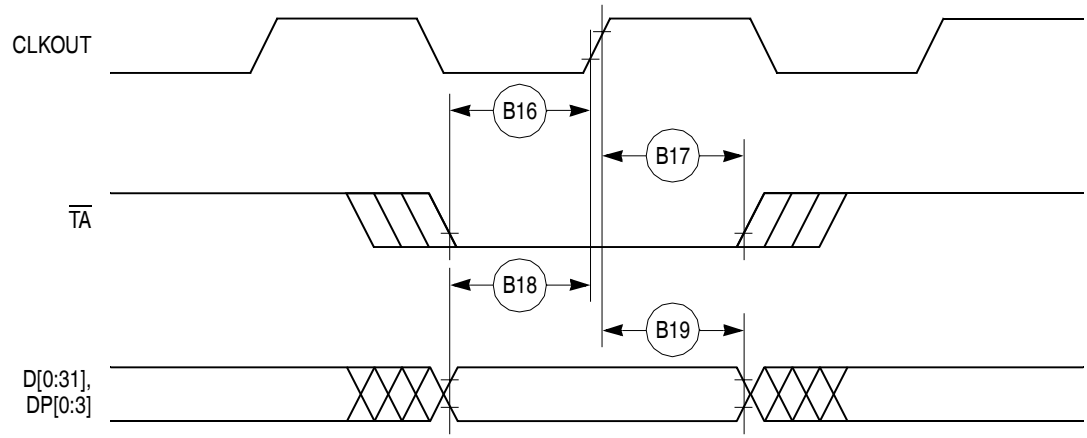


Figure 9. Input Data Timing in Normal Case

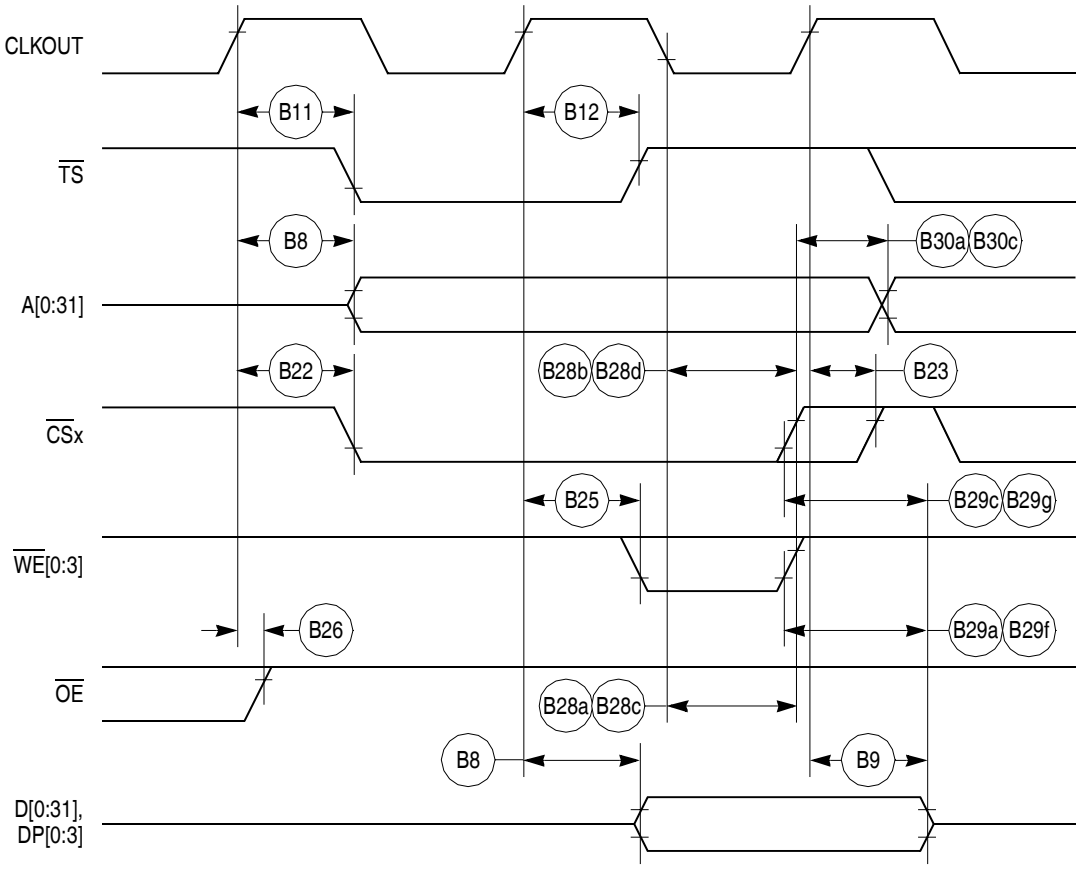


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0,1 CSNT = 1)

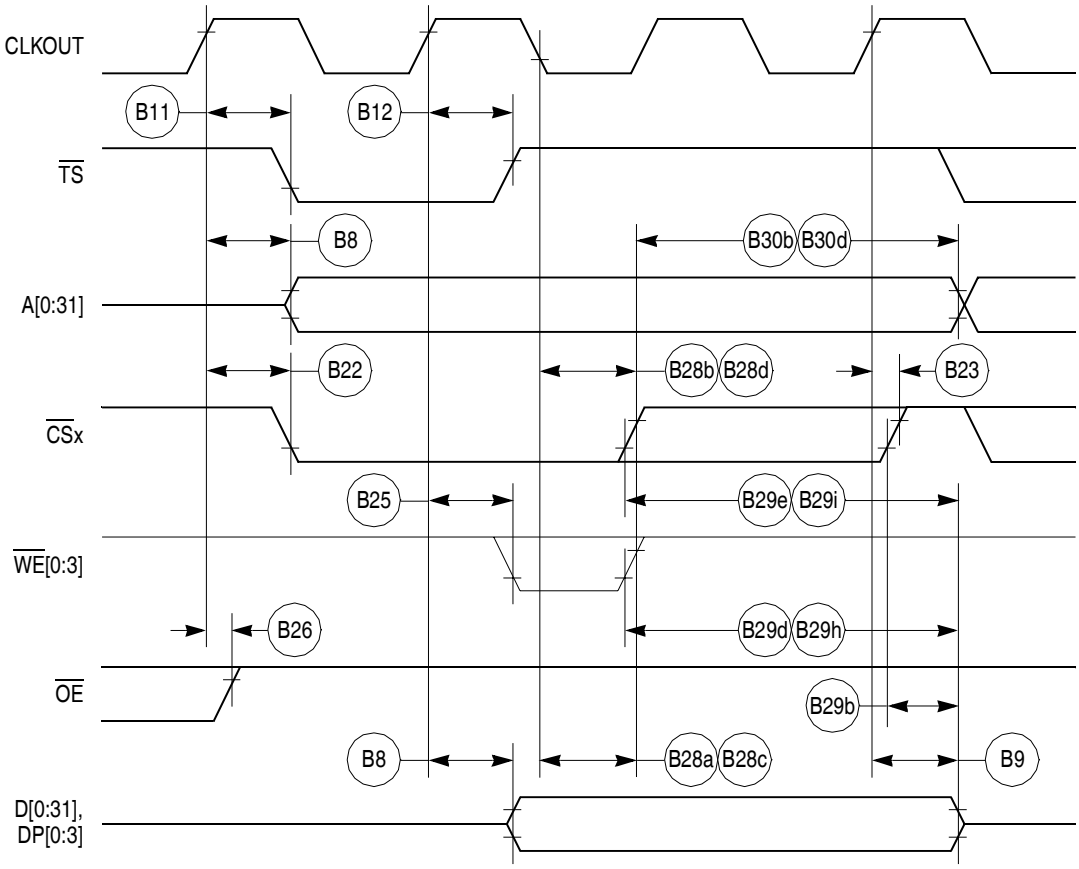


Figure 17. External Bus Write Timing (GPCM Controlled—TRLX = 0,1, CSNT = 1)

Table 10 shows the PCMCIA port timing for the MPC862/857T/857DSL.

Table 10. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx Valid (MAX = 0.00 x B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive [1] (MIN = 0.75 x B1 + 3.00)	25.70	—	21.70	—	18.00	—	14.40	—	ns
P59	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 x B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 x B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

1 OP2 and OP3 only.

Figure 29 provides the PCMCIA output port timing for the MPC862/857T/857DSL.

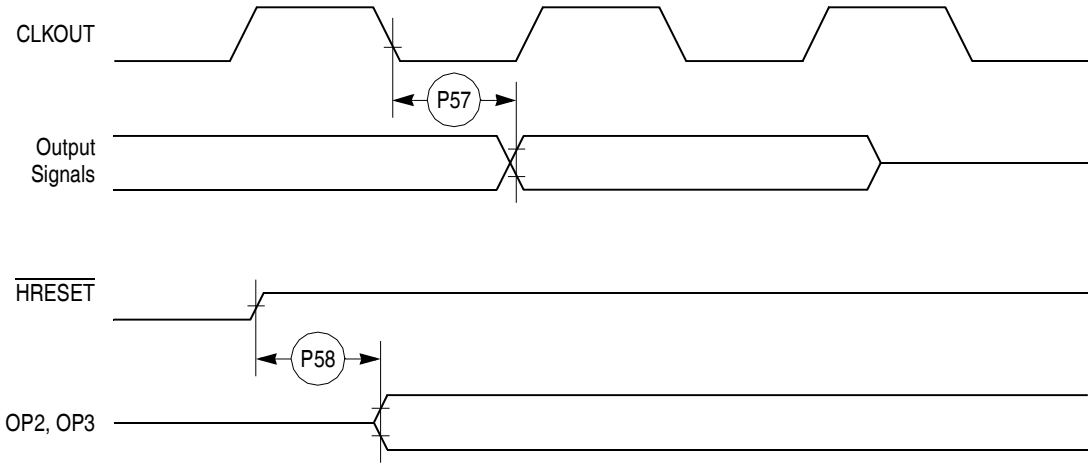


Figure 29. PCMCIA Output Port Timing

Figure 30 provides the PCMCIA output port timing for the MPC862/857T/857DSL.

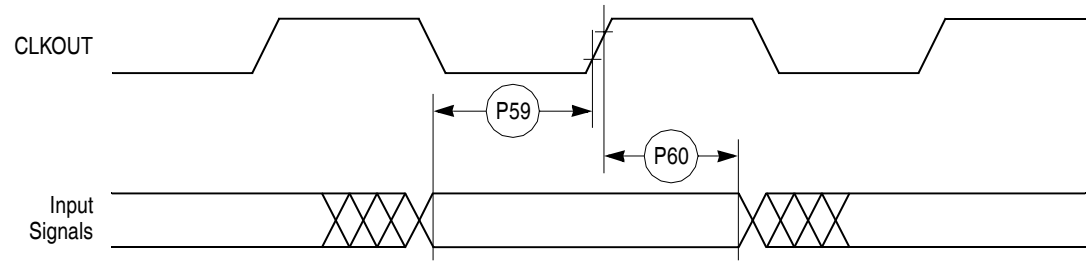


Figure 30. PCMCIA Input Port Timing

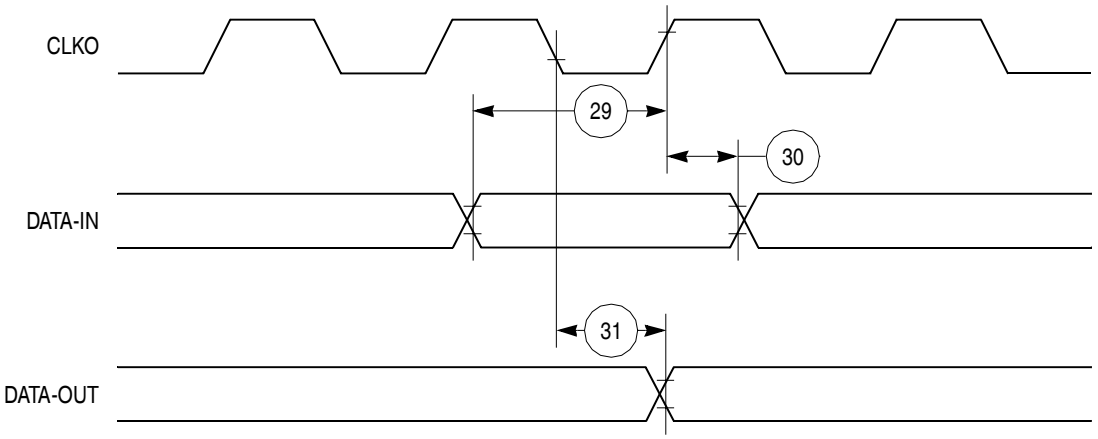


Figure 44. Parallel I/O Data-In/Data-Out Timing Diagram

11.2 Port C Interrupt AC Electrical Specifications

Table 15 provides the timings for port C interrupts.

Table 15. Port C Interrupt Timing

Num	Characteristic	33.34 MHz		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

Figure 45 shows the port C interrupt detection timing.

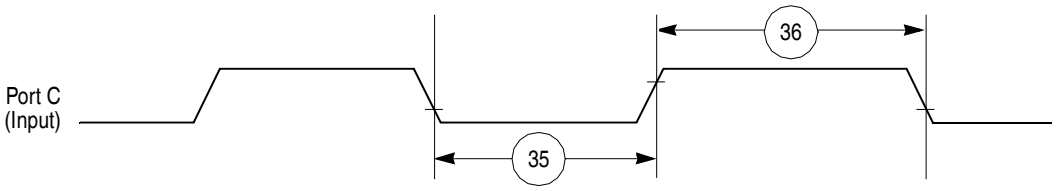


Figure 45. Port C Interrupt Detection Timing

11.3 IDMA Controller AC Electrical Specifications

Table 16 provides the IDMA controller timings as shown in Figure 46 though Figure 49.

Table 16. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high	3	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns

Table 16. IDMA Controller Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

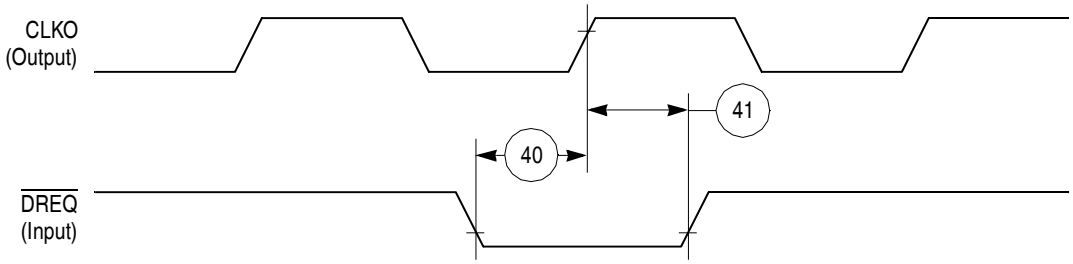


Figure 46. IDMA External Requests Timing Diagram

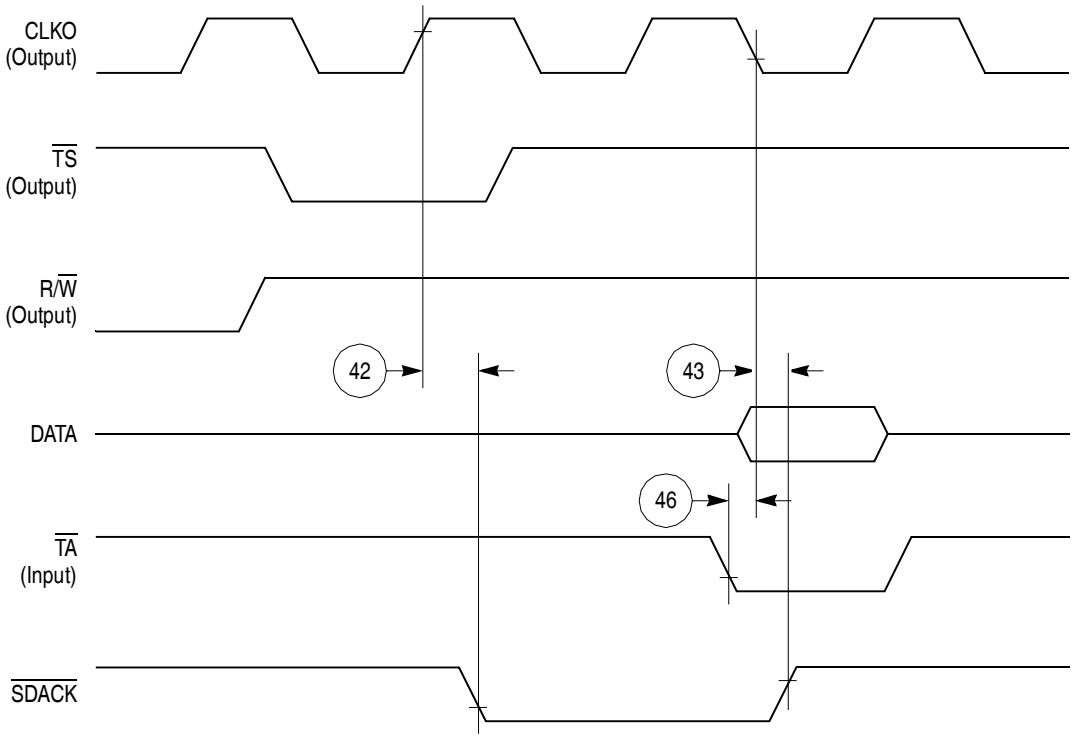


Figure 47. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Externally-Generated $\overline{\text{TA}}$

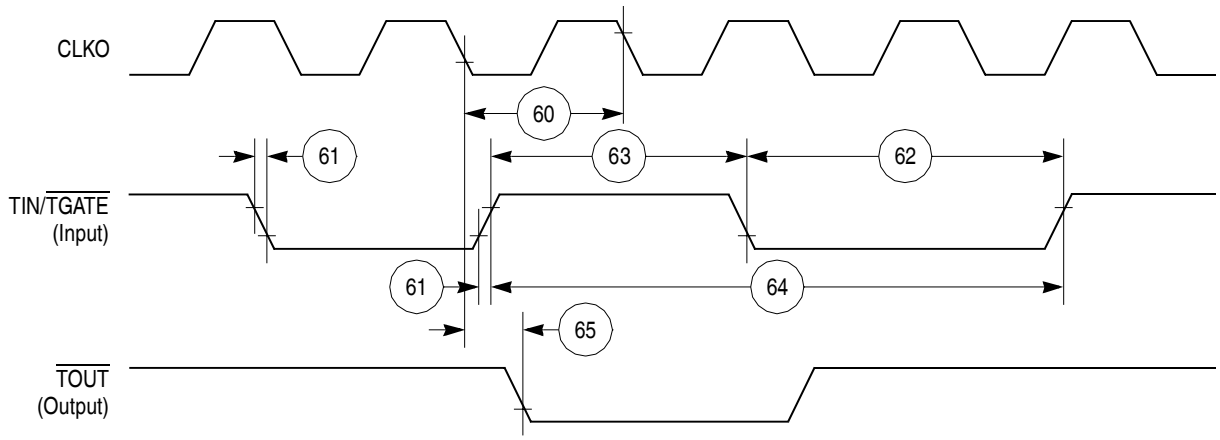


Figure 51. CPM General-Purpose Timers Timing Diagram

11.6 Serial Interface AC Electrical Specifications

Table 19 provides the serial interface timings as shown in Figure 52 though Figure 56.

Table 19. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLK, L1TCLK frequency (DSC = 0) [1, 2]	—	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0) [2]	P + 10	—	ns
71a	L1RCLK, L1TCLK width high (DSC = 0) [3]	P + 10	—	ns
72	L1TXD, L1ST(1–4), $\overline{\text{L1RQ}}$, L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20.00	—	ns
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1–4) valid [4]	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1–4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1–4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid [4]	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns

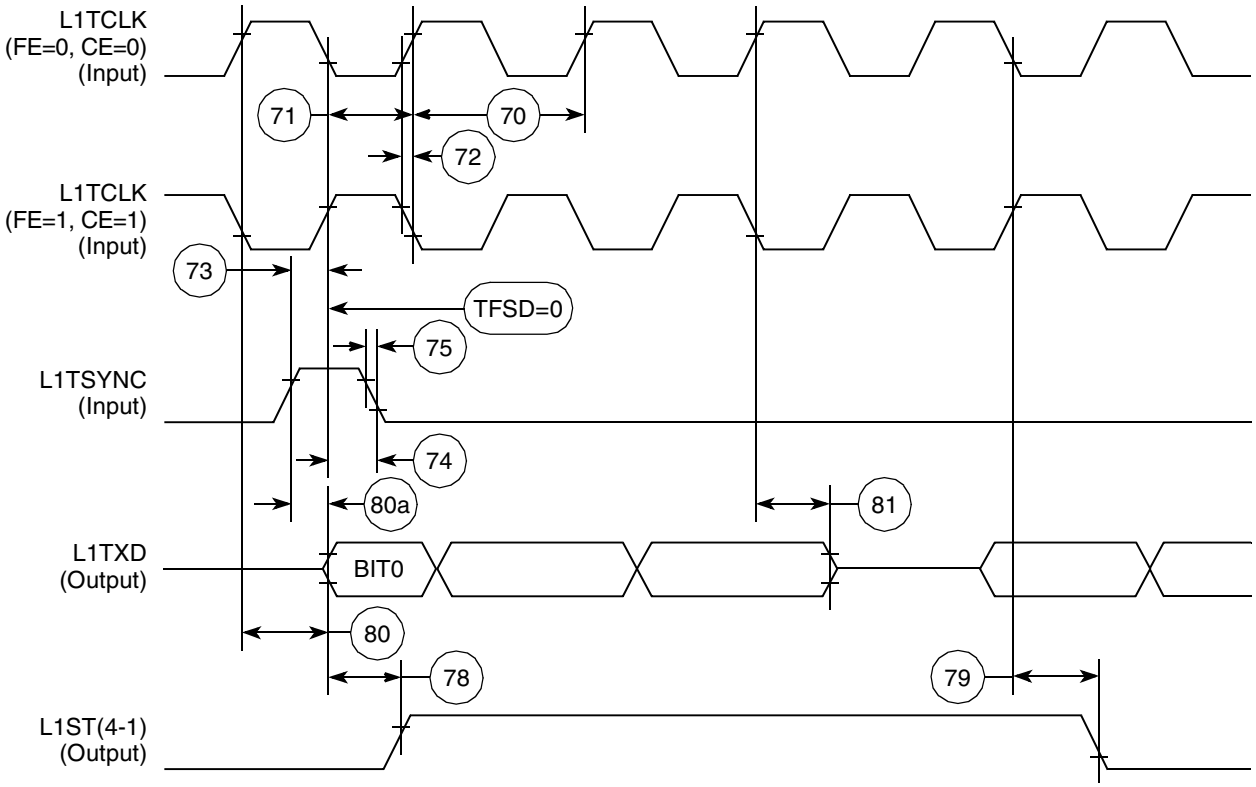


Figure 54. SI Transmit Timing Diagram (DSC = 0)

Table 22. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns
135	$\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted [2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2/1.

2 $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

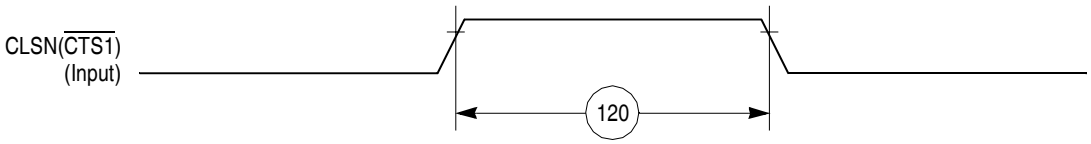


Figure 60. Ethernet Collision Timing Diagram

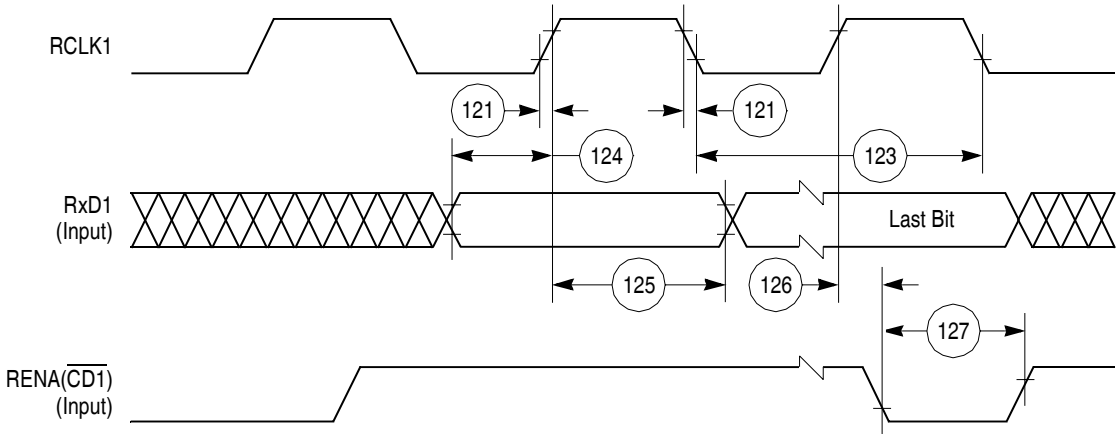
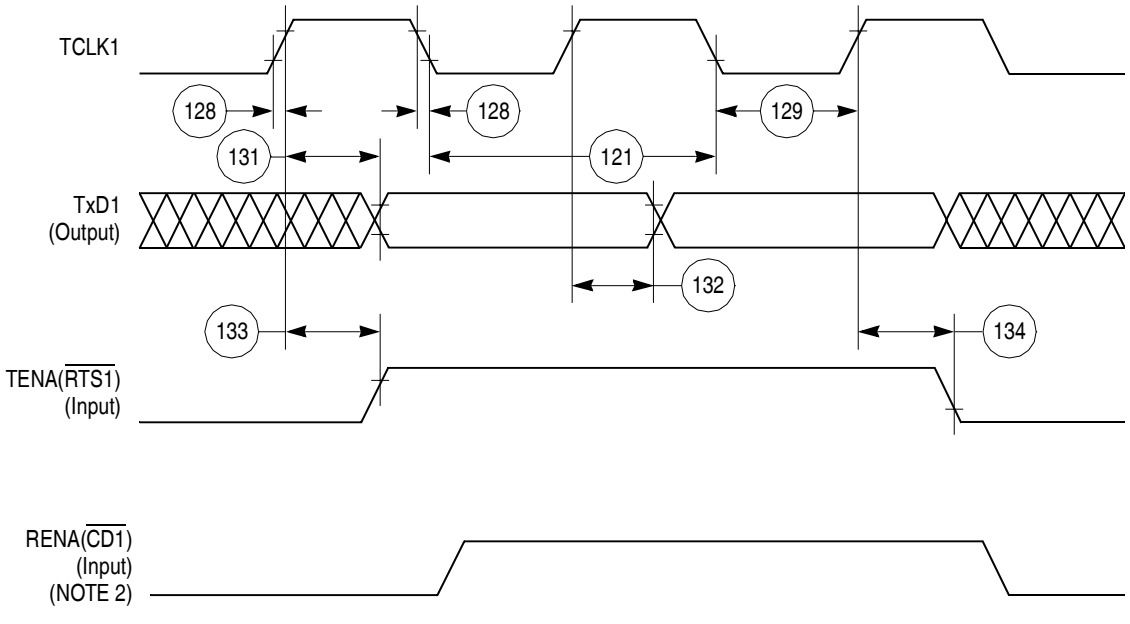


Figure 61. Ethernet Receive Timing Diagram



NOTES:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 62. Ethernet Transmit Timing Diagram

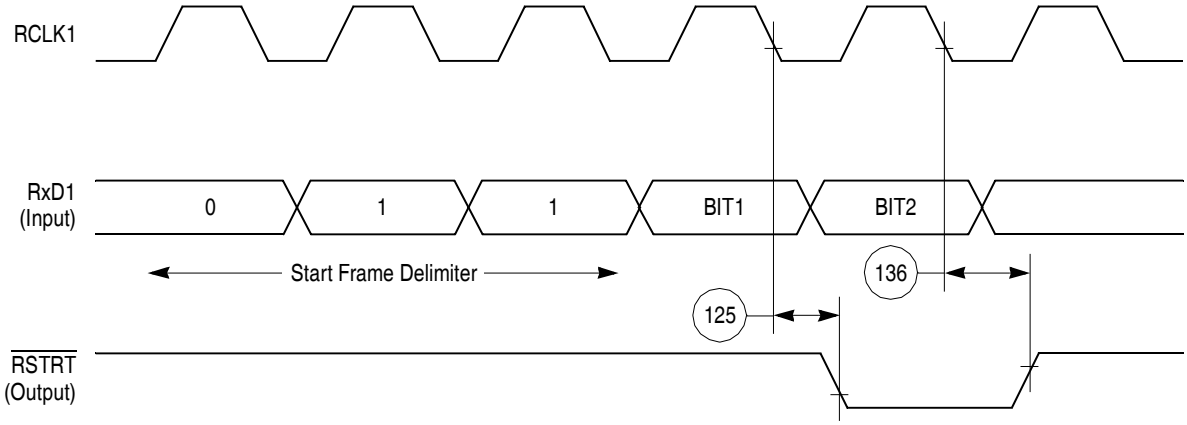


Figure 63. CAM Interface Receive Start Timing Diagram

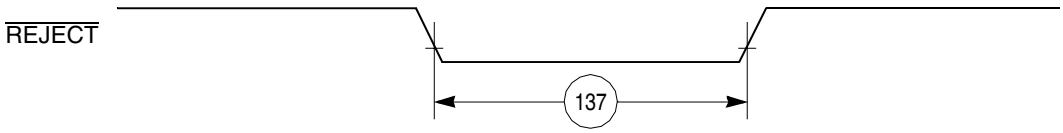


Figure 64. CAM Interface REJECT Timing Diagram

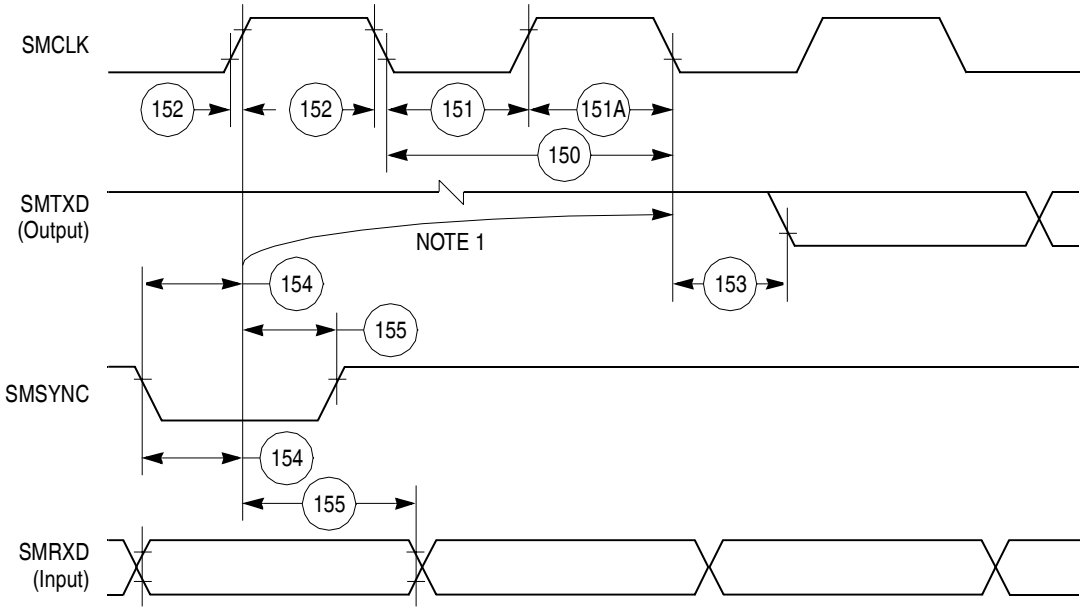
11.9 SMC Transparent AC Electrical Specifications

Table 23 provides the SMC transparent timings as shown in Figure 65.

Table 23. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period [1]	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

1 SyncCLK must be at least twice as fast as SMCLK.



NOTE:
1. This delay is equal to an integer number of character-length clocks.

Figure 65. SMC Transparent Timing Diagram

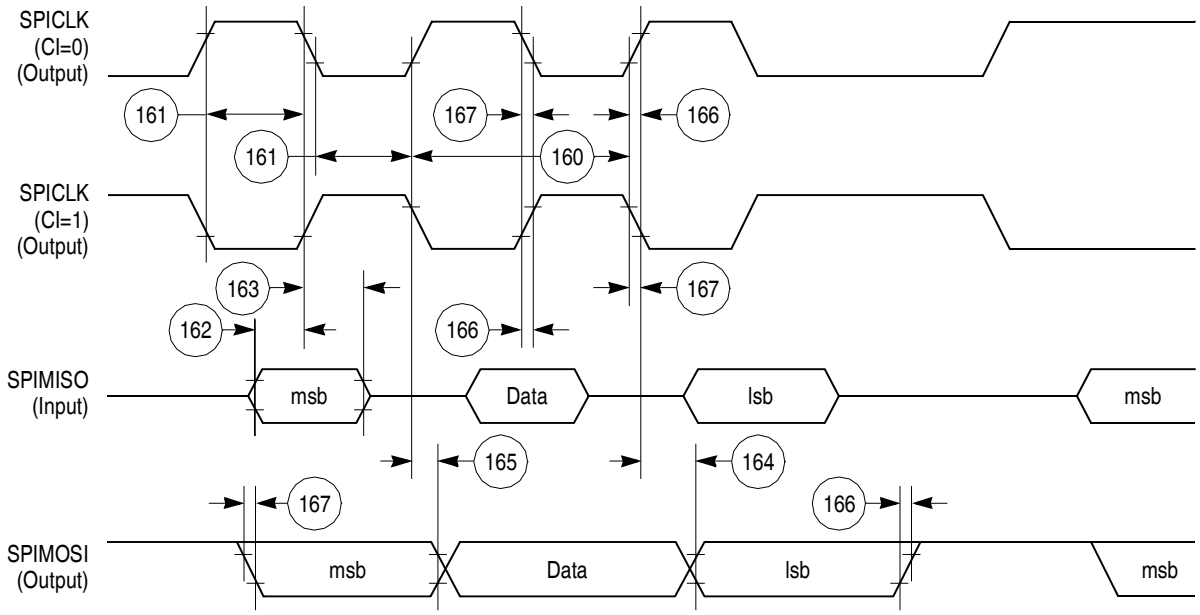


Figure 67. SPI Master (CP = 1) Timing Diagram

11.11 SPI Slave AC Electrical Specifications

Table 25 provides the SPI slave timings as shown in Figure 68 though Figure 69.

Table 25. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns

13.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency - 1%.

Table 29 provides information on the MII receive signal timing.

Table 29. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Figure 73 shows MII receive signal timing.

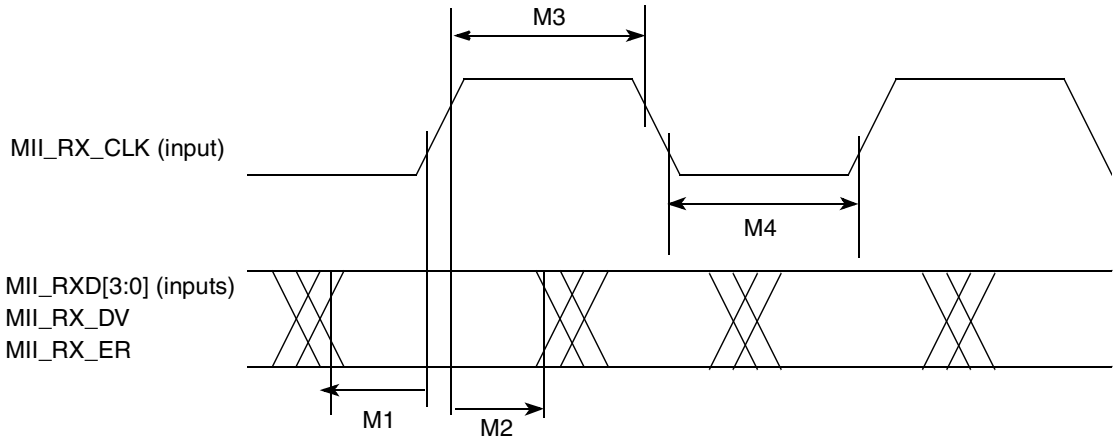


Figure 73. MII Receive Signal Timing Diagram

13.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency - 1%.

Table 30 provides information on the MII transmit signal timing.

Table 30. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	

NOTE: This is the top view of the device.

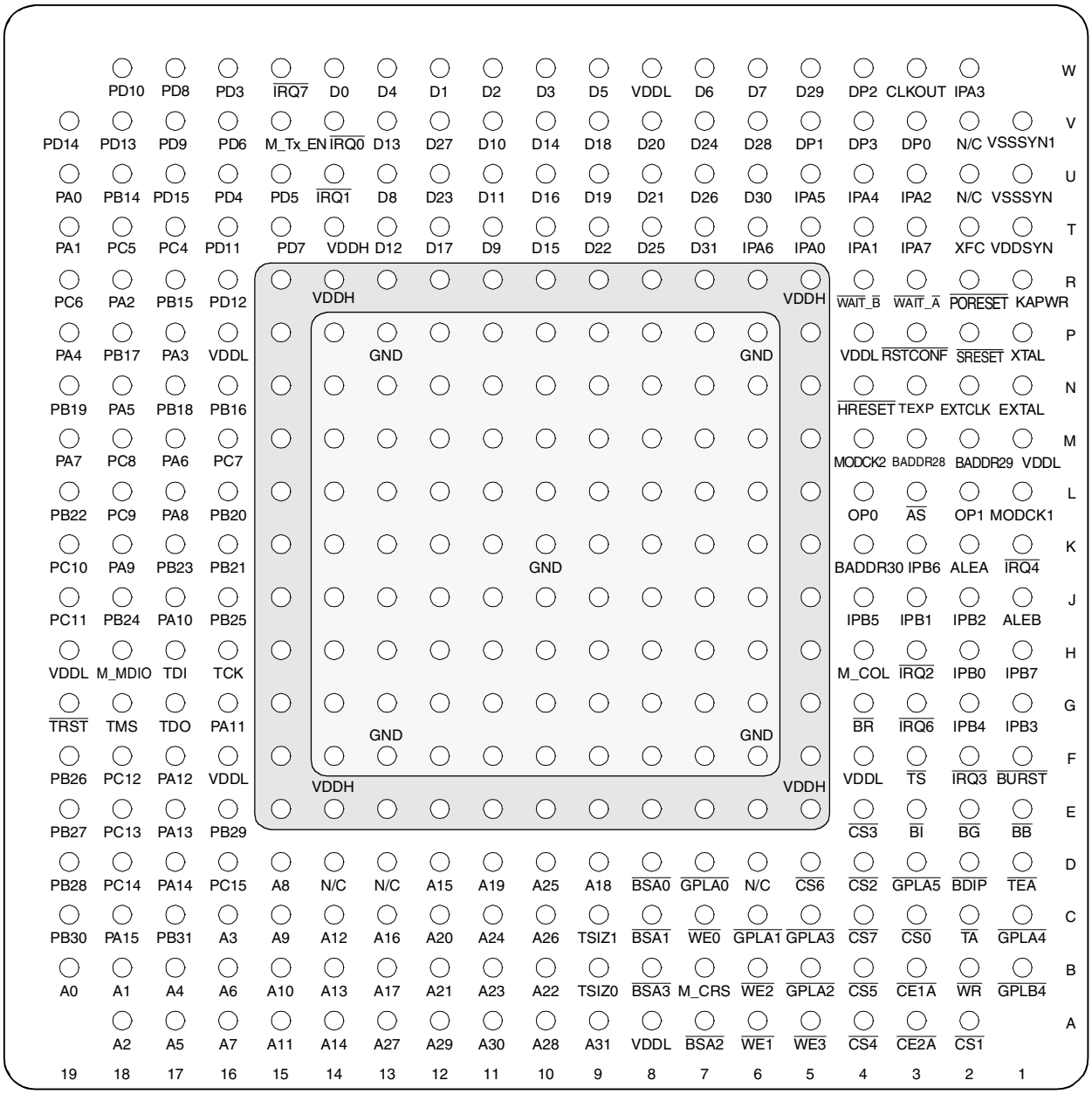


Figure 77. Pinout of the PBGA Package

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
PD12 L1RSYNCB MII-MDC UTPB3	R16	Bidirectional
PD11 RXD3 MII-TXERR $\overline{\text{RXENB}}$	T16	Bidirectional
PD10 TXD3 MII-RXD0 $\overline{\text{TXENB}}$	W18	Bidirectional
PD9 RXD4 MII-TXD0 UTPCLK	V17	Bidirectional
PD8 TXD4 MII-MDC MII-RXCLK	W17	Bidirectional
PD7 $\overline{\text{RTS3}}$ MII-RXERR UTPB4	T15	Bidirectional
PD6 $\overline{\text{RTS4}}$ MII-RXDV UTPB5	V16	Bidirectional
PD5 $\overline{\text{REJECT2}}$ MII-TXD3 UTPB6	U15	Bidirectional
PD4 $\overline{\text{REJECT3}}$ MII-TXD2 UTPB7	U16	Bidirectional
PD3 $\overline{\text{REJECT4}}$ MII-TXD1 SOC	W16	Bidirectional
TMS	G18	Input
TDI DSDI	H17	Input
TCK DSCK	H16	Input