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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc862tvr100b

- The MPC862/857T/857DSL provides enhanced ATM functionality over that of the MPC860SAR. The MPC862/857T/857DSL adds major new features available in “enhanced SAR” (ESAR) mode, including the following:
  - Improved operation, administration and maintenance (OAM) support
  - OAM performance monitoring (PM) support
  - Multiple APC priority levels available to support a range of traffic pace requirements
  - ATM port-to-port switching capability without the need for RAM-based microcode
  - Simultaneous MII (10/100Base-T) and UTOPIA (half-duplex) capability
  - Optional statistical cell counters per PHY
  - UTOPIA level 2 compliant interface with added FIFO buffering to reduce the total cell transmission time. (The earlier UTOPIA level 1 specification is also supported.)
  - Multi-PHY support on the MPC857T
  - Four PHY support on the MPC857DSL
  - Parameter RAM for both SPI and I^2C can be relocated without RAM-based microcode
  - Supports full-duplex UTOPIA both master (ATM side) and slave (PHY side) operation using a “split” bus
  - AAL2/VBR functionality is ROM-resident
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to Page mode/EDO/SDRAM, SRAM, EPROMs, flash EPROMs, and other memory devices.
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbyte–256 Mbyte)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers cascadable to be two 32-bit timers
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- Fast Ethernet controller (FEC)
  - Simultaneous MII (10/100Base-T) and UTOPIA operation when using the UTOPIA multiplexed bus.

Table 2. Maximum Tolerated Ratings (continued)

(GND = 0 V)

Rating	Symbol	Value	Unit	Max Freq (MHz)
Input voltage [2]	V_{in}	GND-0.3 to VDDH	V	-
Temperature [3] (standard) [4]	$T_{A(min)}$	0	°C	100
	$T_{j(max)}$	105	°C	100
Temperature [3] (extended)	$T_{A(min)}$	-40	°C	80
	$T_{j(max)}$	115	°C	80
Storage temperature range	T_{stg}	-55 to +150	°C	-

1 The power supply of the device must start its ramp from 0.0 V.

2 Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC862/857T/857DSL is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

3 Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j.

4 JTAG is tested only at ambient, not at standard maximum or extended maximum.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

Table 4. Power Dissipation (P_D) (continued)

Die Revision	Frequency	Typical [1]	Maximum [2]	Unit
A.1, B.0 (2:1 Mode)	66 MHz	910	1060	mW
	80 MHz	1.06	1.20	W
B.0 (2:1 Mode)	100 MHz	1.35	1.54	W

1 Typical power dissipation is measured at 3.3 V.

2 Maximum power dissipation is measured at 3.5 V.

NOTE

Values in Table 4 represent VDDL based power dissipation and do not include I/O power dissipation over VDDH. I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

6 DC Characteristics

Table 5 provides the DC electrical characteristics for the MPC862/857T/857DSL.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	VDDH, VDDL, KAPWR, VDDSYN	3.135	3.465	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	VDDH – 0.4	VDDH	V
Input High Voltage (all inputs except EXTAL and EXTCLK)	VIH	2.0	5.5	V
Input Low Voltage [1]	VIL	GND	0.8	V
EXTAL, EXTCLK Input High Voltage	VIHC	0.7*(VCC)	VCC+0.3	V
Input Leakage Current, Vin = 5.5 V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I_{in}	—	100	µA
Input Leakage Current, Vin = 3.6 V (Except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI)	I_{In}	—	10	µA
Input Leakage Current, Vin = 0 V (Except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI pins)	I_{In}	—	10	µA
Input Capacitance [2]	C_{in}	—	20	pF
Output High Voltage, IOH = -2.0 mA, VDDH = 3.0 V (Except XTAL, XFC, and Open drain pins)	VOH	2.4	—	V

Table 7 provides the bus operation timing for the MPC862/857T/857DSL at 33 MHz, 40 Mhz, 50 MHz and 66 Mhz.

The timing for the MPC862/857T/857DSL bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays.

Table 7. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	CLKOUT period	30.30	30.30	25.00	30.30	20.00	30.30	15.15	30.30	ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	-0.90	0.90	-0.90	0.90	-0.90	0.90	-0.90	0.90	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	-2.30	2.30	-2.30	2.30	-2.30	2.30	-2.30	2.30	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) [1]	-0.60	0.60	-0.60	0.60	-0.60	0.60	-0.60	0.60	ns
B1d	CLKOUT phase jitter[1]	-2.00	2.00	-2.00	2.00	-2.00	2.00	-2.00	2.00	ns
B1e	CLKOUT frequency jitter (MF < 10) [1]	—	0.50	—	0.50	—	0.50	—	0.50	%
B1f	CLKOUT frequency jitter (10 < MF < 500) [1]	—	2.00	—	2.00	—	2.00	—	2.00	%
B1g	CLKOUT frequency jitter (MF > 500) [1]	—	3.00	—	3.00	—	3.00	—	3.00	%
B1h	Frequency jitter on EXTCLK [2]	—	0.50	—	0.50	—	0.50	—	0.50	%
B2	CLKOUT pulse width low (MIN = 0.040 x B1)	12.10	—	10.00	—	8.00	—	6.10	—	ns
B3	CLKOUT width high (MIN = 0.040 x B1)	12.10	—	10.00	—	8.00	—	6.10	—	ns
B4	CLKOUT rise time [3] (MAX = 0.00 x B1 + 4.00)	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5[33]	CLKOUT fall time[3] (MAX = 0.00 x B1 + 4.00)	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) invalid (MIN = 0.25 x B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), $\overline{BDIP}$, PTR invalid (MIN = 0.25 x B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ invalid [4] (MIN = 0.25 x B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) valid (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29d	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29e	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29f	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 6.30)	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29g	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 - 6.30)	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29h	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns
B29i	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 - 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns
B30	$\overline{CS}$, $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) Invalid GPCM write access [11] (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B30a	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) Invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT =1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B30b	$\overline{WE}$(0:3) negated to A(0:31) Invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B32c	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 x B1 + 6.60)	9.40	18.00	7.60	16.00	13.30	14.10	11.30	12.30	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid - as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{GPL}$ Valid - as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by CST2 in the corresponding word in UPM (MIN = 0.75 x B1 - 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid - as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - As Requested by BST1 in the corresponding word in the UPM (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 x B1 - 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns

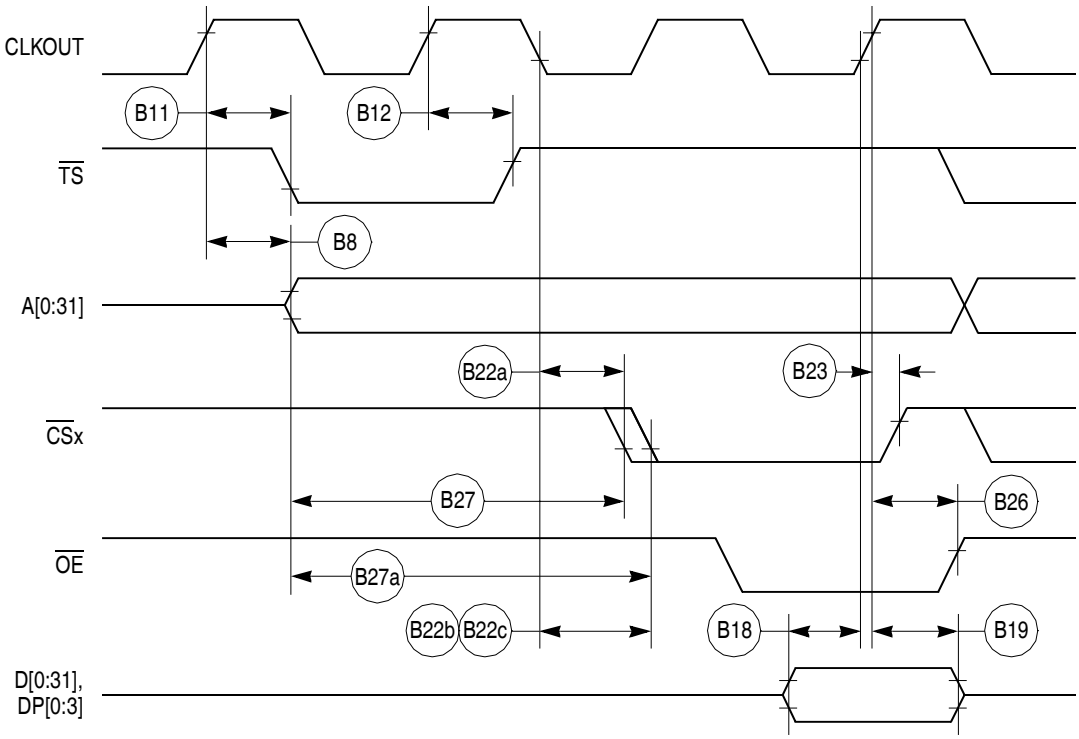

Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

Figure 21 provides the timing for the synchronous external master access controlled by the GPCM.

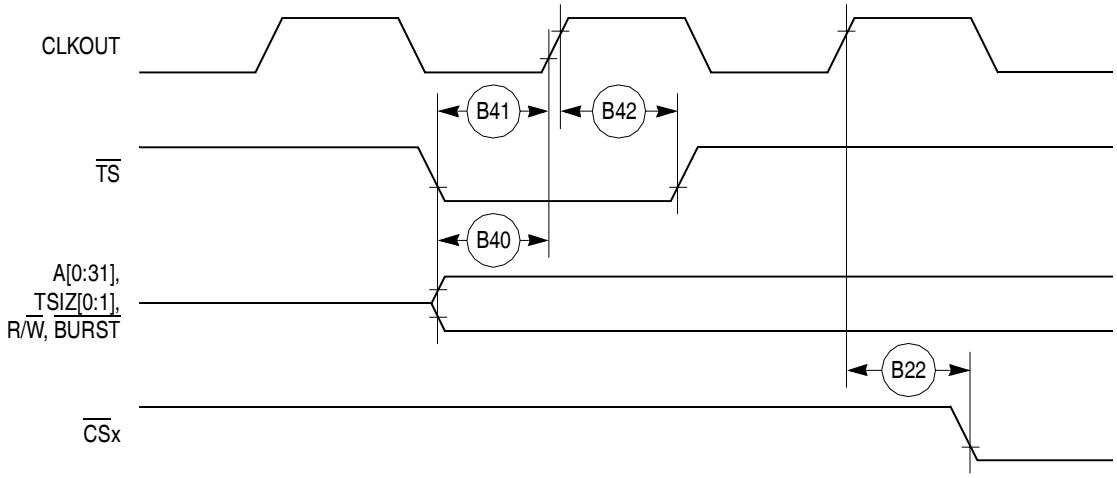

Figure 21. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 22 provides the timing for the asynchronous external master memory access controlled by the GPCM.

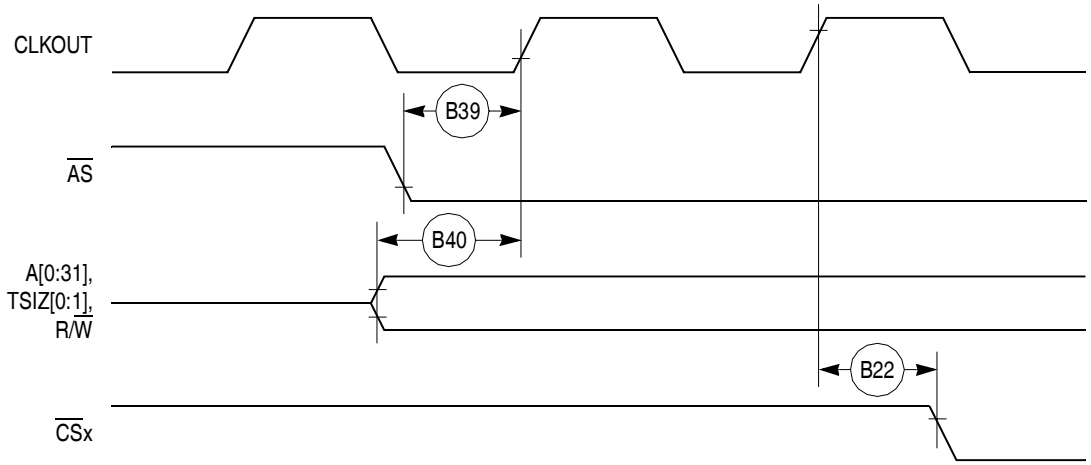

Figure 22. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 23 provides the timing for the asynchronous external master control signals negation.

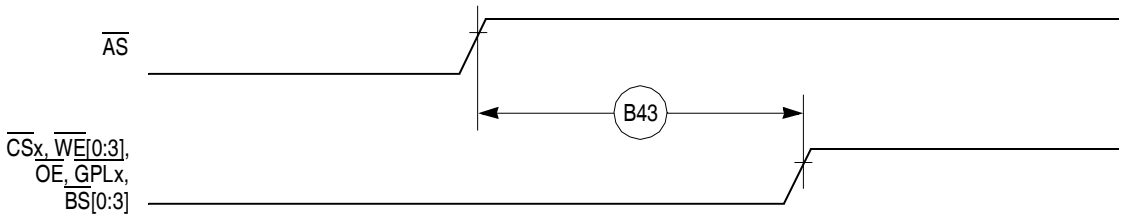

Figure 23. Asynchronous External Master—Control Signals Negation Timing

Table 11 shows the debug port timing for the MPC862/857T/857DSL.

Table 11. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
D61	DSCK cycle time	3 x $T_{CLOCKOUT}$		-
D62	DSCK clock pulse width	1.25 x $T_{CLOCKOUT}$		-
D63	DSCK rise and fall times	0.00	3.00	ns
D64	DSDI input data setup time	8.00		ns
D65	DSDI data hold time	5.00		ns
D66	DSCK low to DSDO data valid	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 31 provides the input timing for the debug port clock.

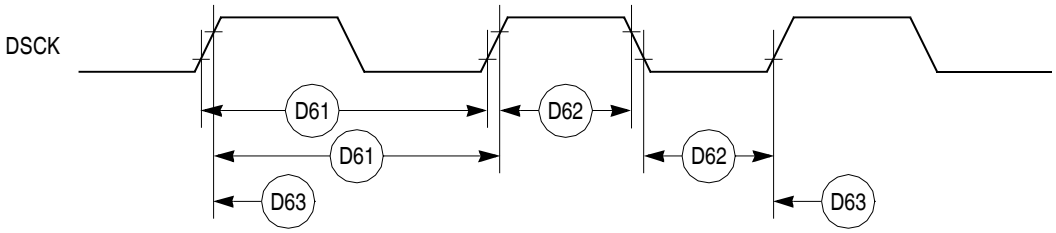

Figure 31. Debug Port Clock Input Timing

Figure 32 provides the timing for the debug port.

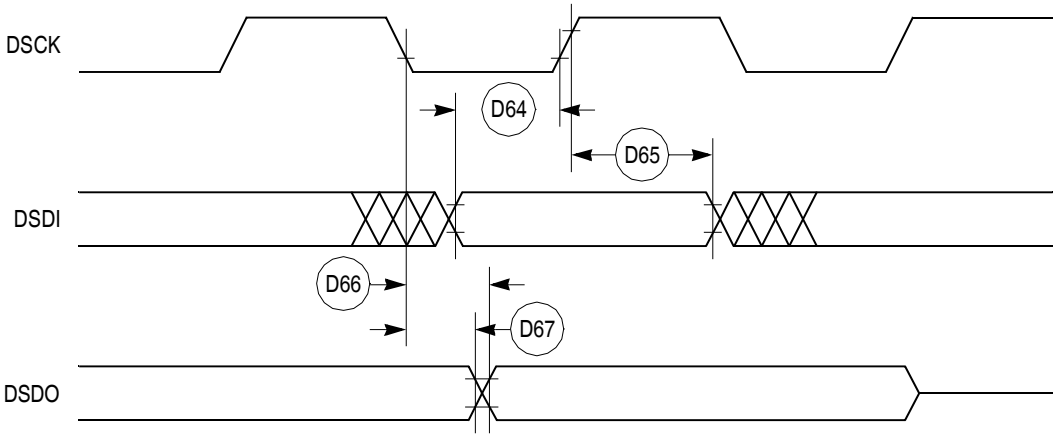

Figure 32. Debug Port Timings

Figure 35 provides the reset timing for the debug port configuration.

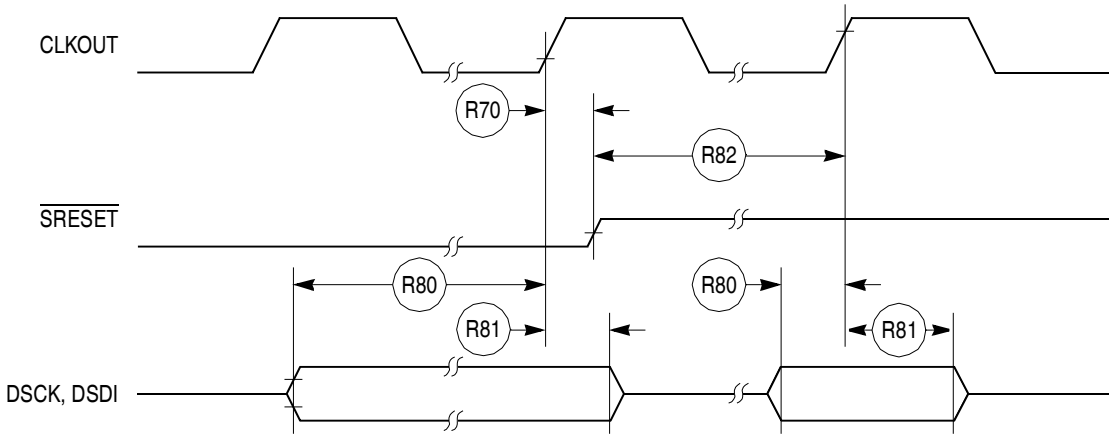

Figure 35. Reset Timing—Debug Port Configuration

10 IEEE 1149.1 Electrical Specifications

Table 13 provides the JTAG timings for the MPC862/857T/857DSL shown in Figure 36 though Figure 39.

Table 13. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

11 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC862/857T/857DSL.

11.1 PIP/PIO AC Electrical Specifications

Table 14 provides the PIP/PIO AC timings as shown in Figure 40 though Figure 44.

Table 14. PIP/PIO Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
21	Data-in setup time to STBI low	0	—	ns
22	Data-in hold time to STBI high	2.5 – t3 [1]	—	clk
23	STBI pulse width	1.5	—	clk
24	STBO pulse width	1 clk – 5 ns	—	ns
25	Data-out setup time to STBO low	2	—	clk
26	Data-out hold time from STBO high	5	—	clk
27	STBI low to STBO low (Rx interlock)	—	2	clk
28	STBI low to STBO high (Tx interlock)	2	—	clk
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns

1 t3 = Specification 23

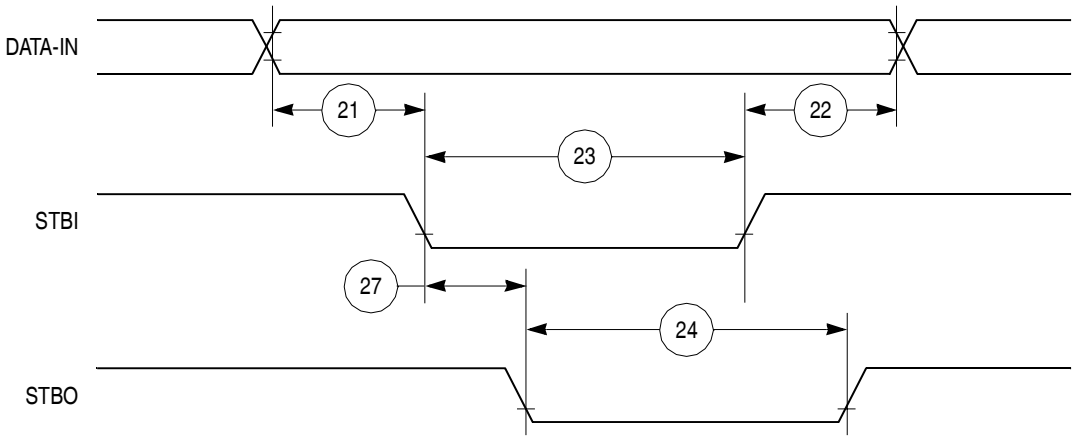

Figure 40. PIP Rx (Interlock Mode) Timing Diagram

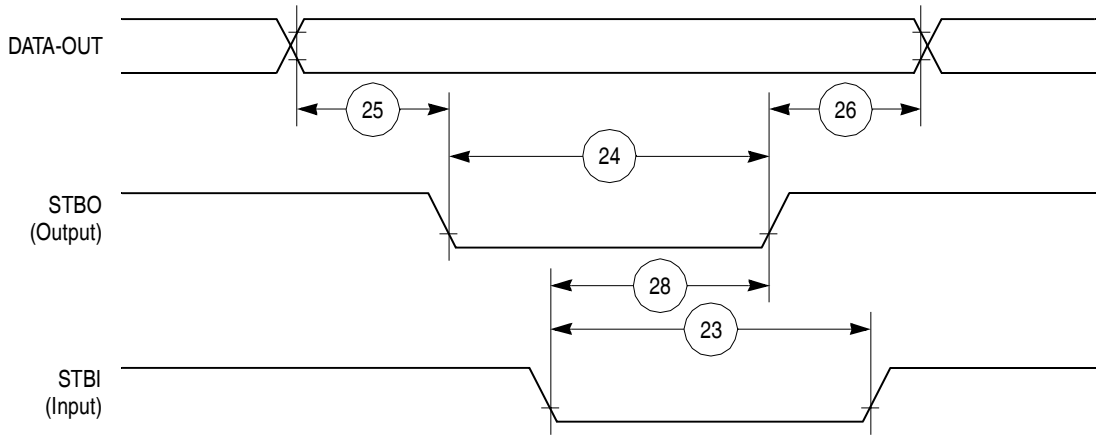

Figure 41. PIP Tx (Interlock Mode) Timing Diagram

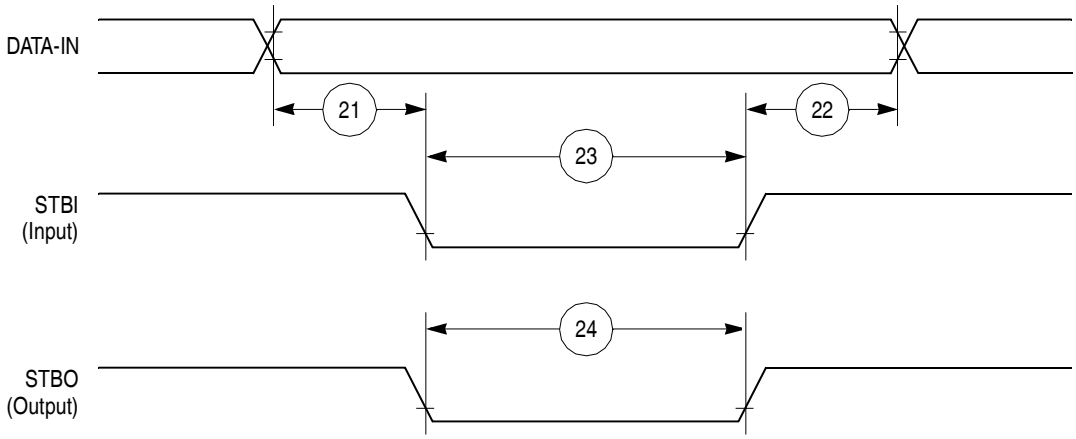

Figure 42. PIP Rx (Pulse Mode) Timing Diagram

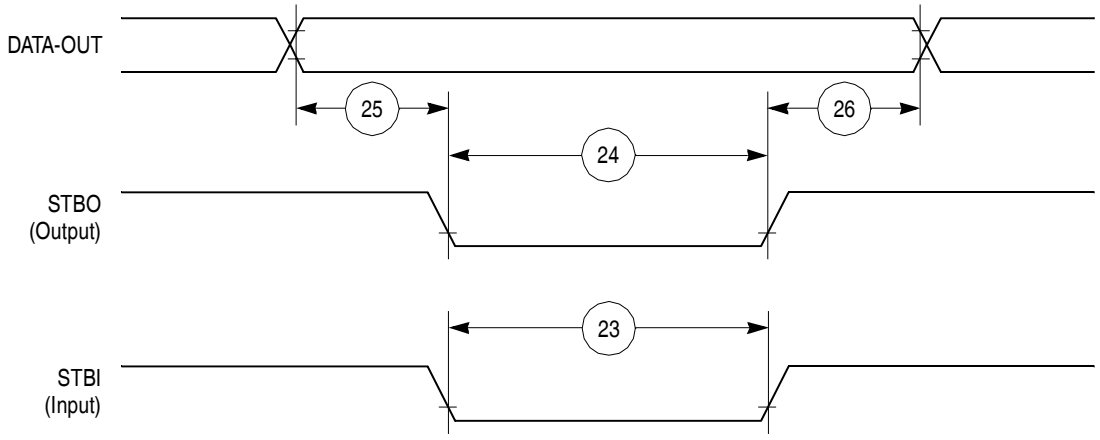

Figure 43. PIP TX (Pulse Mode) Timing Diagram

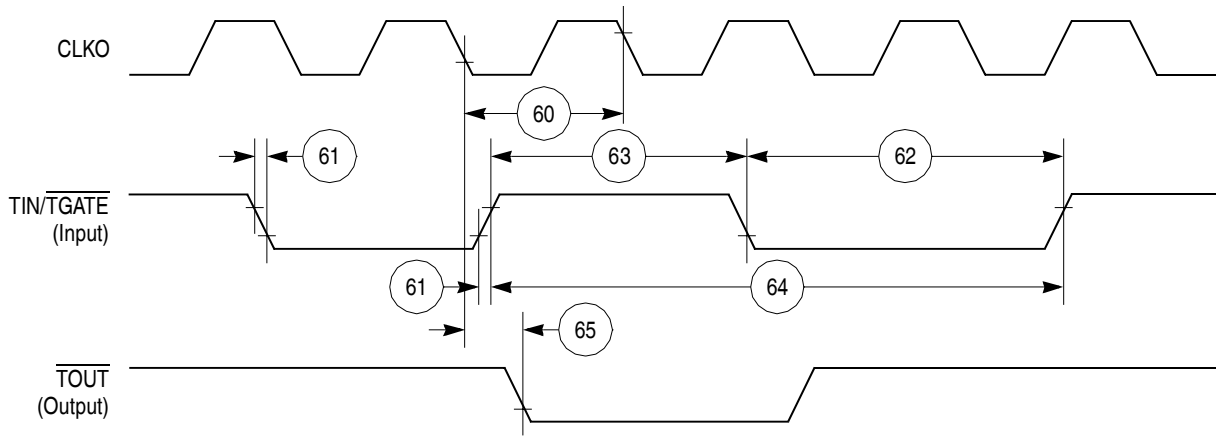

Figure 51. CPM General-Purpose Timers Timing Diagram

11.6 Serial Interface AC Electrical Specifications

Table 19 provides the serial interface timings as shown in Figure 52 though Figure 56.

Table 19. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLK, L1TCLK frequency (DSC = 0) [1, 2]	—	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0) [2]	P + 10	—	ns
71a	L1RCLK, L1TCLK width high (DSC = 0) [3]	P + 10	—	ns
72	L1TXD, L1ST(1–4), $\overline{\text{L1RQ}}$, L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20.00	—	ns
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1–4) valid [4]	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1–4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1–4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid [4]	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns

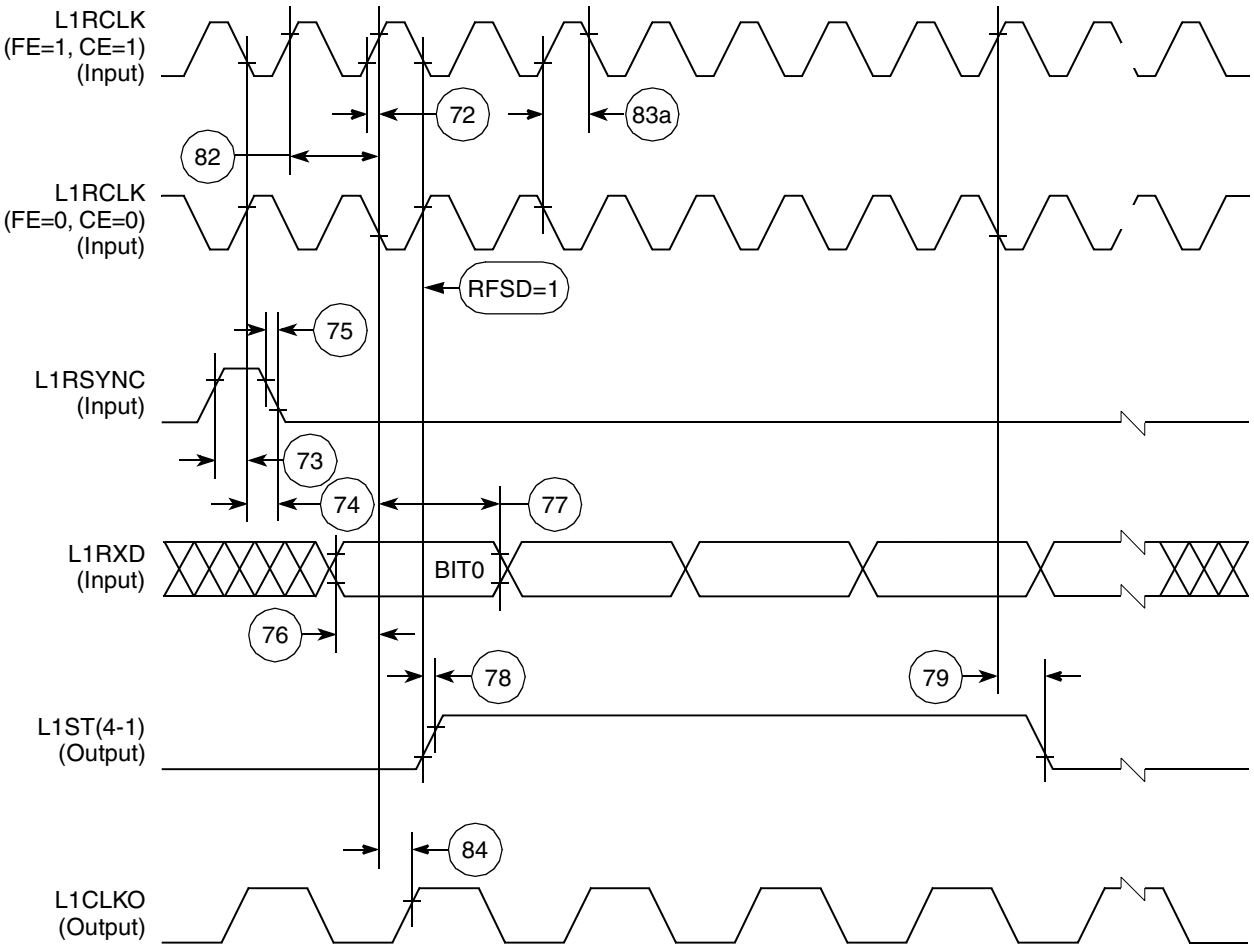

Figure 53. SI Receive Timing with Double-Speed Clocking (DSC = 1)

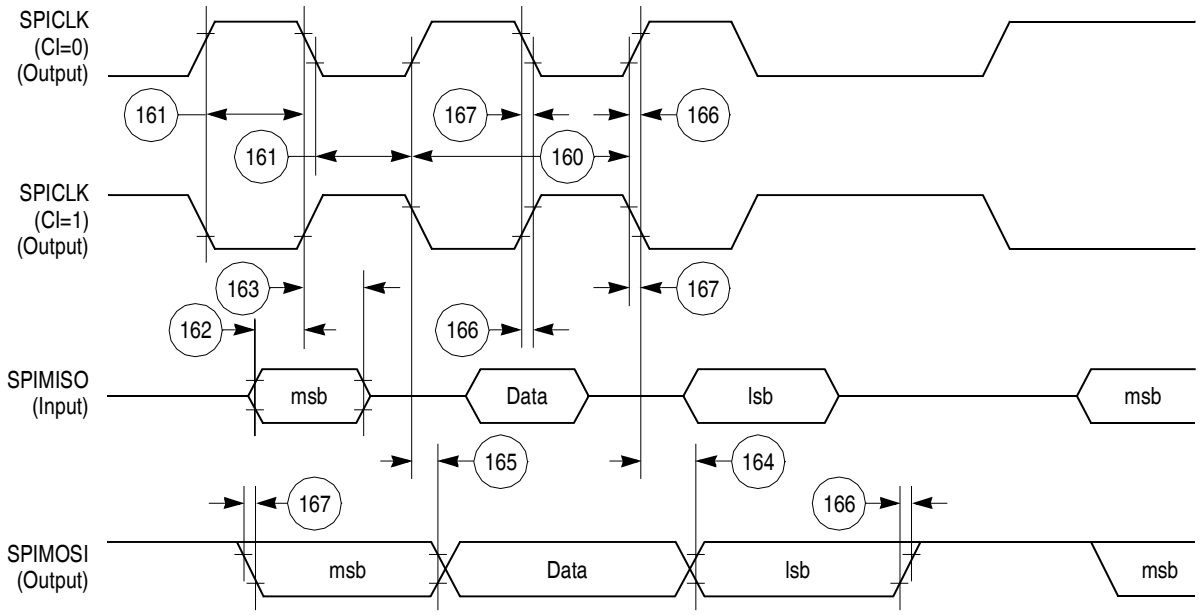

Figure 67. SPI Master (CP = 1) Timing Diagram

11.11 SPI Slave AC Electrical Specifications

Table 25 provides the SPI slave timings as shown in Figure 68 though Figure 69.

Table 25. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns

13.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency - 1%.

Table 29 provides information on the MII receive signal timing.

Table 29. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Figure 73 shows MII receive signal timing.

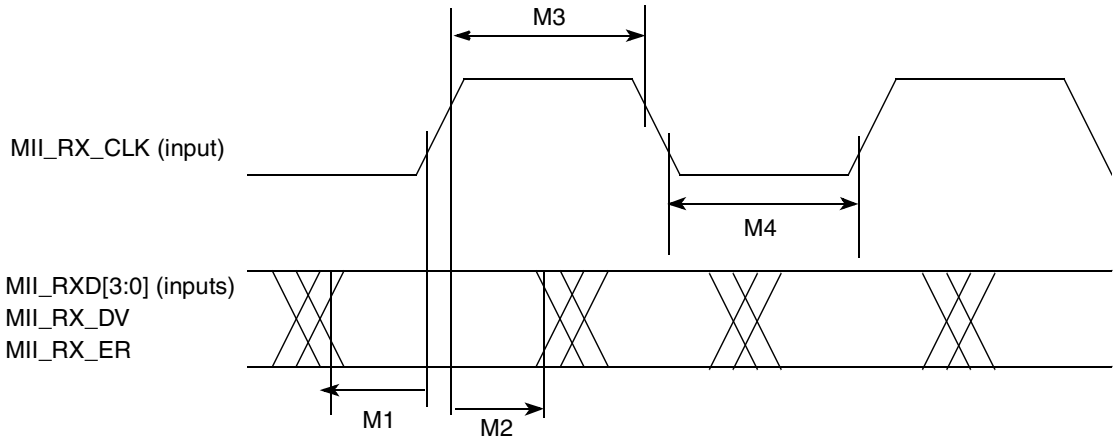

Figure 73. MII Receive Signal Timing Diagram

13.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency - 1%.

Table 30 provides information on the MII transmit signal timing.

Table 30. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	

Table 33. MPC862/857T/857DSL Derivatives (continued)

Device	Number of SCCs [1]	Ethernet Support	Multi-Channel HDLC Support	ATM Support	Cache Size	
					Instruction	Data
MPC857T	One (SCC1)	10/100 Mbps	Yes	Yes	4 Kbytes	4 Kbytes
MPC857DSL	One (SCC1)	10/100 Mbps	No	Up to 4 addresses	4 Kbytes	4 Kbytes

1 Serial communications controller (SCC)

Table 34 identifies the packages and operating frequencies orderable for the MPC862/857T/857DSL derivative devices.

Table 34. MPC862/857T/857DSL Package/Frequency Orderable

Package Type	Temperature (Tj)	Frequency (MHz)	Order Number
Plastic ball grid array (ZP suffix)	0°C to 105°C	50	XPC862PZP50B XPC862TZP50B XPC857TZP50B XPC857DSLZP50B
		66	XPC862PZP66B XPC862TZP66B XPC857TZP66B XPC857DSLZP66B
		80	XPC862PZP80B XPC862TZP80B XPC857TZP80B
		100	XPC862PZP100B XPC862TZP100B XPC857TZP100B
Plastic ball grid array (CZP suffix)	-40°C to 115°C	66 [1]	XPC862PCZP66B XPC857TCZP66B

1 Additional extended temperature devices can be made available at 50MHz, 66MHz, and 80MHz

14.1 .Pin Assignments

Figure 77 shows the top view pinout of the PBGA package. For additional information, see the *MPC862 PowerQUICC Family User s Manual*.

Table 35 contains a list of the MPC862 input and output signals and shows multiplexing and pin assignments.

Table 35. Pin Assignments

Name	Pin Number	Type
A[0:31]	B19, B18, A18, C16, B17, A17, B16, A16, D15, C15, B15, A15, C14, B14, A14, D12, C13, B13, D9, D11, C12, B12, B10, B11, C11, D10, C10, A13, A10, A12, A11, A9	Bidirectional Three-state
TSIZ0 REG	B9	Bidirectional Three-state
TSIZ1	C9	Bidirectional Three-state
RD/WR	B2	Bidirectional Three-state
BURST	F1	Bidirectional Three-state
BDIP GPL_B5	D2	Output
TS	F3	Bidirectional Active Pull-up
TA	C2	Bidirectional Active Pull-up
TEA	D1	Open-drain
BI	E3	Bidirectional Active Pull-up
IRQ2 RSV	H3	Bidirectional Three-state
IRQ4 KR RETRY SPKROUT	K1	Bidirectional Three-state
CR IRQ3	F2	Input
D[0:31]	W14, W12, W11, W10, W13, W9, W7, W6, U13, T11, V11, U11, T13, V13, V10, T10, U10, T12, V9, U9, V8, U8, T9, U12, V7, T8, U7, V12, V6, W5, U6, T7	Bidirectional Three-state
DP0 IRQ3	V3	Bidirectional Three-state
DP1 IRQ4	V5	Bidirectional Three-state
DP2 IRQ5	W4	Bidirectional Three-state
DP3 IRQ6	V4	Bidirectional Three-state

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
PA2 CLK6 TOUT3 L1RCLKB	R18	Bidirectional
PA1 CLK7 BRGO4 TIN4	T19	Bidirectional
PA0 CLK8 TOUT4 L1TCLKB	U19	Bidirectional
PB31 SPISEL REJECT1	C17	Bidirectional (Optional: Open-drain)
PB30 SPICLK RSTRT2	C19	Bidirectional (Optional: Open-drain)
PB29 SPIMOSI	E16	Bidirectional (Optional: Open-drain)
PB28 SPIMISO BRGO4	D19	Bidirectional (Optional: Open-drain)
PB27 I2CSDA BRGO1	E19	Bidirectional (Optional: Open-drain)
PB26 I2CSCL BRGO2	F19	Bidirectional (Optional: Open-drain)
PB25 RXADDR3[2] SMTXD1	J16	Bidirectional (Optional: Open-drain)
PB24 TXADDR3[2] SMRXD1	J18	Bidirectional (Optional: Open-drain)
PB23 TXADDR2[2] SDACK1 SMSYN1	K17	Bidirectional (Optional: Open-drain)
PB22 TXADDR4[2] SDACK2 SMSYN2	L19	Bidirectional (Optional: Open-drain)

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