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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc862tvr66b

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Features

- Universal asynchronous receiver transmitter (UART)
- Synchronous UART
- Serial infrared (IrDA)
- Binary synchronous communication (BISYNC)
- Totally transparent (bit streams)
- Totally transparent (frame based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels) (The MPC857DSL has one SMC, SMC1 for UART)
 - UART
 - Transparent
 - General circuit interface (GCI) controller
 - Can be connected to the time-division multiplexed (TDM) channels
- One serial peripheral interface (SPI)
 - Supports master and slave modes
 - Supports multiple-master operation on the same bus
- One inter-integrated circuit (I²C) port
 - Supports master and slave modes
 - Multiple-master environment support
- Time-slot assigner (TSA) (The MPC857DSL does not have the TSA)
 - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame synchronization, clocking
 - Allows dynamic changes
 - On the MPC862P and MPC862T, can be internally connected to six serial channels (four SCCs and two SMCs); on the MPC857T, can be connected to three serial channels (one SCC and two SMCs)
- Parallel interface port (PIP)
 - Centronics interface support
 - Supports fast connection between compatible ports on MPC862/857T/857DSL or MC68360
- PCMCIA interface
 - Master (socket) interface, release 2.1 compliant
 - Supports one or two PCMCIA sockets dependent upon whether ESAR functionality is enabled
 - 8 memory or I/O windows supported
- Low power support
 - Full on—All units fully powered
 - Doze—Core functional units disabled except time base decrementer, PLL, memory controller, RTC, and CPM in low-power standby



Features

- Sleep—All units disabled except RTC, PIT, time base, and decrementer with PLL active for fast wake up
- Deep sleep—All units disabled including PLL except RTC, PIT, time base, and decrementer.
- Power down mode- All units powered down except PLL, RTC, PIT, time base and
- decrementerDebug interface
 - Eight comparators: four operate on instruction address, two operate on data address, and two
 operate on data
 - Supports conditions: $= \neq < >$
 - Each watchpoint can generate a break point internally
- 3.3 V operation with 5-V TTL compatibility except EXTAL and EXTCLK
- 357-pin plastic ball grid array (PBGA) package
- Operation up to 100MHz

The MPC862/857T/857DSL is comprised of three modules that each use the 32-bit internal bus: the MPC8xx core, the system integration unit (SIU), and the communication processor module (CPM). The MPC862P/862T block diagram is shown in Figure 1. The MPC857T/857DSL block diagram is shown in Figure 2.



Thermal Calculation and Measurement

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_{J} = T_{B} + (R_{\theta JB} \times P_{D})$$

where:

 $R_{\theta JB}$ = junction-to-board thermal resistance (°C/W)

 T_{B} = board temperature (°C)

 P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

 Ψ_{IT} = thermal characterization parameter

 T_T = thermocouple temperature on top of package

 P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.



Nume	n Characteristic Min Max Min Max		MHz	50 MHz		66 MHz		11		
NUM			Max	Min	Max	Min	Мах	Min	Max	Unit
B27	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 x B1 - 2.00)	35.90		29.30		23.00		16.90		ns
B27a	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	_	20.70	_	ns
B28	CLKOUT rising edge to $\overline{WE}(0:3)$ negated GPCM write access CSNT = 0 (MAX = 0.00 x B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, 1, CSNT = 1, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0,1, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	_	14.30	_	13.00	_	11.80	_	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0,1, CSNT = 1, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B28d	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0,1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	_	18.00	_	18.00	_	14.30	_	12.30	ns
B29	WE(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	_	1.80	—	ns
B29a	WE(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	_	10.50	_	8.00	_	5.60	_	ns
B29b	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3), High Z GPCM write access, ACS = 00, TRLX = 0,1 & CSNT = 0 (MIN = 0.25 x B1 - 2.00)	5.60	_	4.30	_	3.00	—	1.80	_	ns
B29c	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	_	10.50	_	8.00	_	5.60	_	ns

Table 7. Bus Operation	i Timings	(continued)
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Figure 15 through Figure 17 provide the timing for the external bus write controlled by various GPCM factors.



Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0,1 CSNT = 0)







Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0,1 CSNT = 1)





Figure 17. External Bus Write Timing (GPCM Controlled—TRLX = 0,1, CSNT = 1)



Figure 19 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.



Cycles Timing

Figure 20 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.





Table 9 shows the PCMCIA timing for the MPC862/857T/857DSL.

Table 9. PCMCIA Timing

Num Characteristic		33 MHz		40 MHz		50 MHz		66 MHz		Unit
Num			Мах	Min	Max	Min	Max	Min	Max	Unit
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA Strobe asserted. ¹ (MIN = 0.75 x B1 - 2.00)	20.70	_	16.70	_	13.00	_	9.40	_	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation. ¹ (MIN = 1.00 x B1 - 2.00)	28.30	—	23.00	—	18.00	_	13.20	—	ns
P46	CLKOUT to REG valid (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P47	CLKOUT to REG Invalid. (MIN = 0.25 x B1 + 1.00)	8.60	_	7.30	_	6.00	_	4.80	_	ns
P48	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ asserted. (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P49	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ negated. (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P50	CLKOUT to \overrightarrow{PCOE} , \overrightarrow{IORD} , \overrightarrow{PCWE} , \overrightarrow{IOWR} assert time. (MAX = 0.00 x B1 + 11.00)	_	11.00	_	11.00	_	11.00	_	11.00	ns
P51	$\frac{\text{CLKOUT to } \overline{\text{PCOE}}, \overline{\text{IORD}}, \overline{\text{PCWE}},}{\overline{\text{IOWR}} \text{ negate time.} (MAX = 0.00 \text{ x})}$ $B1 + 11.00)$	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time (MAX = 0.25 x B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
P53	CLKOUT to ALE negate time (MAX = 0.25 x B1 + 8.00)	_	15.60	—	14.30	—	13.00	-	11.80	ns
P54	$\overline{\text{PCWE}}, \overline{\text{IOWR}} \text{ negated to } D(0:31)$ invalid. ¹ (MIN = 0.25 x B1 - 2.00)	5.60	_	4.30	_	3.00	_	1.80	_	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge. ¹ (MIN = 0.00 x B1 + 8.00)	8.00	—	8.00	—	8.00	_	8.00	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid. ¹ (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00		2.00	—	ns

¹ PSST = 1. Otherwise add PSST times cycle time.

PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the \overline{WAITx} signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The \overline{WAITx} assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the *MPC862 PowerQUICC User s Manual*.



Figure 26 provides the PCMCIA access cycle timing for the external bus read.



Figure 26. PCMCIA Access Cycles Timing External Bus Read



Table 11 shows the debug port timing for the MPC862/857T/857DSL.

Num	Characteristic	All Freq	Unit	
Nulli	Characteristic	Min	Мах	Unit
D61	DSCK cycle time	3 x T _{CLOCKOUT}		-
D62	DSCK clock pulse width	1.25 x T _{CLOCKOUT}		-
D63	DSCK rise and fall times	0.00	3.00	ns
D64	DSDI input data setup time	8.00		ns
D65	DSDI data hold time	5.00		ns
D66	DSCK low to DSDO data valid	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	ns

Table 11. Debug Port Timing

Figure 31 provides the input timing for the debug port clock.



Figure 31. Debug Port Clock Input Timing

Figure 32 provides the timing for the debug port.



Figure 32. Debug Port Timings







Figure 33. Reset Timing—Configuration from Data Bus

Figure 34 provides the reset timing for the data bus weak drive during configuration.



Figure 34. Reset Timing—Data Bus Weak Drive during Configuration



CPM Electrical Characteristics







Figure 42. PIP Rx (Pulse Mode) Timing Diagram



Figure 43. PIP TX (Pulse Mode) Timing Diagram



CPM Electrical Characteristics





CPM Electrical Characteristics

11.10 SPI Master AC Electrical Specifications

Table 24 provides the SPI master timings as shown in Figure 66 though Figure 67.

Table 24. SPI Master Timing

Num	Characteristic	All Freq	Unit	
Num			Мах	Onit
160	MASTER cycle time	4	1024	t _{cyc}
161	MASTER clock (SCK) high or low time	2	512	t _{cyc}
162	MASTER data setup time (inputs)	15	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	10	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns



Figure 66. SPI Master (CP = 0) Timing Diagram



11.12 I²C AC Electrical Specifications

Table 26 provides the I^2C (SCL < 100 KHz) timings.

Num	Characteristic	All Freq	Unit	
Num			Max	Unit
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master) ¹	1.5	100	kHz
202	Bus free time between transmissions		_	μs
203	Low period of SCL	4.7	_	μs
204	High period of SCL	4.0	_	μs
205	Start condition setup time	4.7	_	μs
206	Start condition hold time	4.0	_	μs
207	Data hold time	0	_	μs
208	Data setup time	250	_	ns
209	SDL/SCL rise time	_	1	μs
210	SDL/SCL fall time	_	300	ns
211	Stop condition setup time	4.7	_	μs

SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 27 provides the I^2C (SCL > 100 kHz) timings.

Table 27. I^2C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Freq	Unit	
Nulli	Characteristic	Expression	Min	Max	Onit
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) ¹	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	_	1/(2.2 * fSCL)	_	S
203	Low period of SCL	—	1/(2.2 * fSCL)	_	S
204	High period of SCL	—	1/(2.2 * fSCL)	_	S
205	Start condition setup time	—	1/(2.2 * fSCL)	_	S
206	Start condition hold time	—	1/(2.2 * fSCL)	_	S
207	Data hold time	—	0	_	S
208	Data setup time	—	1/(40 * fSCL)	_	S
209	SDL/SCL rise time	_	_	1/(10 * fSCL)	S
210	SDL/SCL fall time	—	—	1/(33 * fSCL)	S
211	Stop condition setup time	—	1/2(2.2 * fSCL)	_	S

SCL frequency is given by SCL = BrgClk_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

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Num	Characteristic	Min	Мах	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	_	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	_	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	_	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	_	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period



Figure 76 shows the MII serial management channel timing diagram.



Figure 76. MII Serial Management Channel Timing Diagram

14 Mechanical Data and Ordering Information

Table 33 provides information on the MPC862/857T/857DSL derivative devices.

Table 33. MPC862/857T/857DSL Derivatives

Device	Number	Ethernet	Multi-Channel	ATM Support	Cache	e Size
Device	SCCs ¹	Support	HDLC Support		Instruction	Data
MPC862T	Four	10/100 Mbps	Yes	Yes	4 Kbytes	4 Kbytes
MPC862P	Four	10/100 Mbps	Yes	Yes	16 Kbytes	8 Kbytes



Name	Pin Number	Туре
PA15 RXD1 RXD4	C18	Bidirectional
PA14 TXD1 TXD4	D17	Bidirectional (Optional: Open-drain)
PA13 RXD2	E17	Bidirectional
PA12 TXD2	F17	Bidirectional (Optional: Open-drain)
PA11 L1TXDB RXD3	G16	Bidirectional (Optional: Open-drain)
PA10 L1RXDB TXD3	J17	Bidirectional (Optional: Open-drain)
PA9 L1TXDA	К18	Bidirectional (Optional: Open-drain)
RXD4		
PA8 L1RXDA TXD4	L17	Bidirectional (Optional: Open-drain)
PA7 CLK1 L1RCLKA BRGO1 TIN1	M19	Bidirectional
PA6 CLK2 TOUT1	M17	Bidirectional
PA5 CLK3 L1TCLKA BRGO2 TIN2	N18	Bidirectional
PA4 CLK4 TOUT2	P19	Bidirectional
PA3 CLK5 BRGO3 TIN3	P17	Bidirectional

Table 35. Pin Assignments (continued)



Name	Pin Number	Туре
PA2 CLK6 TOUT3 L1RCLKB	R18	Bidirectional
PA1 CLK7 BRGO4 TIN4	T19	Bidirectional
PA0 CLK8 TOUT4 L1TCLKB	U19	Bidirectional
PB31 SPISEL REJECT1	C17	Bidirectional (Optional: Open-drain)
PB30 SPICLK RSTRT2	C19	Bidirectional (Optional: Open-drain)
PB29 SPIMOSI	E16	Bidirectional (Optional: Open-drain)
PB28 SPIMISO BRGO4	D19	Bidirectional (Optional: Open-drain)
PB27 I2CSDA BRGO1	E19	Bidirectional (Optional: Open-drain)
PB26 I2CSCL BRGO2	F19	Bidirectional (Optional: Open-drain)
PB25 RXADDR3 ² SMTXD1	J16	Bidirectional (Optional: Open-drain)
PB24 TXADDR3 ² SMRXD1	J18	Bidirectional (Optional: Open-drain)
PB23 TXADDR2 ² SDACK1 SMSYN1	K17	Bidirectional (Optional: Open-drain)
PB22 TXADDR4 ² SDACK2 SMSYN2	L19	Bidirectional (Optional: Open-drain)

Table 35. Pin Assignments (continued)



Mechanical Data and Ordering Information







SIDE VIEW

NOTES:

- 1. Dimensions and tolerancing per ASME Y14.5M, 1994.
- 2. Dimensions in millimeters.
- 3. Dimension b is the maximum solder ball diameter measured parallel to datum C.

	MILLIMETERS		
DIM	MIN	MAX	
Α		2.05	
A1	0.50	0.70	
A2	0.95	1.35	
A3	0.70	0.90	
b	0.60	0.90	
D	25.00 BSC		
D1	22.86 BSC		
D2	22.40	22.60	
е	1.27 BSC		
Е	25.00 BSC		
E1	22.86 BSC		
E2	22.40	22.60	

Case No. 1103-01



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