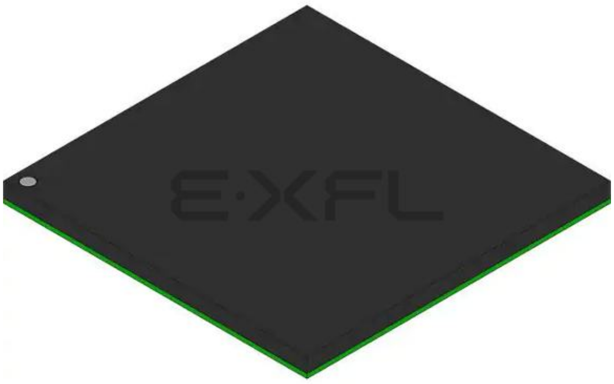

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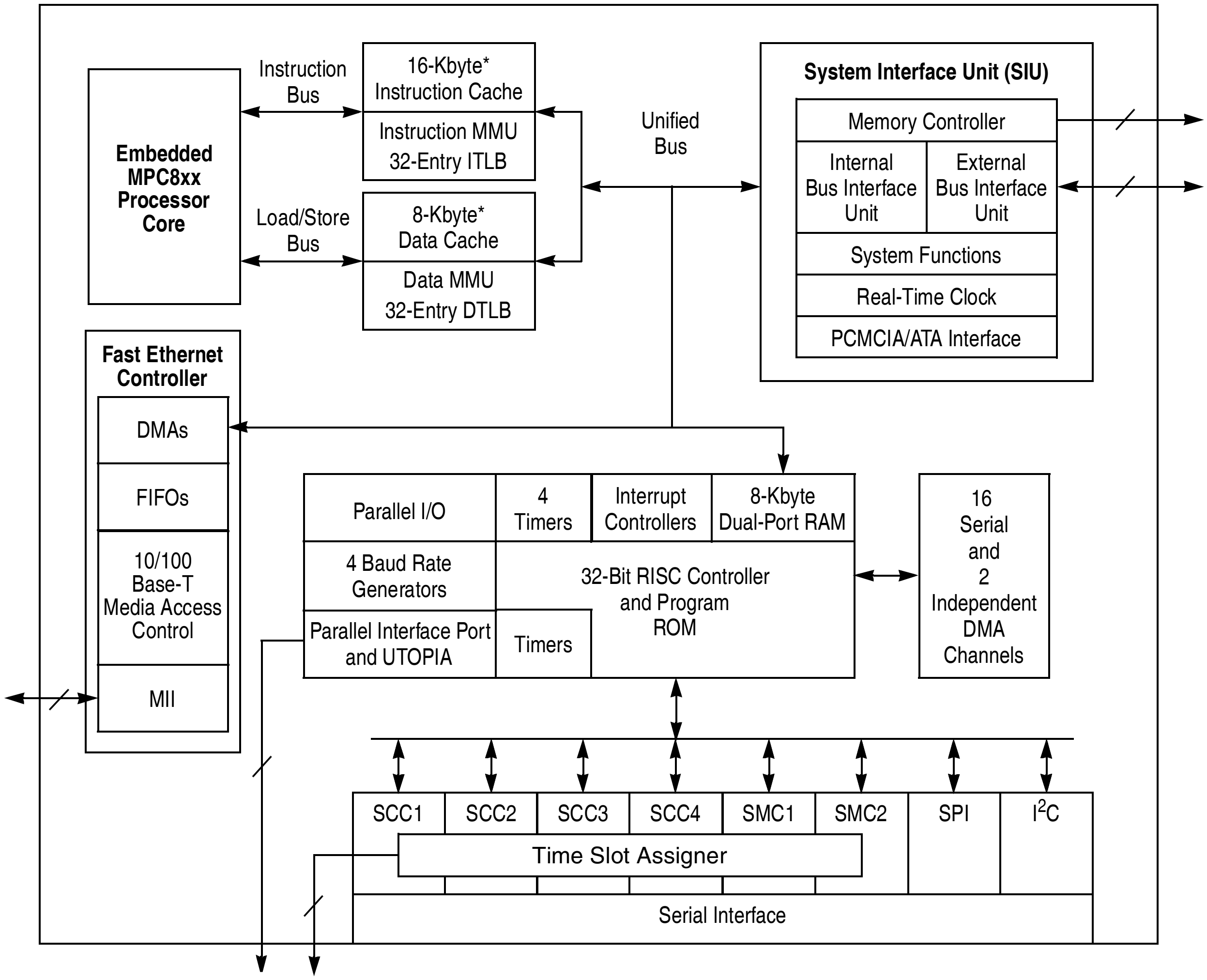
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 115°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc857dslcvr66b



*The MPC862T contains 4-Kbyte instruction cache and 4-Kbyte data cache.

Figure 1. MPC862P/862T Block Diagram

7.6 References

Semiconductor Equipment and Materials International (415) 964-5111
805 East Middlefield Rd.
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) Specifications 800-854-7179 or
(Available from Global Engineering Documents) 303-397-7956

JEDEC Specifications http://www.jedec.org

1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

8 Layout Practices

Each V_{CC} pin on the MPC862/857T/857DSL should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC862/857T/857DSL have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

9 Bus Signal Timing

The maximum bus speed supported by the MPC862/857T/857DSL is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC862/857T/857DSL used at 80MHz must be configured for a 40 MHz bus). Table 6 shows the period ranges for standard part frequencies.

Table 6. Period Range for Standard Part Frequencies

Freq	50 MHz		66 MHz		80 MHz		100 MHz	
	Min	Max	Min	Max	Min	Max	Min	Max
Period	20.00	30.30	15.15	30.30	25.00	30.30	20.00	30.30

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B37	UPWAIT valid to CLKOUT falling edge [12] (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid [12] (MIN = 0.00 x B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge [13] (MIN = 0.00 x B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge (MIN = 0.00 x B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 x B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

2 If the rate of change of the frequency of EXTAL is slow (I.e. it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (I.e., it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

3 The timings specified in B4 and B5 are based on full strength clock.

4 The timing for $\overline{BR}$ output is relevant when the MPC862/857T/857DSL is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC862/857T/857DSL is selected to work with internal bus arbiter.

5 For part speeds above 50MHz, use 9.80ns for B11a.

6 The timing required for $\overline{BR}$ input is relevant when the MPC862/857T/857DSL is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC862/857T/857DSL is selected to work with external bus arbiter.

7 For part speeds above 50MHz, use 2ns for B17.

8 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

9 For part speeds above 50MHz, use 2ns for B19.

10 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

11 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

12 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 19.

13 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 22.

Figure 6 provides the timing for the synchronous output signals.

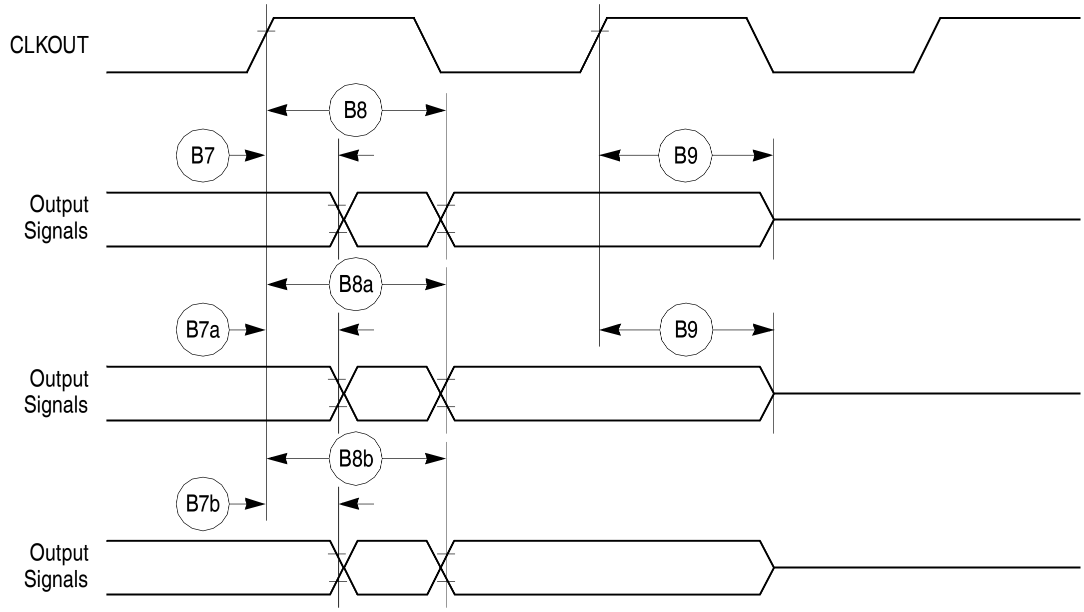


Figure 6. Synchronous Output Signals Timing

Figure 7 provides the timing for the synchronous active pull-up and open-drain output signals.

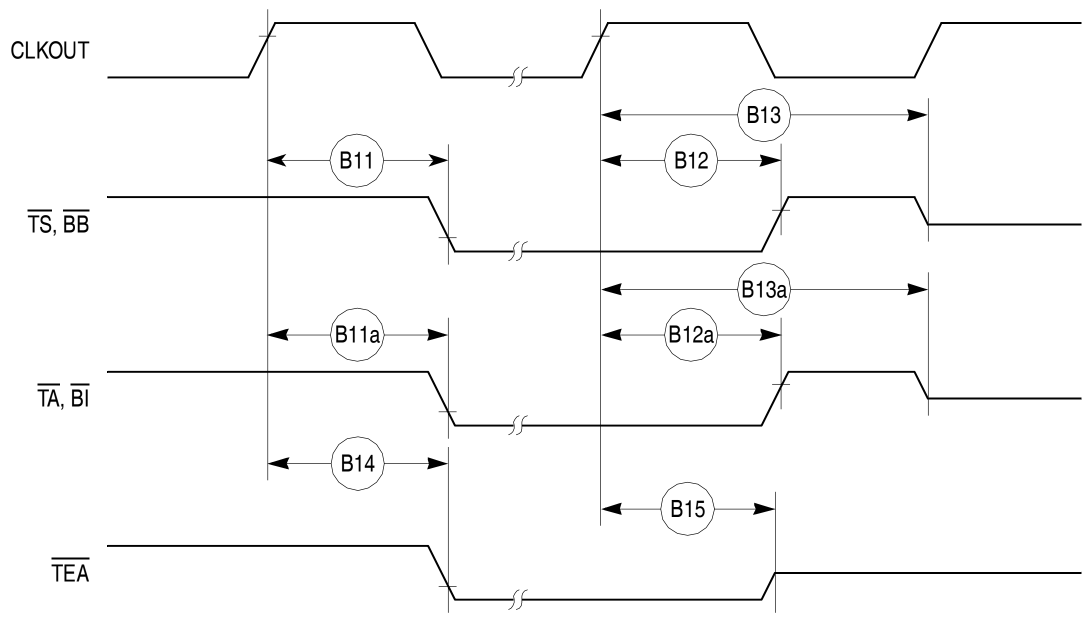


Figure 7. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

Figure 15 through Figure 17 provide the timing for the external bus write controlled by various GPCM factors.

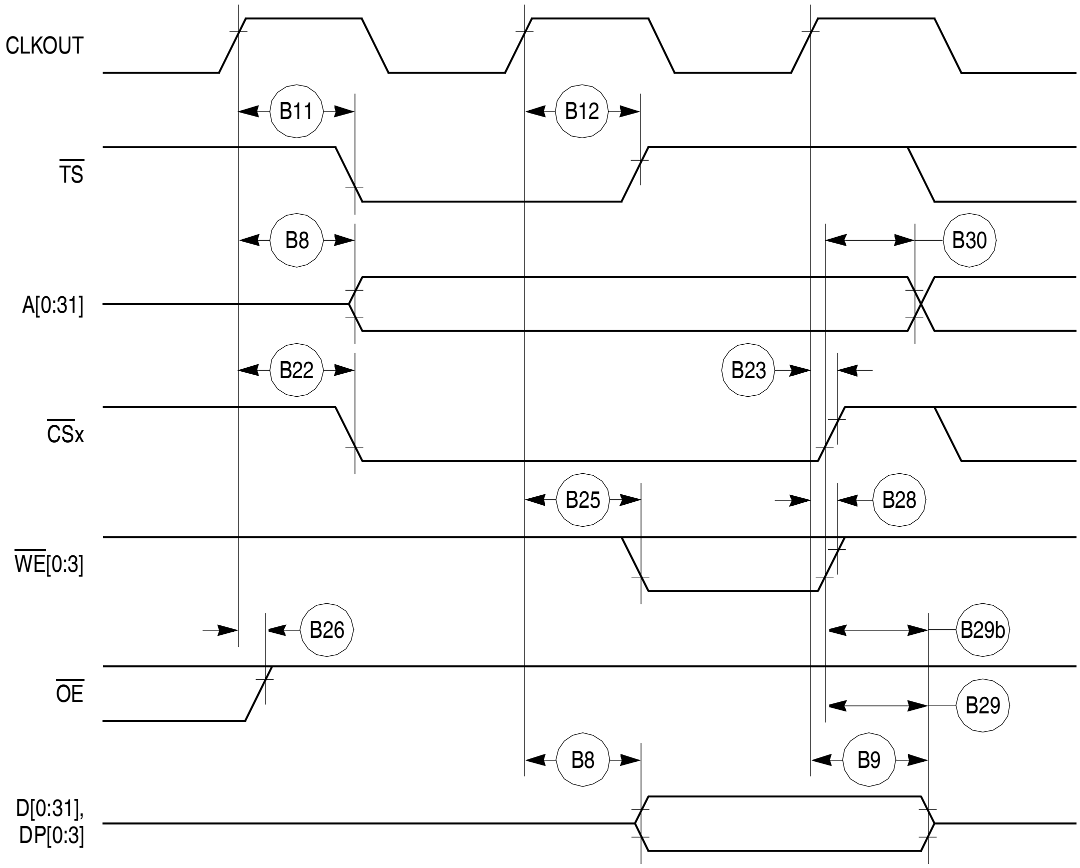


Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0,1 CSNT = 0)

Figure 18 provides the timing for the external bus controlled by the UPM.

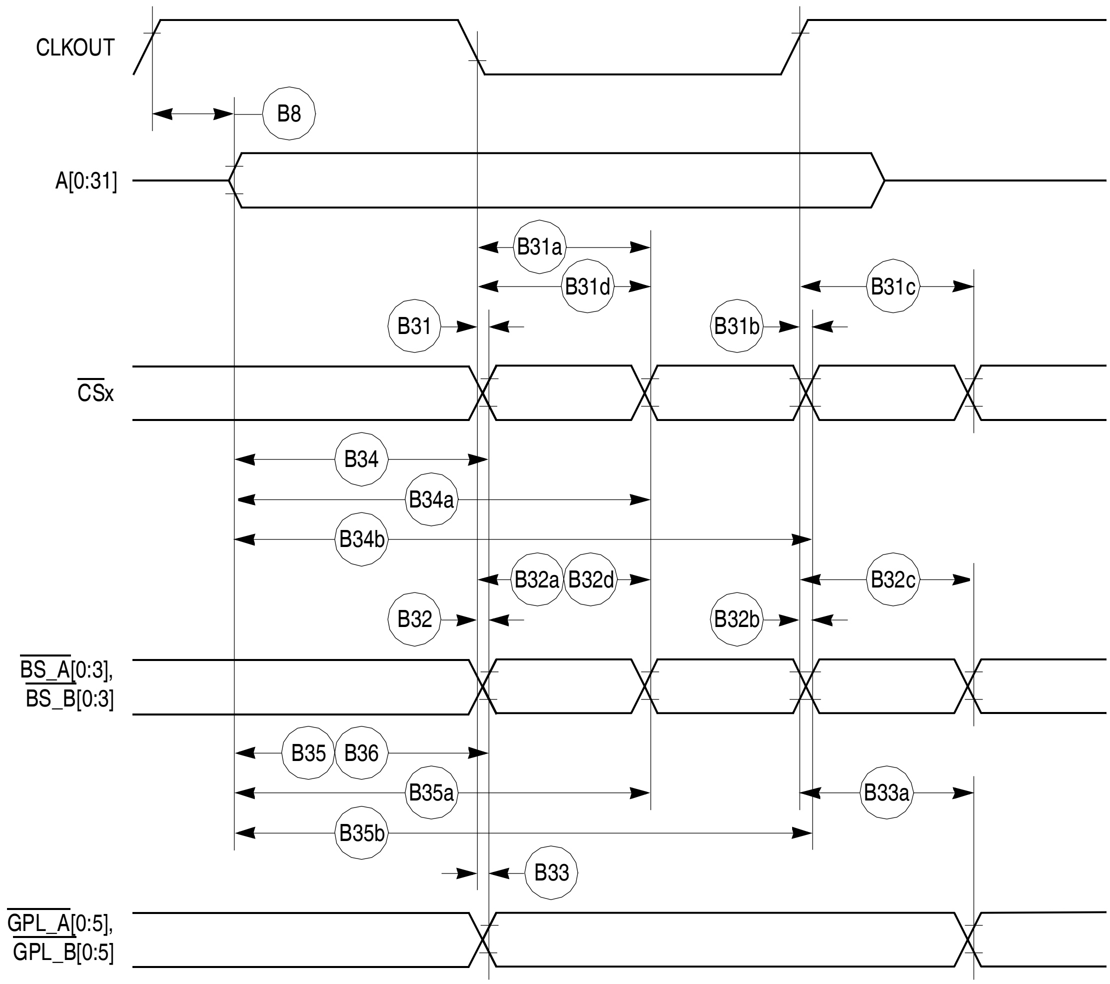


Figure 18. External Bus Timing (UPM Controlled Signals)

Figure 26 provides the PCMCIA access cycle timing for the external bus read.

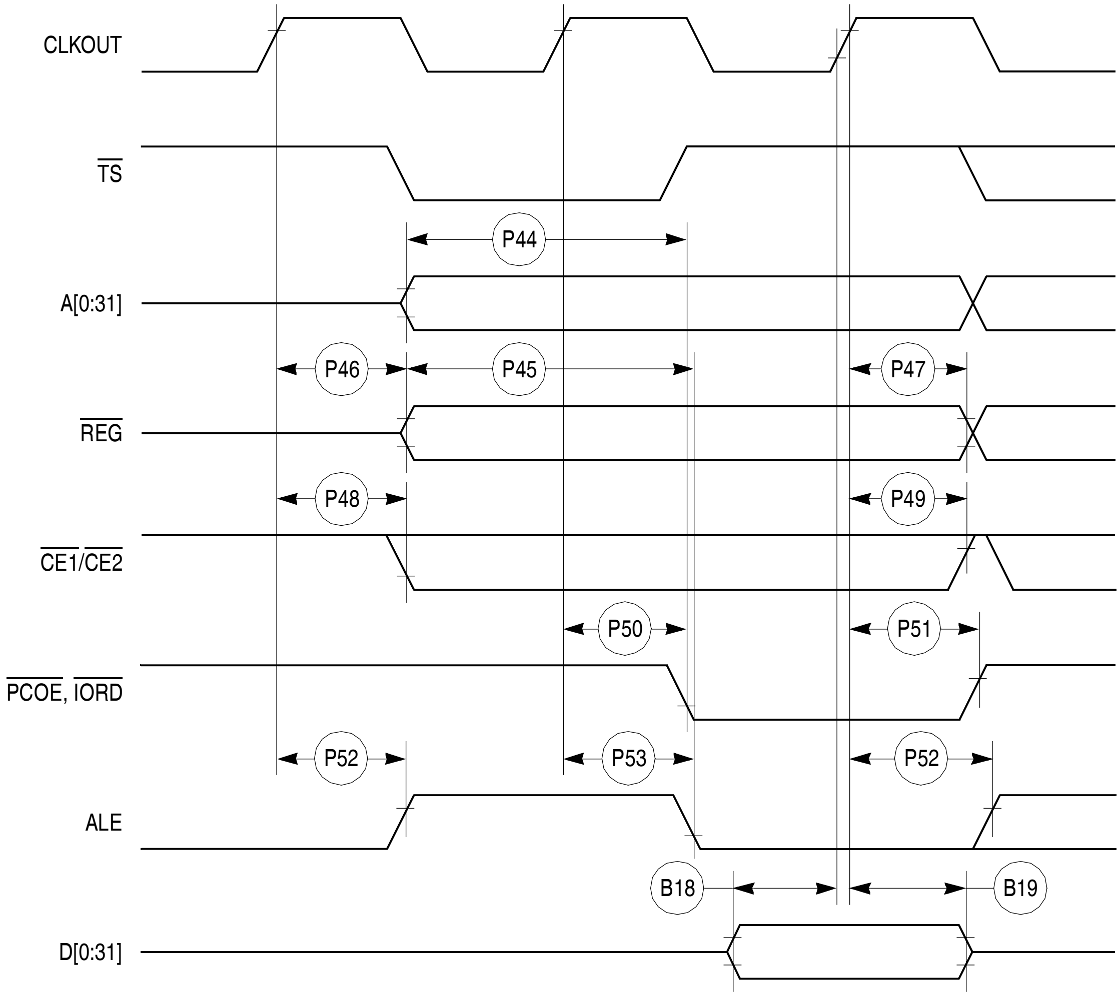


Figure 26. PCMCIA Access Cycles Timing External Bus Read

Table 10 shows the PCMCIA port timing for the MPC862/857T/857DSL.

Table 10. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx Valid (MAX = 0.00 x B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive [1] (MIN = 0.75 x B1 + 3.00)	25.70	—	21.70	—	18.00	—	14.40	—	ns
P59	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 x B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 x B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

[1] OP2 and OP3 only.

Figure 29 provides the PCMCIA output port timing for the MPC862/857T/857DSL.

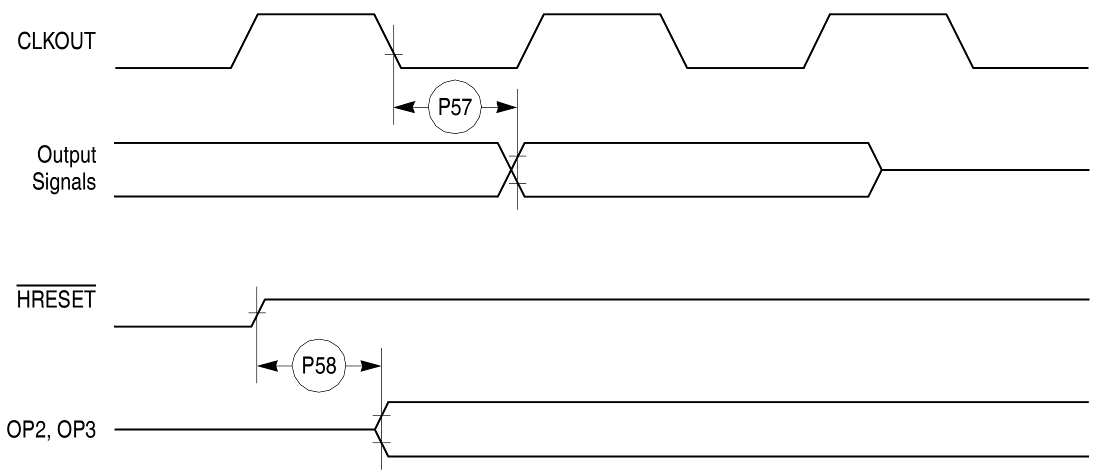


Figure 29. PCMCIA Output Port Timing

Figure 30 provides the PCMCIA output port timing for the MPC862/857T/857DSL.

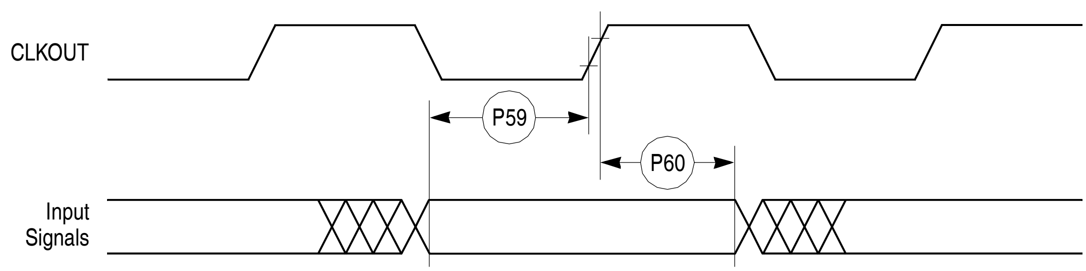


Figure 30. PCMCIA Input Port Timing

Table 12 shows the reset timing for the MPC862/857T/857DSL.

Table 12. Reset Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 x B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 x B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 x B1)	515.20	—	425.00	—	340.00	—	257.60	—	ns
R72	—	—	—	—	—	—	—	—	—	—
R73	Configuration data to HRESET rising edge set up time (MIN = 15.00 x B1 + 50.00)	504.50	—	425.00	—	350.00	—	277.30	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time (MIN = 0.00 x B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 x B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 x B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 x B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance. (MAX = 0.00 x B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance. (MAX = 0.00 x B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK set up (MIN = 3.00 x B1)	90.90	—	75.00	—	60.00	—	45.50	—	ns
R81	DSDI, DSCK hold time (MIN = 0.00 x B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 x B1)	242.40	—	200.00	—	160.00	—	121.20	—	ns

Table 16. IDMA Controller Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
43	SDACK negation delay from clock low	—	12	ns
44	SDACK negation delay from TA low	—	20	ns
45	SDACK negation delay from clock high	—	15	ns
46	TA assertion to falling edge of the clock setup time (applies to external TA)	7	—	ns

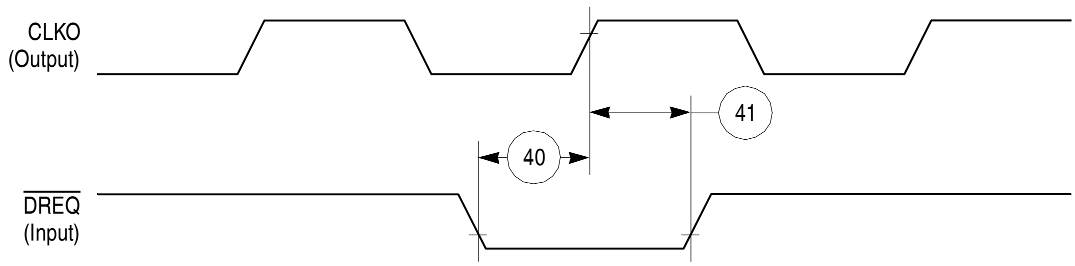


Figure 46. IDMA External Requests Timing Diagram

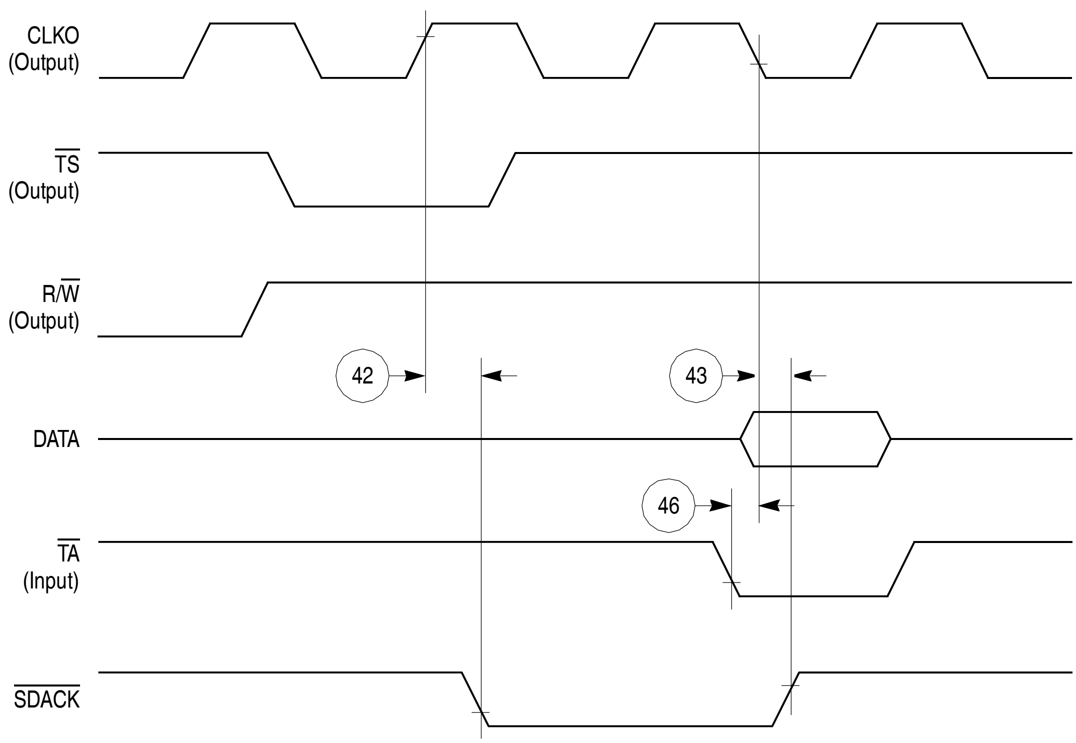


Figure 47. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA

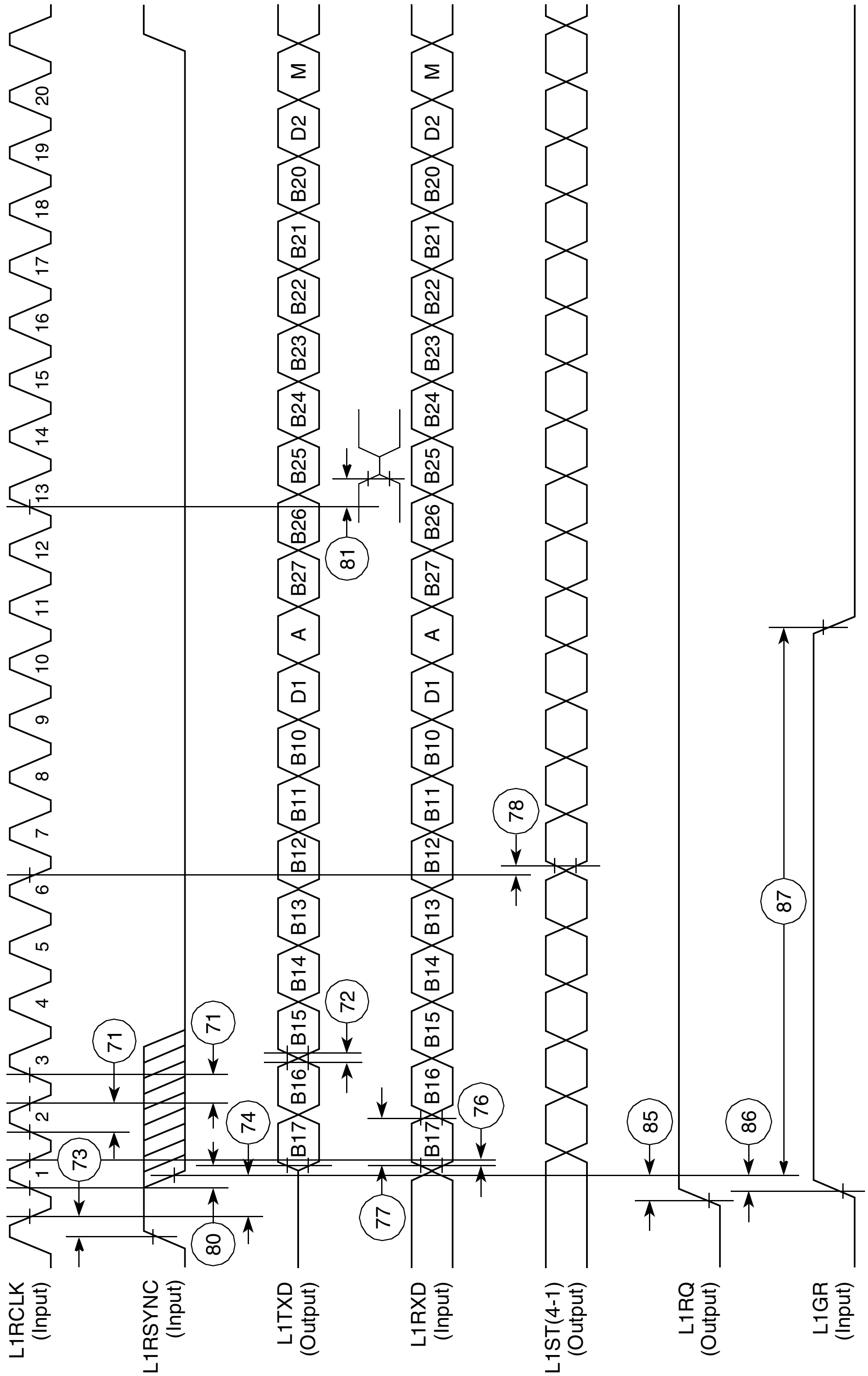


Figure 56. IDL Timing

11.7 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

Table 20. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 width high [1]	1/SYNCCLK	—	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK +5	—	ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	—	ns
107	RXD1 hold time from RCLK1 rising edge [2]	5.00	—	ns
108	$\overline{\text{CD1}}$ setup Time to RCLK1 rising edge	5.00	—	ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.

[2] Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 frequency [1]	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge [2]	0.00	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	40.00	—	ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 3/1.

[2] Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

Table 22. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns
135	$\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted [2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2/1.

[2] $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

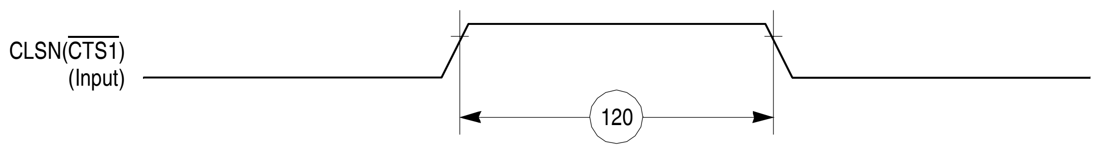


Figure 60. Ethernet Collision Timing Diagram

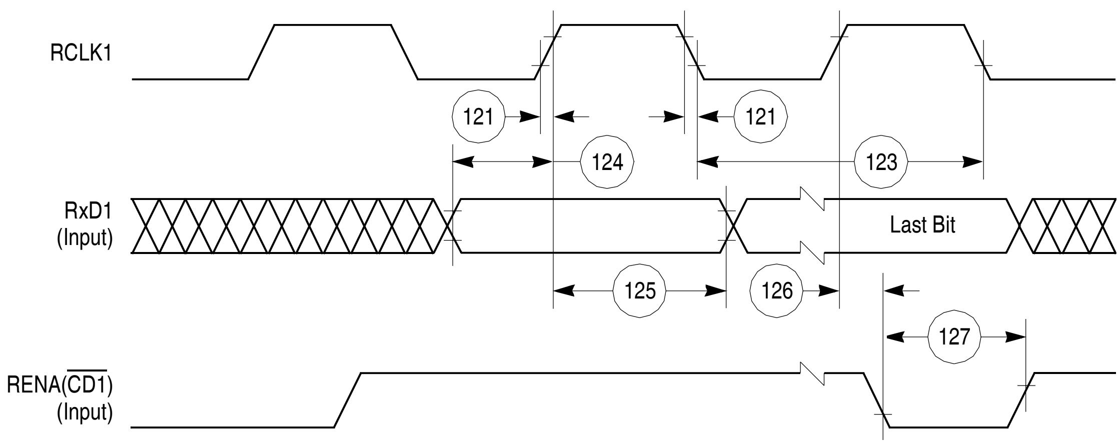


Figure 61. Ethernet Receive Timing Diagram

Table 35 contains a list of the MPC862 input and output signals and shows multiplexing and pin assignments.

Table 35. Pin Assignments

Name	Pin Number	Type
A[0:31]	B19, B18, A18, C16, B17, A17, B16, A16, D15, C15, B15, A15, C14, B14, A14, D12, C13, B13, D9, D11, C12, B12, B10, B11, C11, D10, C10, A13, A10, A12, A11, A9	Bidirectional Three-state
TSIZ0 $\overline{\text{REG}}$	B9	Bidirectional Three-state
TSIZ1	C9	Bidirectional Three-state
RD/$\overline{\text{WR}}$	B2	Bidirectional Three-state
$\overline{\text{BURST}}$	F1	Bidirectional Three-state
$\overline{\text{BDIP}}$ $\overline{\text{GPL\_B5}}$	D2	Output
$\overline{\text{TS}}$	F3	Bidirectional Active Pull-up
$\overline{\text{TA}}$	C2	Bidirectional Active Pull-up
$\overline{\text{TEA}}$	D1	Open-drain
$\overline{\text{BI}}$	E3	Bidirectional Active Pull-up
$\overline{\text{IRQ2}}$ $\overline{\text{RSV}}$	H3	Bidirectional Three-state
$\overline{\text{IRQ4}}$ $\overline{\text{KR}}$ $\overline{\text{RETRY}}$ SPKROUT	K1	Bidirectional Three-state
$\overline{\text{CR}}$ $\overline{\text{IRQ3}}$	F2	Input
D[0:31]	W14, W12, W11, W10, W13, W9, W7, W6, U13, T11, V11, U11, T13, V13, V10, T10, U10, T12, V9, U9, V8, U8, T9, U12, V7, T8, U7, V12, V6, W5, U6, T7	Bidirectional Three-state
DP0 $\overline{\text{IRQ3}}$	V3	Bidirectional Three-state
DP1 $\overline{\text{IRQ4}}$	V5	Bidirectional Three-state
DP2 $\overline{\text{IRQ5}}$	W4	Bidirectional Three-state
DP3 $\overline{\text{IRQ6}}$	V4	Bidirectional Three-state

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
PA2 CLK6 TOUT3 L1RCLKB	R18	Bidirectional
PA1 CLK7 BRGO4 TIN4	T19	Bidirectional
PA0 CLK8 TOUT4 L1TCLKB	U19	Bidirectional
PB31 SPISEL REJECT1	C17	Bidirectional (Optional: Open-drain)
PB30 SPICLK RSTRT2	C19	Bidirectional (Optional: Open-drain)
PB29 SPIMOSI	E16	Bidirectional (Optional: Open-drain)
PB28 SPIMISO BRGO4	D19	Bidirectional (Optional: Open-drain)
PB27 I2CSDA BRGO1	E19	Bidirectional (Optional: Open-drain)
PB26 I2CSCL BRGO2	F19	Bidirectional (Optional: Open-drain)
PB25 RXADDR3[2] SMTXD1	J16	Bidirectional (Optional: Open-drain)
PB24 TXADDR3[2] SMRXD1	J18	Bidirectional (Optional: Open-drain)
PB23 TXADDR2[2] SDACK1 SMSYN1	K17	Bidirectional (Optional: Open-drain)
PB22 TXADDR4[2] SDACK2 SMSYN2	L19	Bidirectional (Optional: Open-drain)

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
PB21 SMTXD2 L1CLKOB PHSEL1 [1] TXADDR1 [2]	K16	Bidirectional (Optional: Open-drain)
PB20 SMRXD2 L1CLKOA PHSEL0[1] TXADDR0[2]	L16	Bidirectional (Optional: Open-drain)
PB19 $\overline{RTS1}$ L1ST1	N19	Bidirectional (Optional: Open-drain)
PB18 RXADDR4[2] $\overline{RTS2}$ L1ST2	N17	Bidirectional (Optional: Open-drain)
PB17 $\overline{L1RQb}$ L1ST3 $\overline{RTS3}$ PHREQ1[1] RXADDR1[2]	P18	Bidirectional (Optional: Open-drain)
PB16 $\overline{L1RQa}$ L1ST4 $\overline{RTS4}$ PHREQ0[1] RXADDR0[2]	N16	Bidirectional (Optional: Open-drain)
PB15 BRGO3 TxClav	R17	Bidirectional
PB14 RXADDR2[2] $\overline{RSTRT1}$	U18	Bidirectional
PC15 $\overline{DREQ0}$ $\overline{RTS1}$ L1ST1 RxClav	D16	Bidirectional
PC14 $\overline{DREQ1}$ $\overline{RTS2}$ L1ST2	D18	Bidirectional

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
PC13 L1RQb L1ST3 RTS3	E18	Bidirectional
PC12 L1RQa L1ST4 RTS4	F18	Bidirectional
PC11 CTS1	J19	Bidirectional
PC10 CD1 TGATE1	K19	Bidirectional
PC9 CTS2	L18	Bidirectional
PC8 CD2 TGATE2	M18	Bidirectional
PC7 CTS3 L1TSYNCB SDACK2	M16	Bidirectional
PC6 CD3 L1RSYNCB	R19	Bidirectional
PC5 CTS4 L1TSYNCA SDACK1	T18	Bidirectional
PC4 CD4 L1RSYNCA	T17	Bidirectional
PD15 L1TSYNCA MII-RXD3 UTPB0	U17	Bidirectional
PD14 L1RSYNCA MII-RXD2 UTPB1	V19	Bidirectional
PD13 L1TSYNCB MII-RXD1 UTPB2	V18	Bidirectional

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
PD12 L1RSYNCB MII-MDC UTPB3	R16	Bidirectional
PD11 RXD3 MII-TXERR RXENB	T16	Bidirectional
PD10 TXD3 MII-RXD0 TXENB	W18	Bidirectional
PD9 RXD4 MII-TXD0 UTPCLK	V17	Bidirectional
PD8 TXD4 MII-MDC MII-RXCLK	W17	Bidirectional
PD7 RTS3 MII-RXERR UTPB4	T15	Bidirectional
PD6 RTS4 MII-RXDV UTPB5	V16	Bidirectional
PD5 REJECT2 MII-TXD3 UTPB6	U15	Bidirectional
PD4 REJECT3 MII-TXD2 UTPB7	U16	Bidirectional
PD3 REJECT4 MII-TXD1 SOC	W16	Bidirectional
TMS	G18	Input
TDI DSDI	H17	Input
TCK DSCK	H16	Input

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
TRST	G19	Input
TDO DSDO	G17	Output
M_CRS	B7	Input
M_MDIO	H18	Bidirectional
M_TXEN	V15	Output
M_COL	H4	Input
KAPWR	R1	Power
GND	F6, F7, F8, F9, F10, F11, F12, F13, F14, G6, G7, G8, G9, G10, G11, G12, G13, G14, H6, H7, H8, H9, H10, H11, H12, H13, H14, J6, J7, J8, J9, J10, J11, J12, J13, J14, K6, K7, K8, K9, K10, K11, K12, K13, K14, L6, L7, L8, L9, L10, L11, L12, L13, L14, M6, M7, M8, M9, M10, M11, M12, M13, M14, N6, N7, N8, N9, N10, N11, N12, N13, N14, P6, P7, P8, P9, P10, P11, P12, P13, P14	Power
VDDL	A8, M1, W8, H19, F4, F16, P4, P16	Power
VDDH	E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P5, P15, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, T14	Power
N/C	D6, D13, D14, U2, V2	No-connect

[1] Classic SAR mode only

[2] ESAR mode only

14.2 Mechanical Dimensions of the PBGA Package

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to *Plastic Ball Grid Array Application Note* (order number: AN1231/D) available from your local Freescale sales office. Figure 78 shows the mechanical dimensions of the PBGA package.

15 Document Revision History

Table 36 lists significant changes between revisions of this document.

Table 36. Document Revision History

Rev. No.	Date	Substantive Changes
0	2001	Initial revision
0.1	9/2001	Change extended temperature from 95 to 105
0.2	11/2001	Revised for new template, changed Table 7 B23 max value @ 66 MHz from 2 ns to 8 ns.
0.3	4/2002	• Timing modified and equations added, for Rev. A and B devices. • Modified power numbers and temperature ranges. Added ESAR UTOPIA timing.
1.0	9/2002	• Specification changed to include the MPC857T and MPC857DSL. • Changed maximum operating frequency from 80 MHz to 100 MHz. • Removed MPC862DP, DT, and SR derivatives and part numbers. • Corrected power dissipation numbers. • Changed UTOPIA maximum frequency from 50 MHz to 33 MHz. • Changed part number ordering information to Rev. B devices only. • To maximum ratings for temperature, added frequency ranges.
1.1	5/2003	Changed SPI Master Timing Specs. 162 and 164
1.2	8/2003	• Changed B28a through B28d and B29b to show that TRLX can be 0 or 1. • Non-technical reformatting
2.0	11/2004	• Added a table footnote to Table 5 DC Electrical Specifications about meeting the VIL Max of the I2C Standard. • Updated document template.
3.0	2/2006	• Changed Tj from 95C to 105C in table 34