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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 115°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc857dslczq66b

1 Overview

The MPC862/857T/857DSL is a derivative of Freescale's MPC860 PowerQUICC™ family of devices. It is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC862/857T/857DSL provides enhanced ATM functionality over that of other ATM-enabled members of the MPC860 family.

Table 1 shows the functionality supported by the members of the MPC862/857T/857DSL family.

Table 1. MPC862 Family Functionality

Part	Cache		Ethernet		SCC	SMC
	Instruction Cache	Data Cache	10T	10/100		
MPC862P	16 Kbyte	8 Kbyte	Up to 4	1	4	2
MPC862T	4 Kbyte	4 Kbyte	Up to 4	1	4	2
MPC857T	4 Kbyte	4 Kbyte	1	1	1	2
MPC857DSL	4 Kbyte	4 Kbyte	1	1	1 [1]	1 [2]

[1] On the MPC857DSL, the SCC (SCC1) is for ethernet only. Also, the MPC857DSL does not support the Time Slot Assigner (TSA).

[2] On the MPC857DSL, the SMC (SMC1) is for UART only.

2 Features

The following list summarizes the key MPC862/857T/857DSL features:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch, without conditional execution
  - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1).
    - 16-Kbyte instruction cache (MPC862P) is four-way, set-associative with 256 sets; 4-Kbyte instruction cache (MPC862T, MPC857T, and MPC857DSL) is two-way, set-associative with 128 sets.
    - 8-Kbyte data cache (MPC862P) is two-way, set-associative with 256 sets; 4-Kbyte data cache (MPC862T, MPC857T, and MPC857DSL) is two-way, set-associative with 128 sets.
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully associative instruction and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip-emulation debug mode

Table 2. Maximum Tolerated Ratings (continued)

(GND = 0 V)

Rating	Symbol	Value	Unit	Max Freq (MHz)
Input voltage [2]	V_{in}	GND-0.3 to VDDH	V	-
Temperature [3] (standard) [4]	$T_{A(min)}$	0	°C	100
	$T_{j(max)}$	105	°C	100
Temperature [3] (extended)	$T_{A(min)}$	-40	°C	80
	$T_{j(max)}$	115	°C	80
Storage temperature range	T_{stg}	-55 to +150	°C	-

1 The power supply of the device must start its ramp from 0.0 V.

2 Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC862/857T/857DSL is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

3 Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j.

4 JTAG is tested only at ambient, not at standard maximum or extended maximum.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature; see Figure 3.

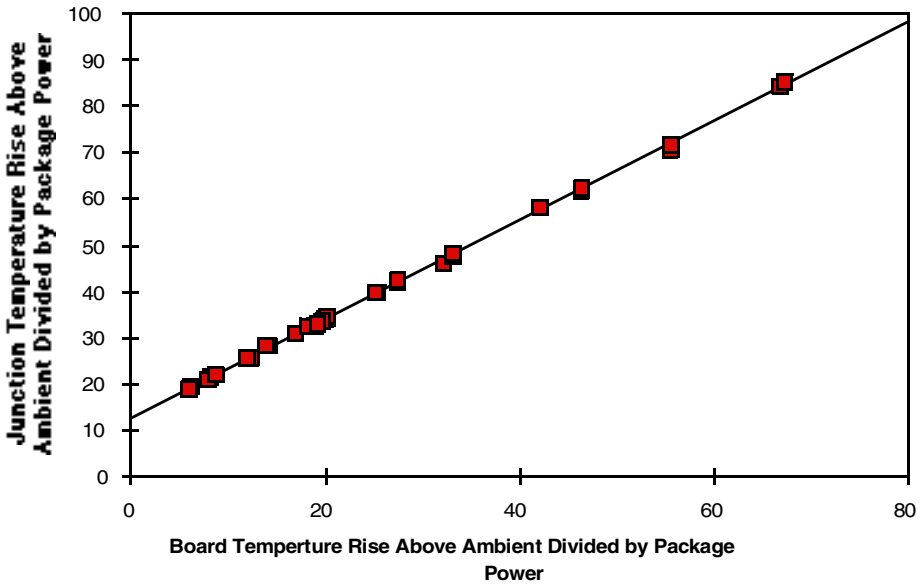


Figure 3. Effect of Board Temperature Rise on Thermal Behavior

Figure 6 provides the timing for the synchronous output signals.

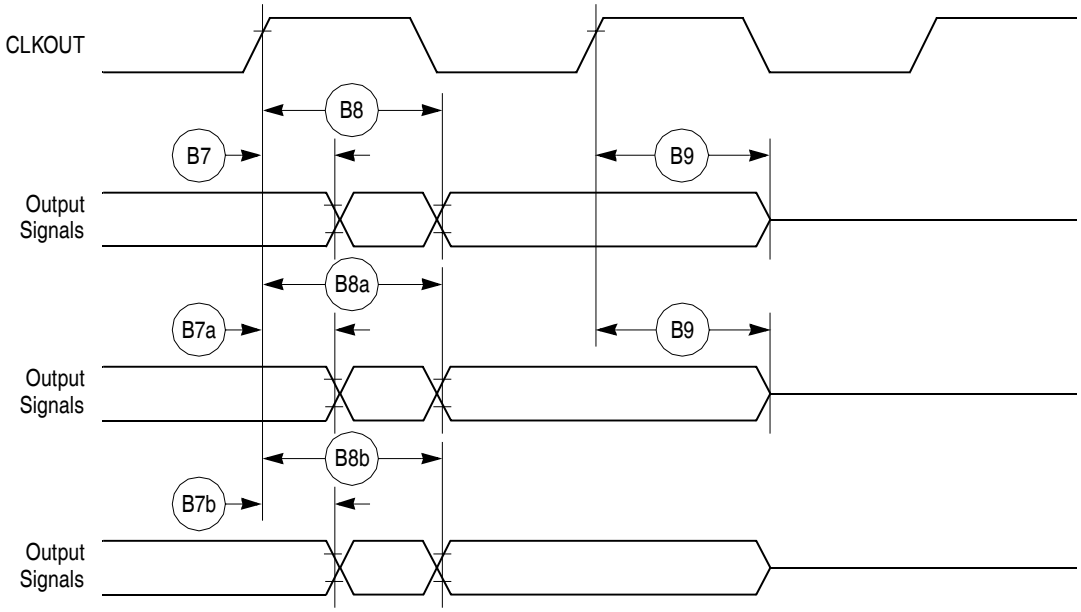


Figure 6. Synchronous Output Signals Timing

Figure 7 provides the timing for the synchronous active pull-up and open-drain output signals.

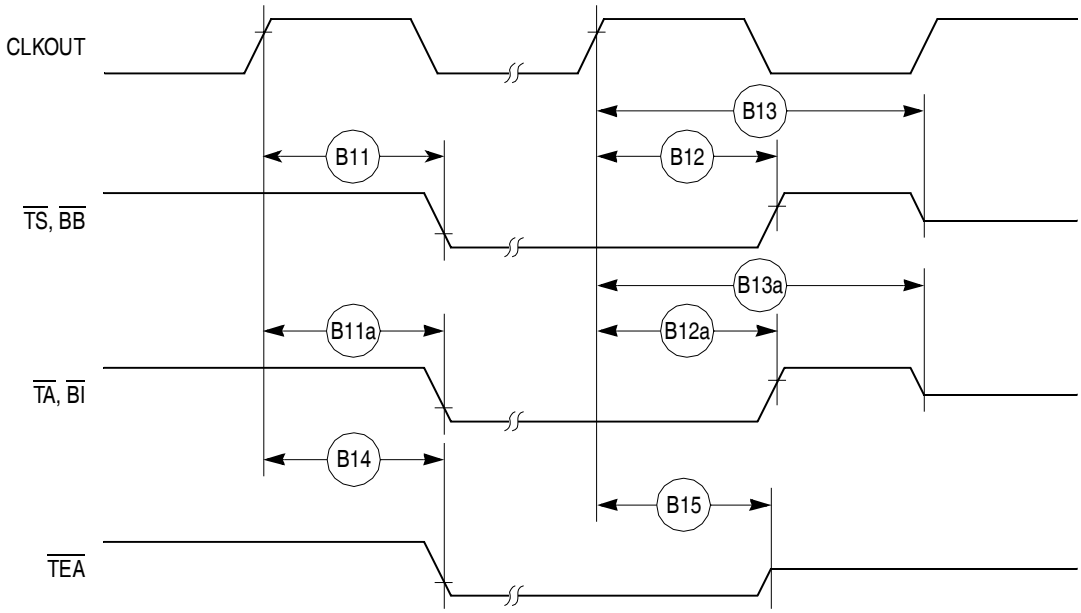


Figure 7. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

Figure 15 through Figure 17 provide the timing for the external bus write controlled by various GPCM factors.

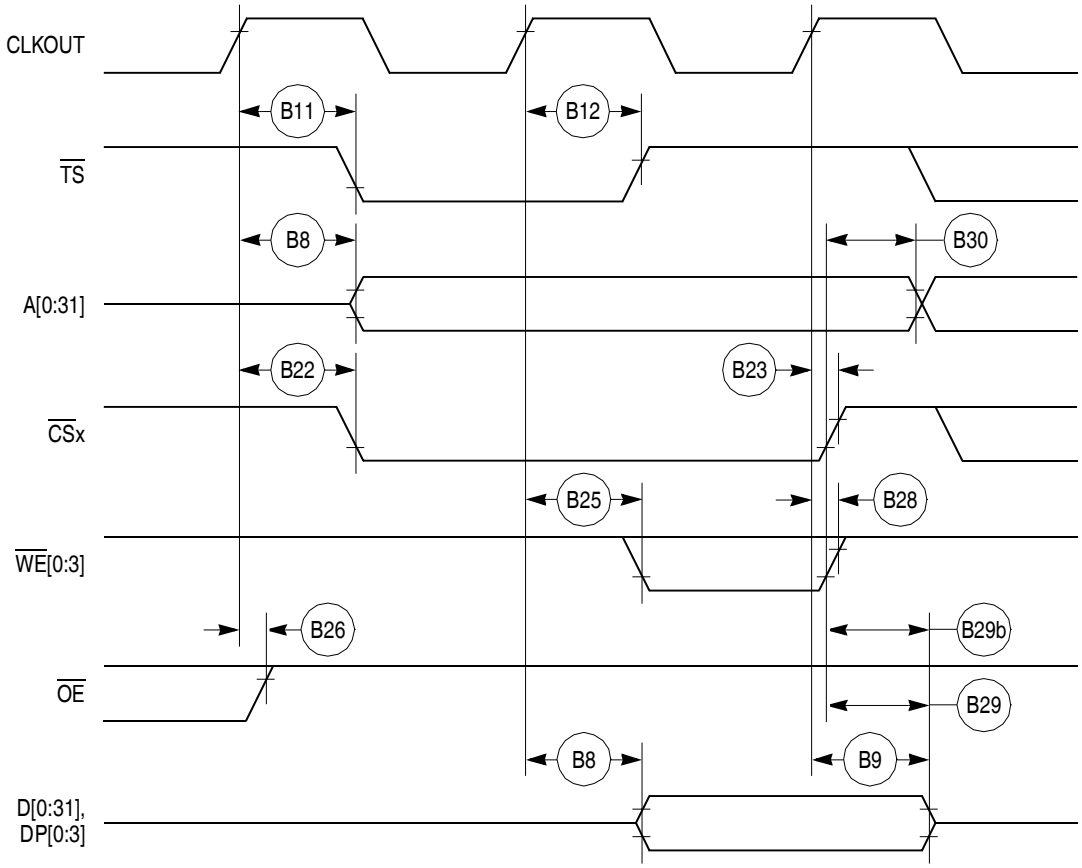


Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0,1 CSNT = 0)

Figure 18 provides the timing for the external bus controlled by the UPM.

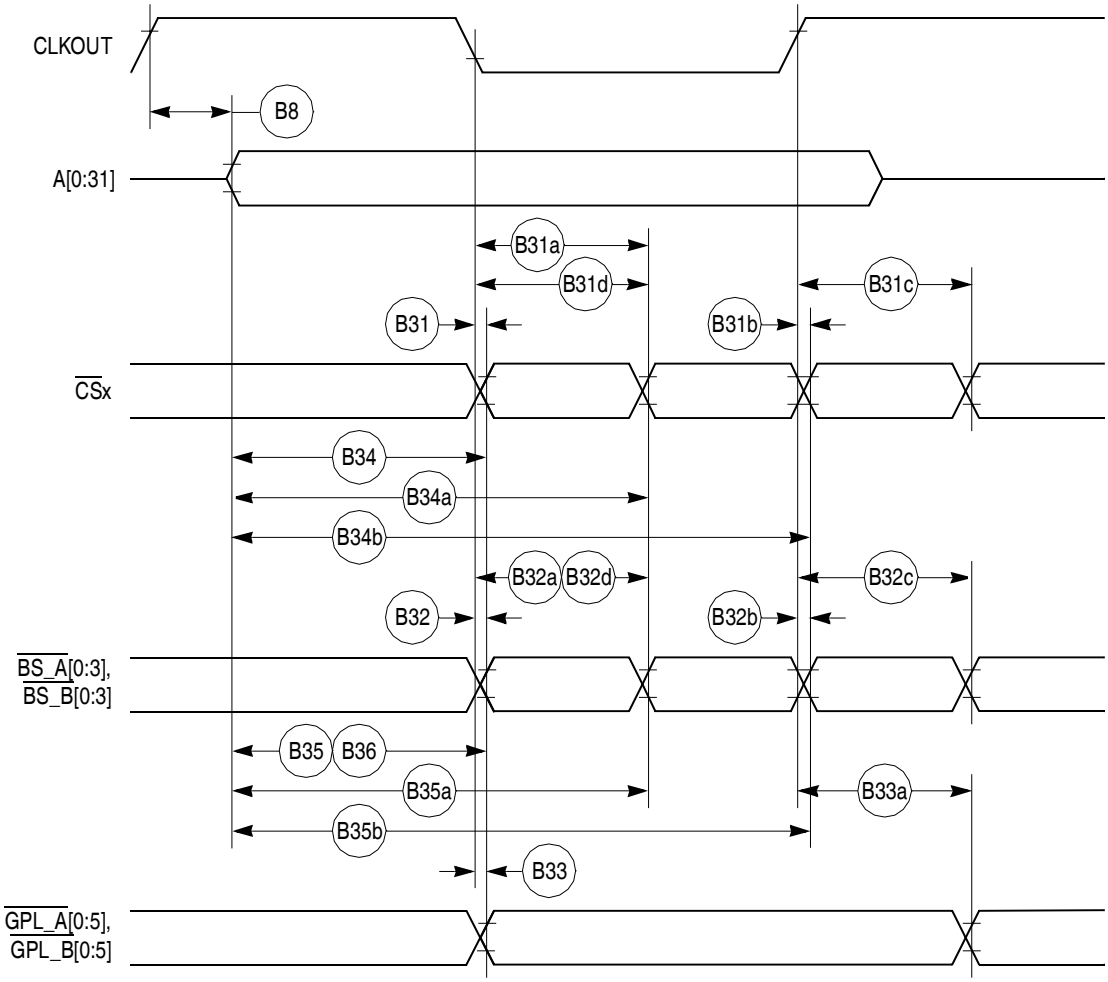


Figure 18. External Bus Timing (UPM Controlled Signals)

Table 8 provides interrupt timing for the MPC862/857T/857DSL.

Table 8. Interrupt Timing

Num	Characteristic [1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{IRQ}$x valid to CLKOUT rising edge (set up time)	6.00		ns
I40	$\overline{IRQ}$x hold time after CLKOUT	2.00		ns
I41	$\overline{IRQ}$x pulse width low	3.00		ns
I42	$\overline{IRQ}$x pulse width high	3.00		ns
I43	$\overline{IRQ}$x edge-to-edge time	$4xT_{CLOCKOUT}$		—

1 The timings I39 and I40 describe the testing conditions under which the $\overline{IRQ}$ lines are tested when being defined as level sensitive. The $\overline{IRQ}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{IRQ}$ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC862/857T/857DSL is able to support.

Figure 24 provides the interrupt detection timing for the external level-sensitive lines.

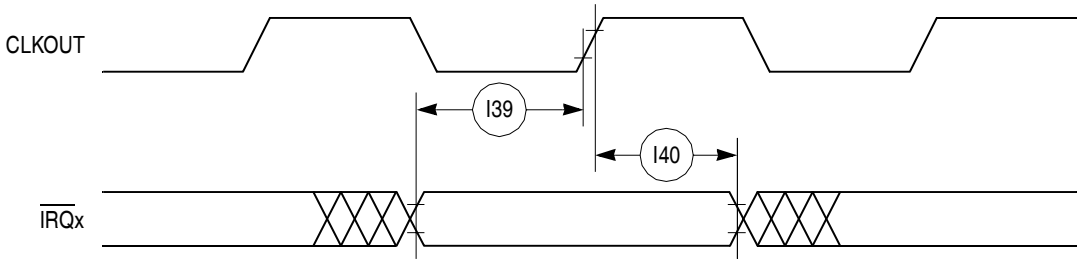


Figure 24. Interrupt Detection Timing for External Level Sensitive Lines

Figure 25 provides the interrupt detection timing for the external edge-sensitive lines.

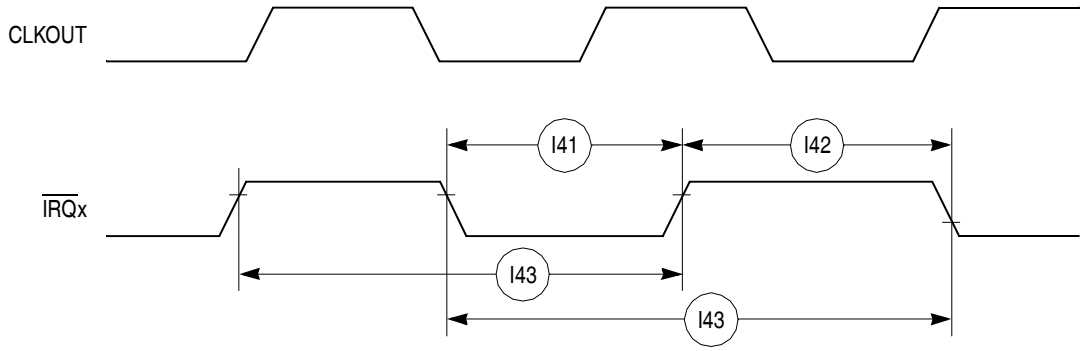


Figure 25. Interrupt Detection Timing for External Edge Sensitive Lines

Figure 35 provides the reset timing for the debug port configuration.

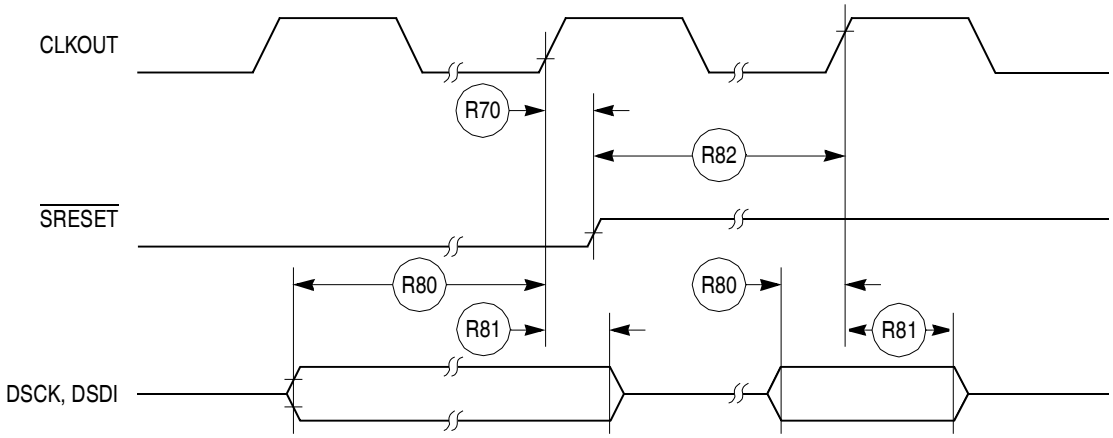


Figure 35. Reset Timing—Debug Port Configuration

10 IEEE 1149.1 Electrical Specifications

Table 13 provides the JTAG timings for the MPC862/857T/857DSL shown in Figure 36 though Figure 39.

Table 13. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

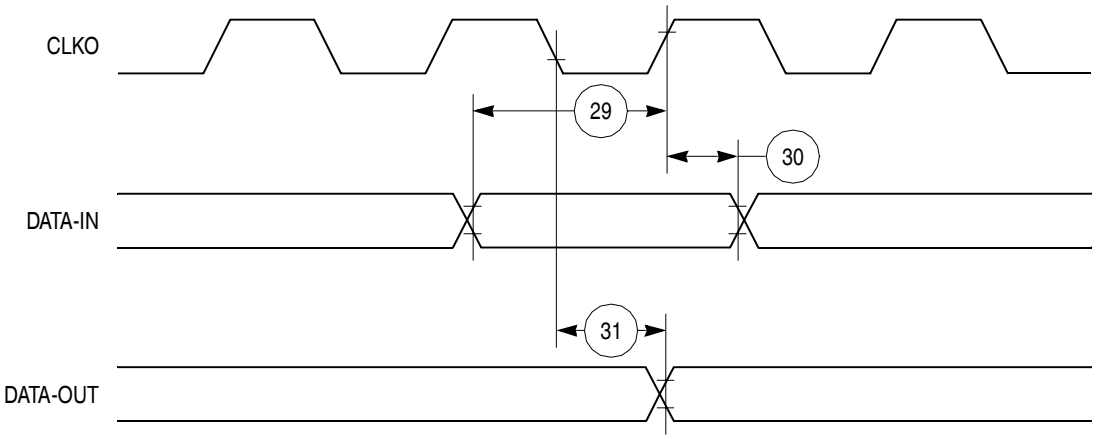


Figure 44. Parallel I/O Data-In/Data-Out Timing Diagram

11.2 Port C Interrupt AC Electrical Specifications

Table 15 provides the timings for port C interrupts.

Table 15. Port C Interrupt Timing

Num	Characteristic	33.34 MHz		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

Figure 45 shows the port C interrupt detection timing.

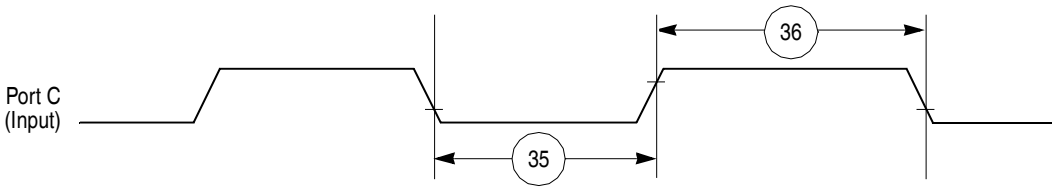


Figure 45. Port C Interrupt Detection Timing

11.3 IDMA Controller AC Electrical Specifications

Table 16 provides the IDMA controller timings as shown in Figure 46 though Figure 49.

Table 16. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high	3	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns

Table 16. IDMA Controller Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

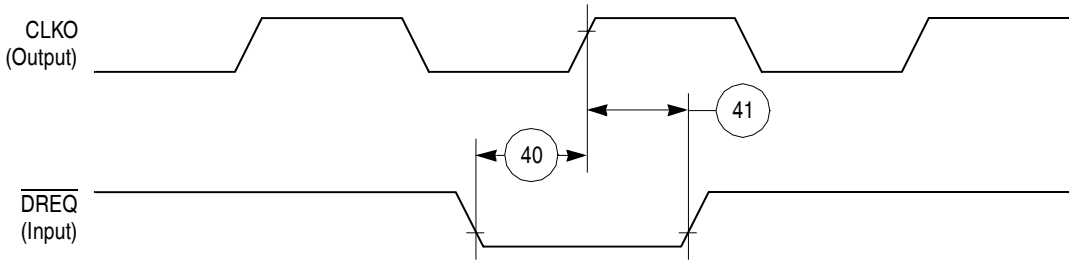


Figure 46. IDMA External Requests Timing Diagram

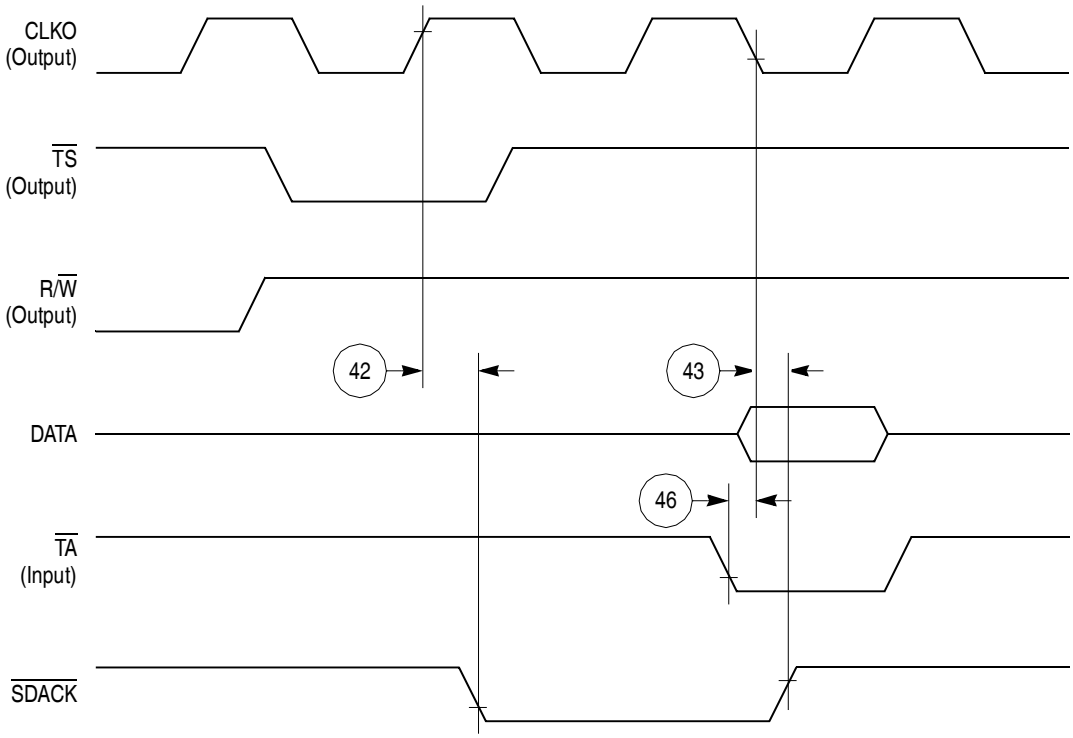


Figure 47. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Externally-Generated $\overline{\text{TA}}$

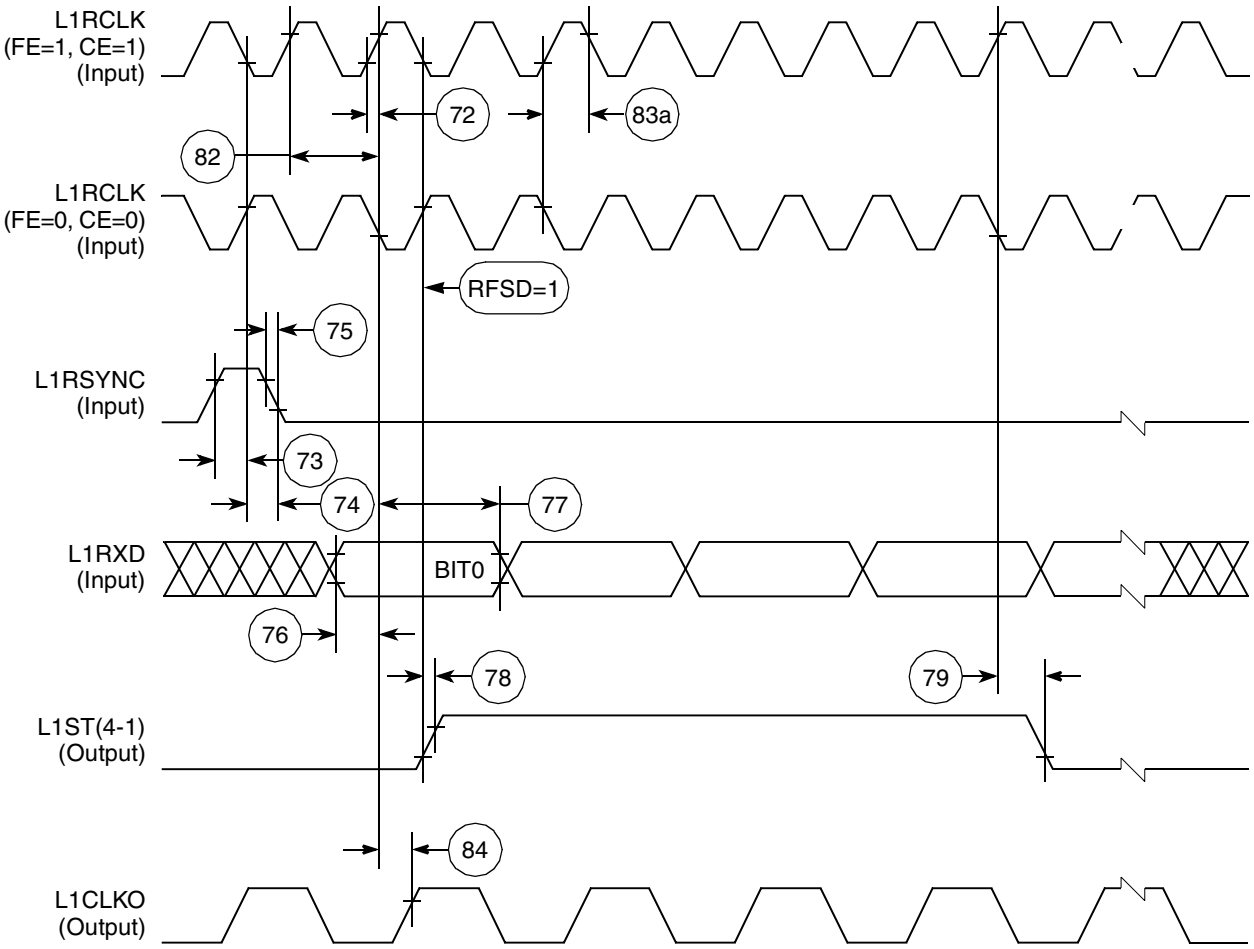


Figure 53. SI Receive Timing with Double-Speed Clocking (DSC = 1)

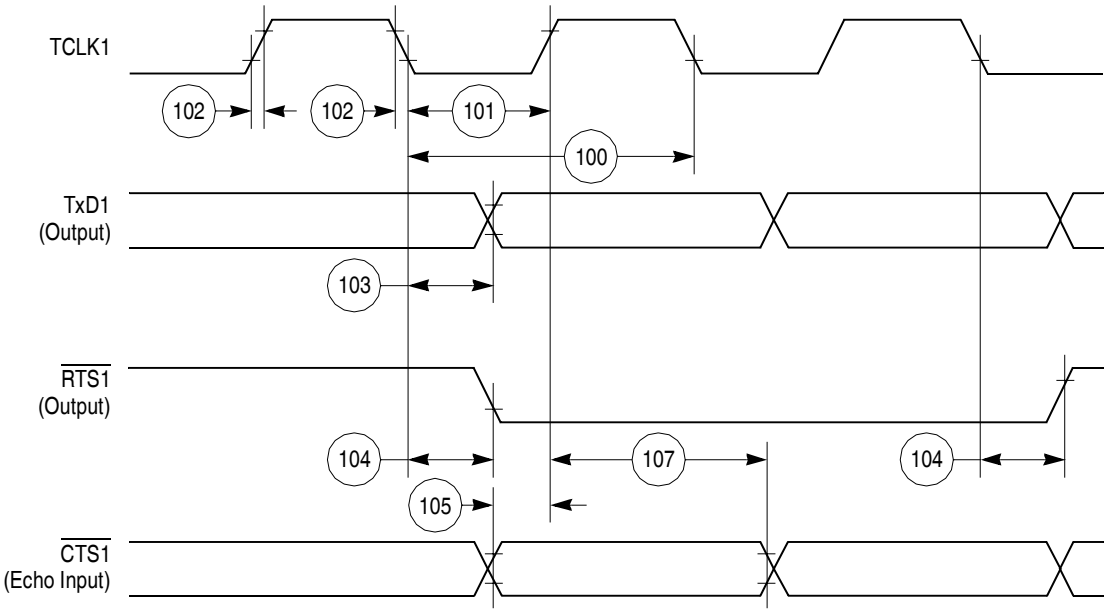


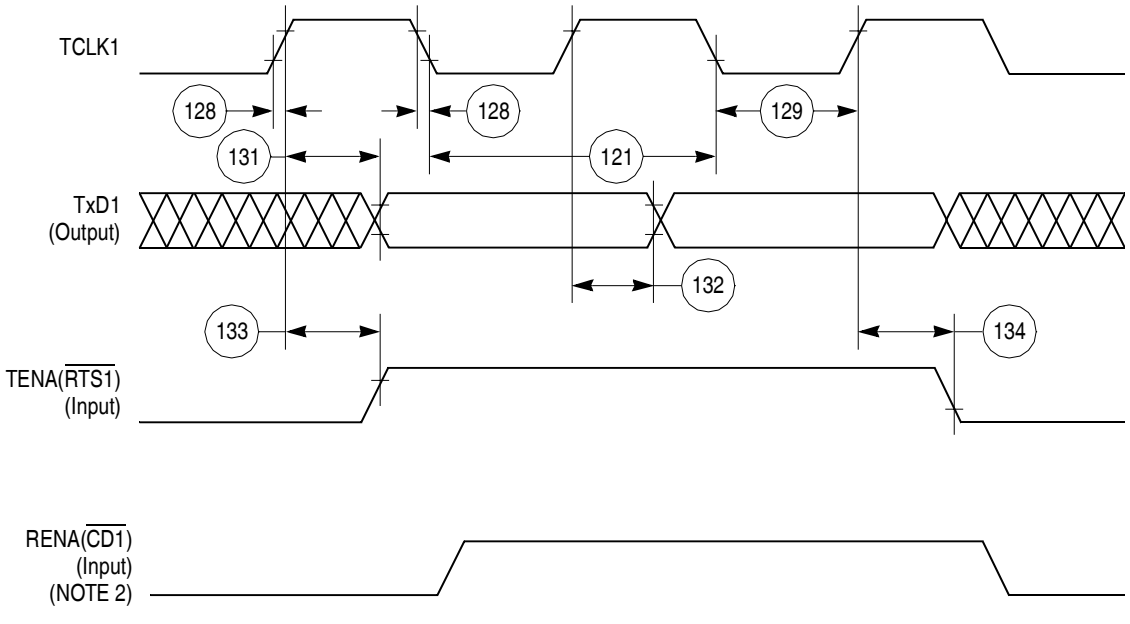
Figure 59. HDLC Bus Timing Diagram

11.8 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 60 though Figure 64.

Table 22. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period [1]	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period[1]	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	10	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	10	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns



NOTES:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 62. Ethernet Transmit Timing Diagram

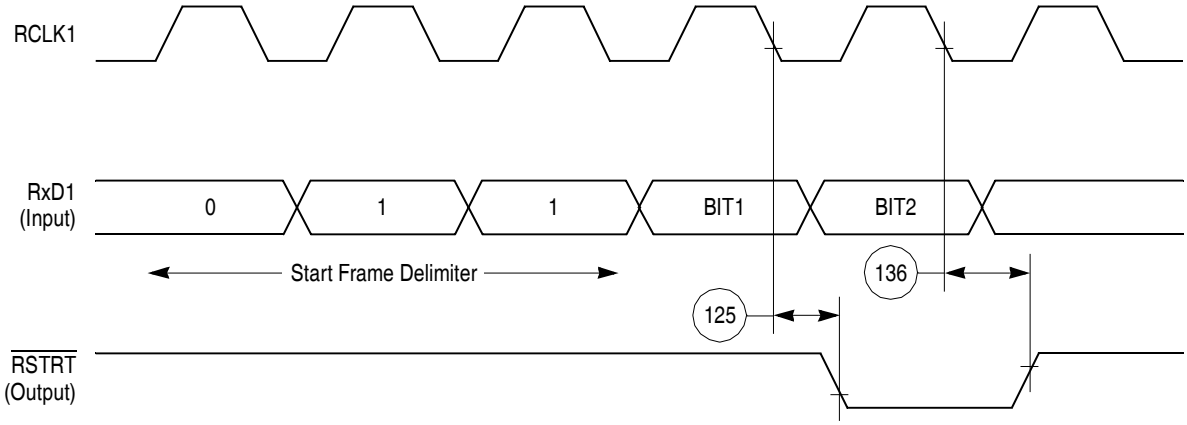


Figure 63. CAM Interface Receive Start Timing Diagram

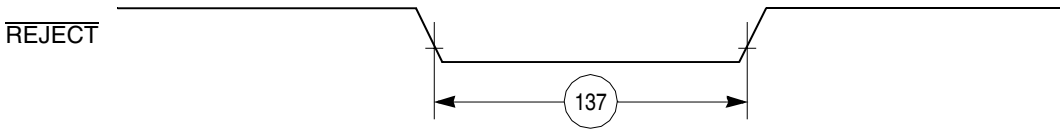


Figure 64. CAM Interface REJECT Timing Diagram

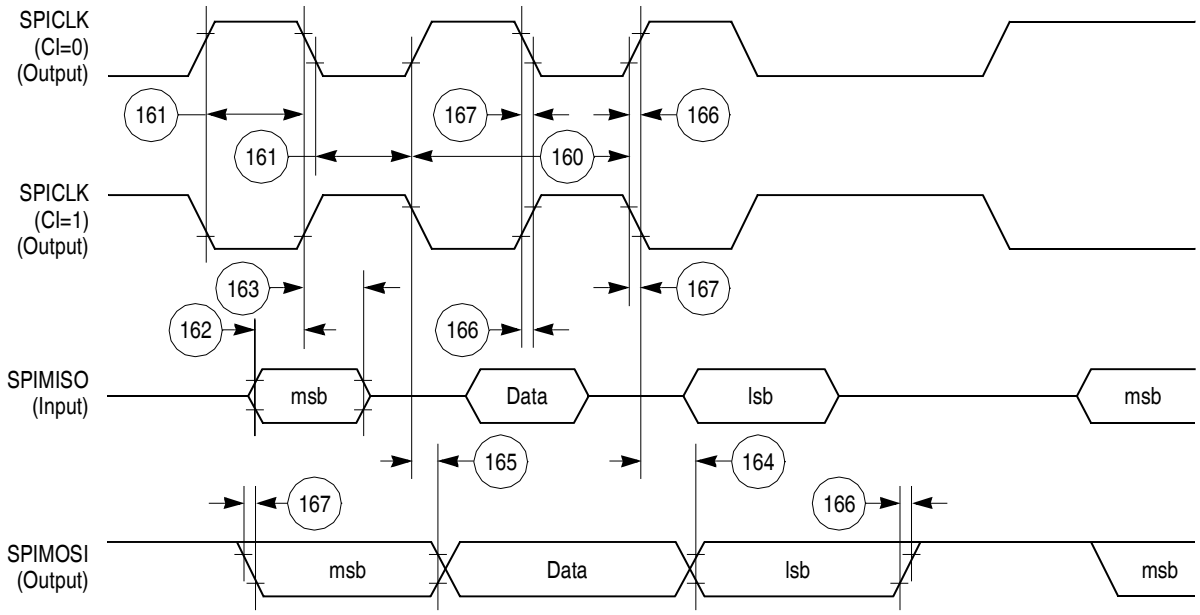


Figure 67. SPI Master (CP = 1) Timing Diagram

11.11 SPI Slave AC Electrical Specifications

Table 25 provides the SPI slave timings as shown in Figure 68 though Figure 69.

Table 25. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns

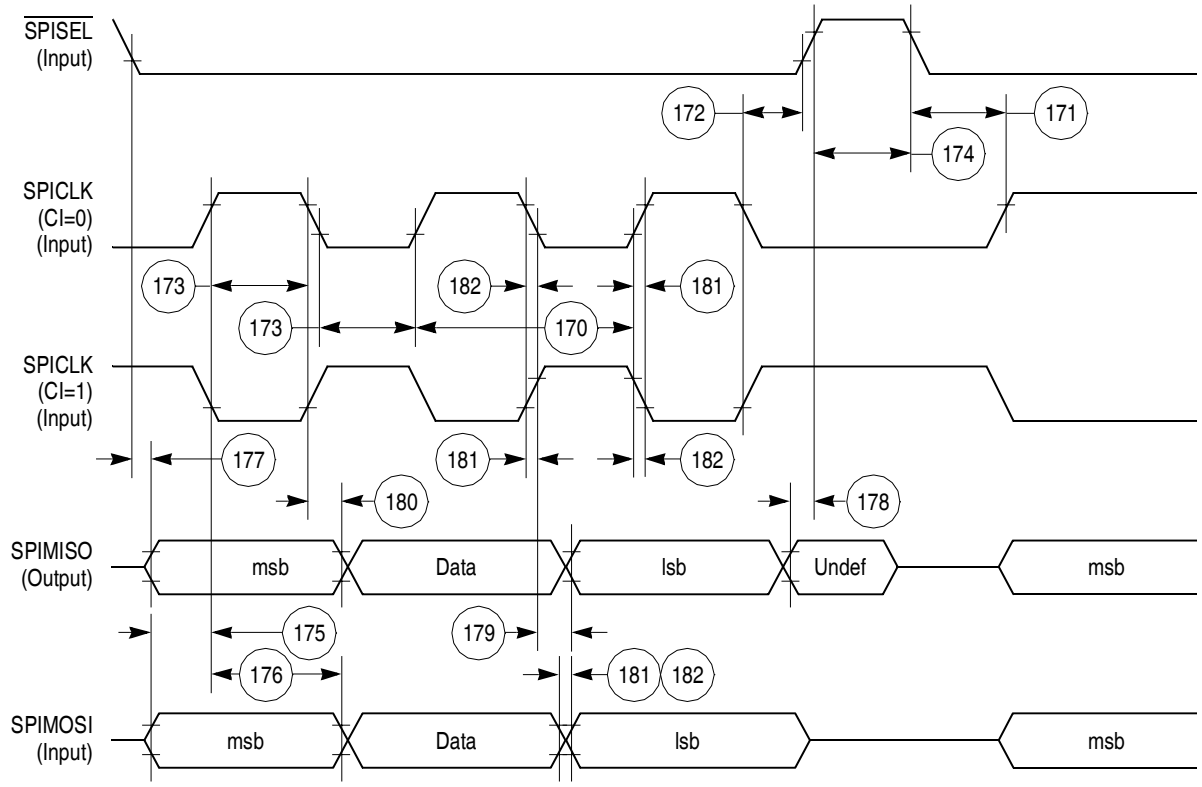


Figure 68. SPI Slave (CP = 0) Timing Diagram

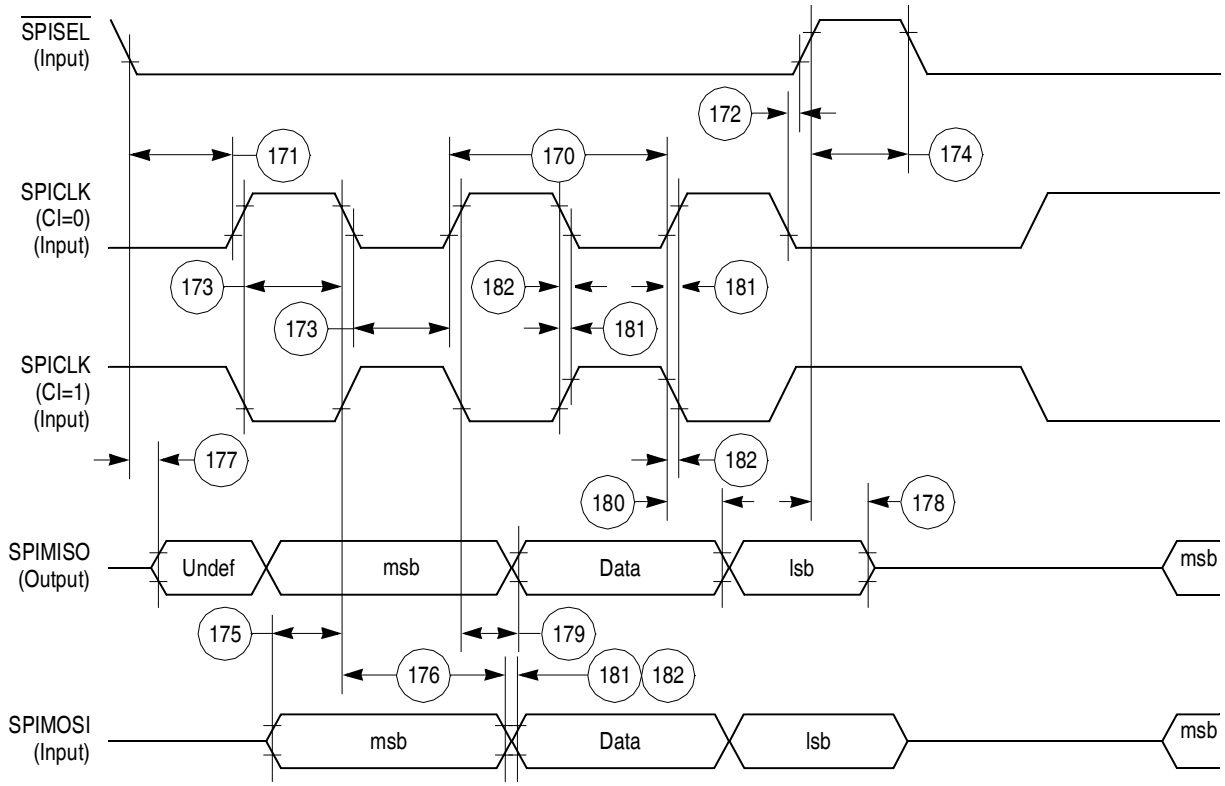


Figure 69. SPI Slave (CP = 1) Timing Diagram

Figure 71 shows signal timings during UTOPIA receive operations.

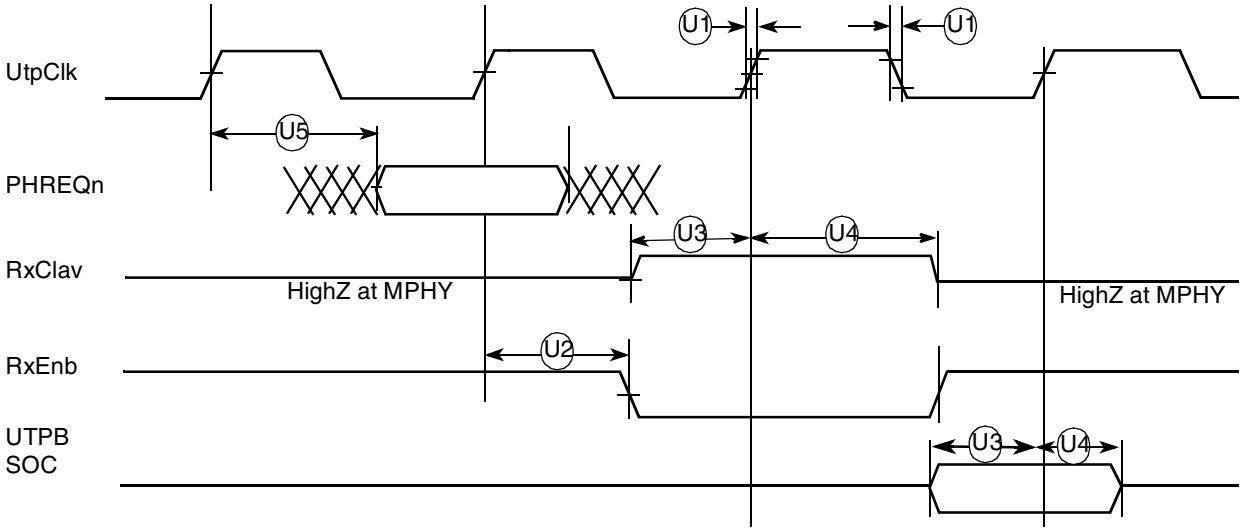


Figure 71. UTOPIA Receive Timing

Figure 72 shows signal timings during UTOPIA transmit operations.

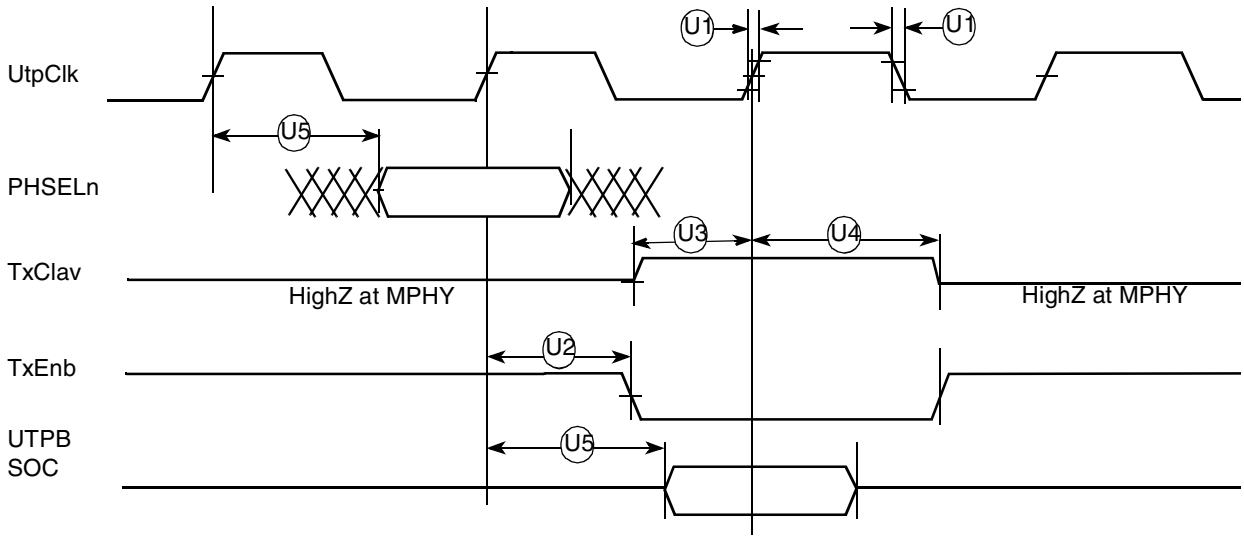


Figure 72. UTOPIA Transmit Timing

13 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Furthermore, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

13.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency - 1%.

Table 29 provides information on the MII receive signal timing.

Table 29. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Figure 73 shows MII receive signal timing.

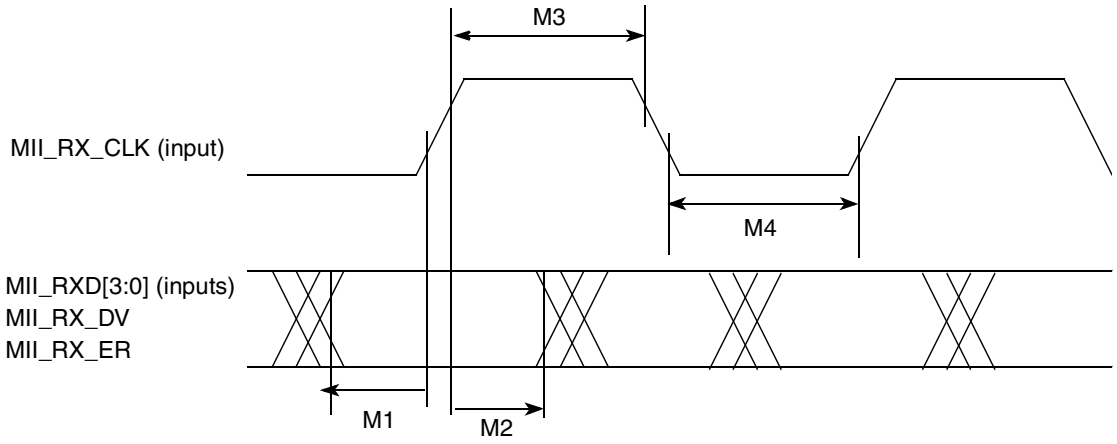


Figure 73. MII Receive Signal Timing Diagram

13.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency - 1%.

Table 30 provides information on the MII transmit signal timing.

Table 30. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	

Table 32. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Figure 76 shows the MII serial management channel timing diagram.

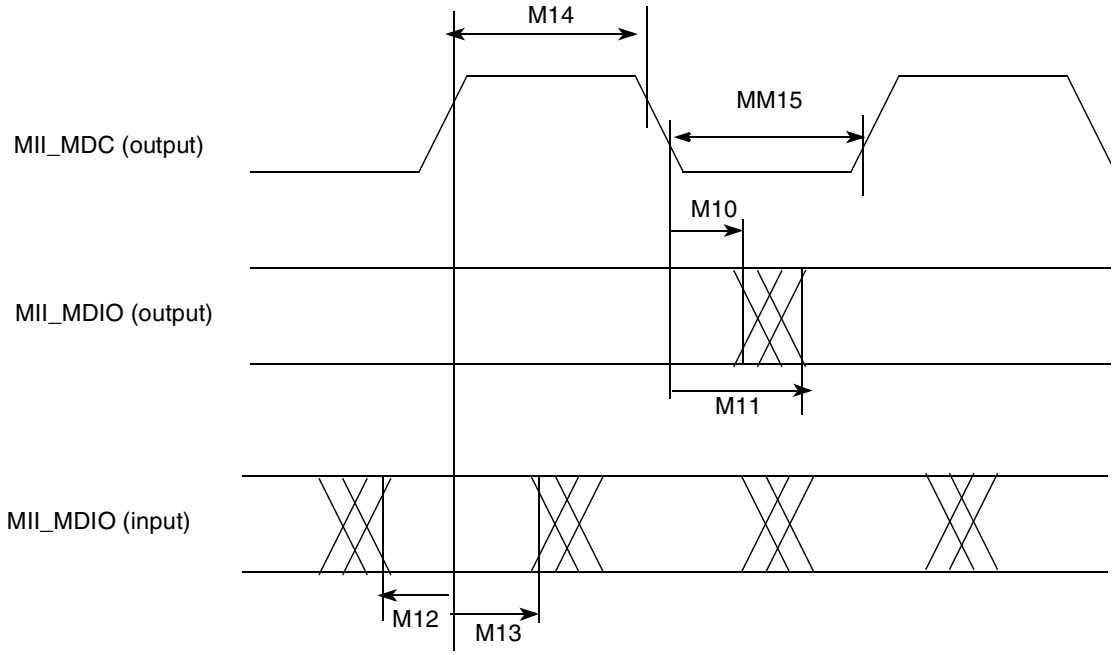


Figure 76. MII Serial Management Channel Timing Diagram

14 Mechanical Data and Ordering Information

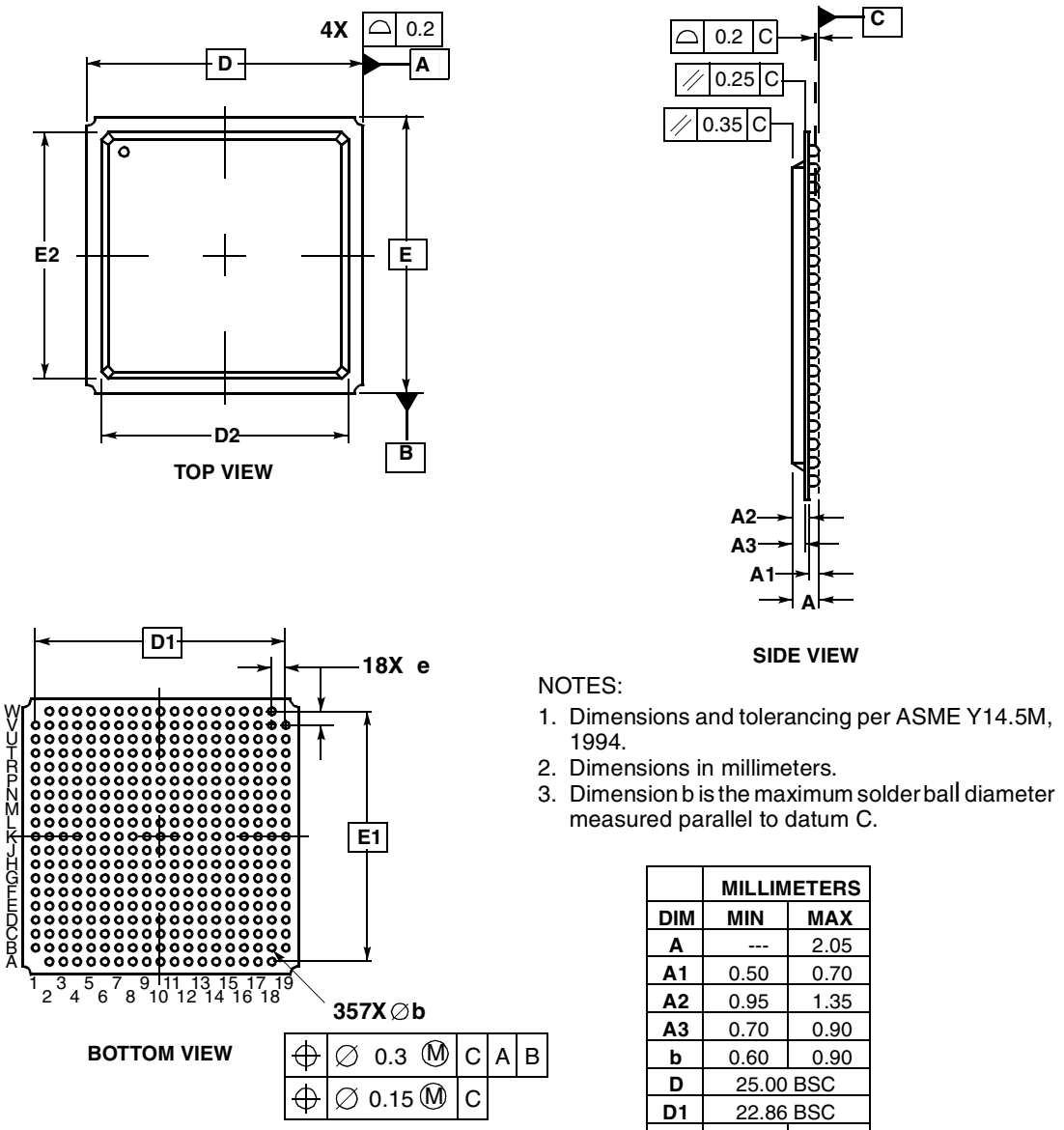
Table 33 provides information on the MPC862/857T/857DSL derivative devices.

Table 33. MPC862/857T/857DSL Derivatives

Device	Number of SCCs [1]	Ethernet Support	Multi-Channel HDLC Support	ATM Support	Cache Size	
					Instruction	Data
MPC862T	Four	10/100 Mbps	Yes	Yes	4 Kbytes	4 Kbytes
MPC862P	Four	10/100 Mbps	Yes	Yes	16 Kbytes	8 Kbytes

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
PC13 L1RQb L1ST3 RTS3	E18	Bidirectional
PC12 L1RQa L1ST4 RTS4	F18	Bidirectional
PC11 CTS1	J19	Bidirectional
PC10 CD1 TGATE1	K19	Bidirectional
PC9 CTS2	L18	Bidirectional
PC8 CD2 TGATE2	M18	Bidirectional
PC7 CTS3 L1TSYNCB SDACK2	M16	Bidirectional
PC6 CD3 L1RSYNCB	R19	Bidirectional
PC5 CTS4 L1TSYNCA SDACK1	T18	Bidirectional
PC4 CD4 L1RSYNCA	T17	Bidirectional
PD15 L1TSYNCA MII-RXD3 UTPB0	U17	Bidirectional
PD14 L1RSYNCA MII-RXD2 UTPB1	V19	Bidirectional
PD13 L1TSYNCB MII-RXD1 UTPB2	V18	Bidirectional



NOTES:
1. Dimensions and tolerancing per ASME Y14.5M, 1994.
2. Dimensions in millimeters.
3. Dimension b is the maximum solder ball diameter measured parallel to datum C.

	MILLIMETERS	
DIM	MIN	MAX
A	---	2.05
A1	0.50	0.70
A2	0.95	1.35
A3	0.70	0.90
b	0.60	0.90
D	25.00 BSC	
D1	22.86 BSC	
D2	22.40	22.60
e	1.27 BSC	
E	25.00 BSC	
E1	22.86 BSC	
E2	22.40	22.60

Case No. 1103-01

Figure 78. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package