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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 115°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc857tczq80b

1 Overview

The MPC862/857T/857DSL is a derivative of Freescale's MPC860 PowerQUICC™ family of devices. It is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC862/857T/857DSL provides enhanced ATM functionality over that of other ATM-enabled members of the MPC860 family.

Table 1 shows the functionality supported by the members of the MPC862/857T/857DSL family.

Table 1. MPC862 Family Functionality

Part	Cache		Ethernet		SCC	SMC
	Instruction Cache	Data Cache	10T	10/100		
MPC862P	16 Kbyte	8 Kbyte	Up to 4	1	4	2
MPC862T	4 Kbyte	4 Kbyte	Up to 4	1	4	2
MPC857T	4 Kbyte	4 Kbyte	1	1	1	2
MPC857DSL	4 Kbyte	4 Kbyte	1	1	1 [1]	1 [2]

[1] On the MPC857DSL, the SCC (SCC1) is for ethernet only. Also, the MPC857DSL does not support the Time Slot Assigner (TSA).

[2] On the MPC857DSL, the SMC (SMC1) is for UART only.

2 Features

The following list summarizes the key MPC862/857T/857DSL features:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch, without conditional execution
  - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1).
    - 16-Kbyte instruction cache (MPC862P) is four-way, set-associative with 256 sets; 4-Kbyte instruction cache (MPC862T, MPC857T, and MPC857DSL) is two-way, set-associative with 128 sets.
    - 8-Kbyte data cache (MPC862P) is two-way, set-associative with 256 sets; 4-Kbyte data cache (MPC862T, MPC857T, and MPC857DSL) is two-way, set-associative with 128 sets.
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully associative instruction and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip-emulation debug mode

- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC) from the PowerPC architecture
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - The MPC862P and MPC862T have 23 internal interrupt sources; the MPC857T and MPC857DSL have 20 internal interrupt sources
  - Programmable priority between SCCs (MPC862P and MPC862T)
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 8-Kbytes of dual-port RAM
  - The MPC862P and MPC862T have 16 serial DMA (SDMA) channels; the MPC857T and MPC857DSL have 10 serial DMA (SDMA) channels
  - Three parallel I/O registers with open-drain capability
- Four baud rate generators
  - Independent (can be connected to any SCC or SMC)
  - Allow changes during operation
  - Autobaud support option
- The MPC862P and MPC862T have four SCCs (serial communication controller) The MPC857T and MPC857DSL have one SCC, SCC1; the MPC857DSL supports ethernet only
  - Serial ATM capability on all SCCs
  - Optional UTOPIA port on SCC4
  - Ethernet/IEEE 802.3 optional on SCC1–4, supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk

Table 4. Power Dissipation (P_D) (continued)

Die Revision	Frequency	Typical [1]	Maximum [2]	Unit
A.1, B.0 (2:1 Mode)	66 MHz	910	1060	mW
	80 MHz	1.06	1.20	W
B.0 (2:1 Mode)	100 MHz	1.35	1.54	W

1 Typical power dissipation is measured at 3.3 V.

2 Maximum power dissipation is measured at 3.5 V.

NOTE

Values in Table 4 represent VDDL based power dissipation and do not include I/O power dissipation over VDDH. I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

6 DC Characteristics

Table 5 provides the DC electrical characteristics for the MPC862/857T/857DSL.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	VDDH, VDDL, KAPWR, VDDSYN	3.135	3.465	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	VDDH – 0.4	VDDH	V
Input High Voltage (all inputs except EXTAL and EXTCLK)	VIH	2.0	5.5	V
Input Low Voltage [1]	VIL	GND	0.8	V
EXTAL, EXTCLK Input High Voltage	VIHC	0.7*(VCC)	VCC+0.3	V
Input Leakage Current, Vin = 5.5 V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I_{in}	—	100	µA
Input Leakage Current, Vin = 3.6 V (Except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI)	I_{In}	—	10	µA
Input Leakage Current, Vin = 0 V (Except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI pins)	I_{In}	—	10	µA
Input Capacitance [2]	C_{in}	—	20	pF
Output High Voltage, IOH = -2.0 mA, VDDH = 3.0 V (Except XTAL, XFC, and Open drain pins)	VOH	2.4	—	V

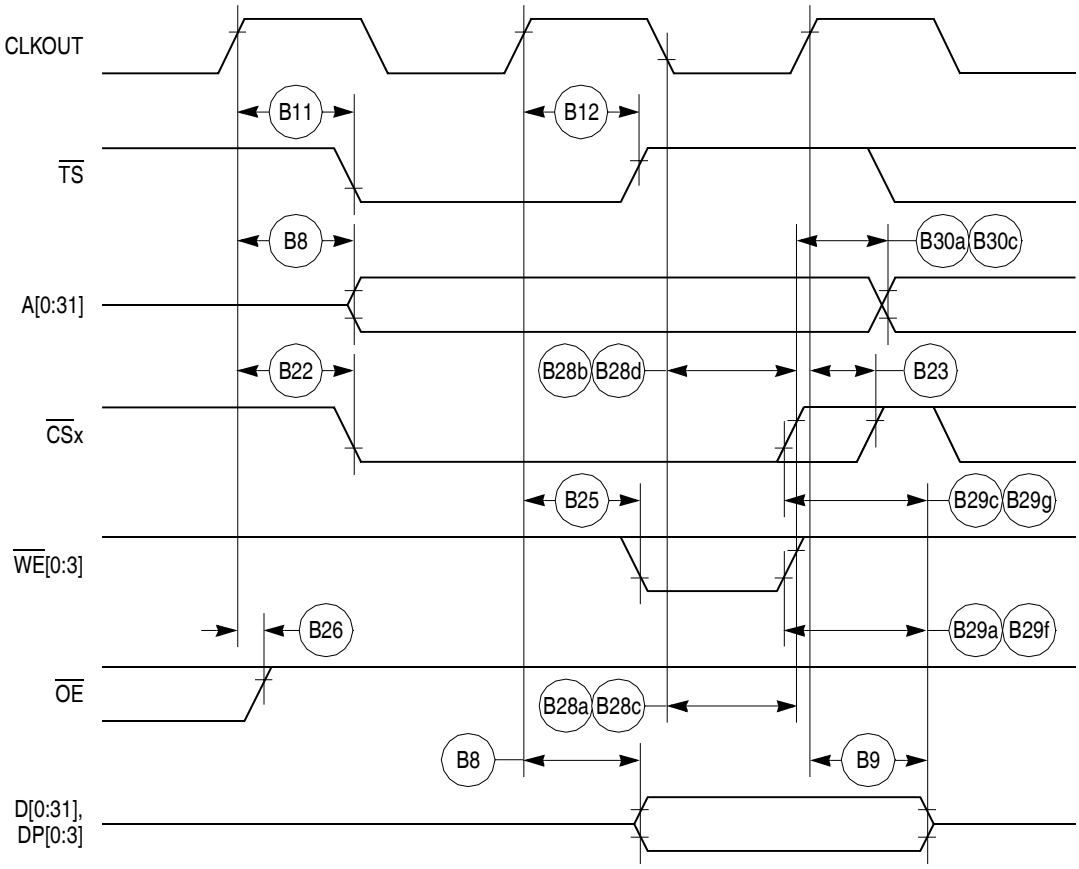

Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0,1 CSNT = 1)

Table 11 shows the debug port timing for the MPC862/857T/857DSL.

Table 11. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
D61	DSCK cycle time	3 x $T_{CLOCKOUT}$		-
D62	DSCK clock pulse width	1.25 x $T_{CLOCKOUT}$		-
D63	DSCK rise and fall times	0.00	3.00	ns
D64	DSDI input data setup time	8.00		ns
D65	DSDI data hold time	5.00		ns
D66	DSCK low to DSDO data valid	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 31 provides the input timing for the debug port clock.

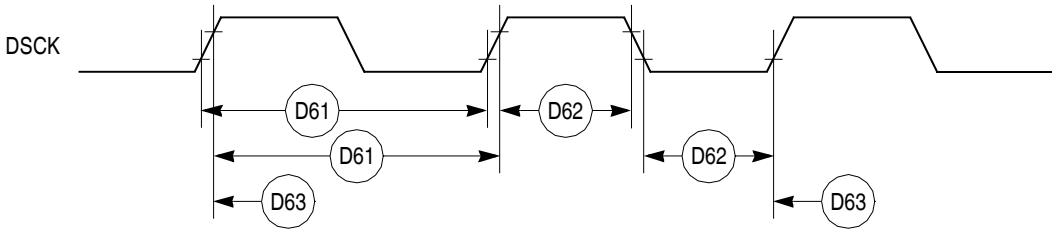

Figure 31. Debug Port Clock Input Timing

Figure 32 provides the timing for the debug port.

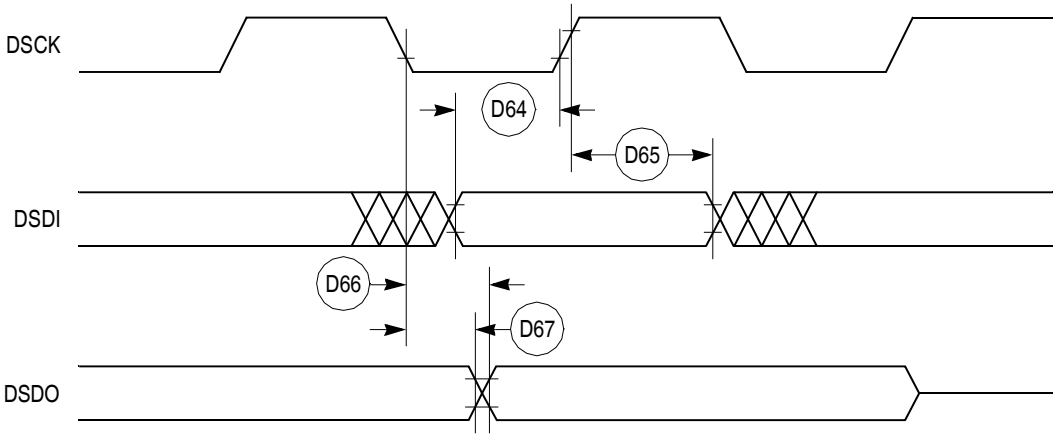

Figure 32. Debug Port Timings

Figure 33 shows the reset timing for the data bus configuration.

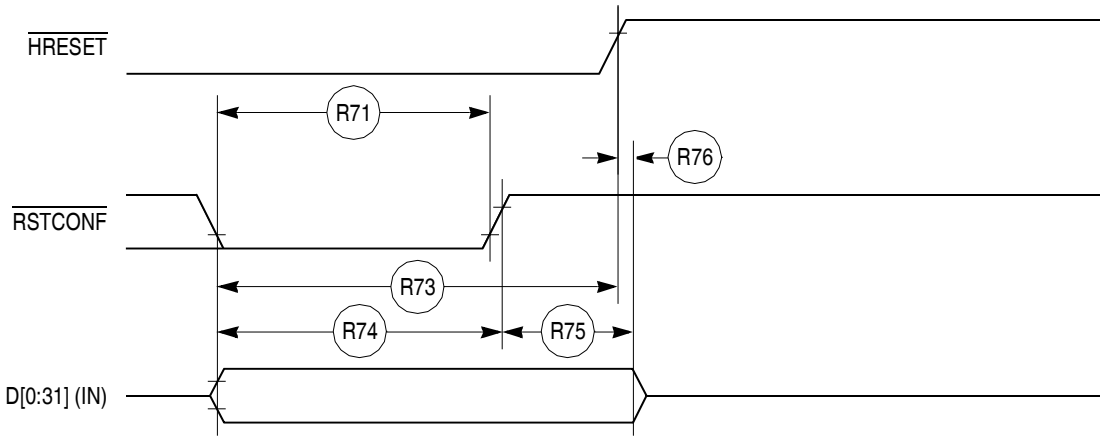

Figure 33. Reset Timing—Configuration from Data Bus

Figure 34 provides the reset timing for the data bus weak drive during configuration.

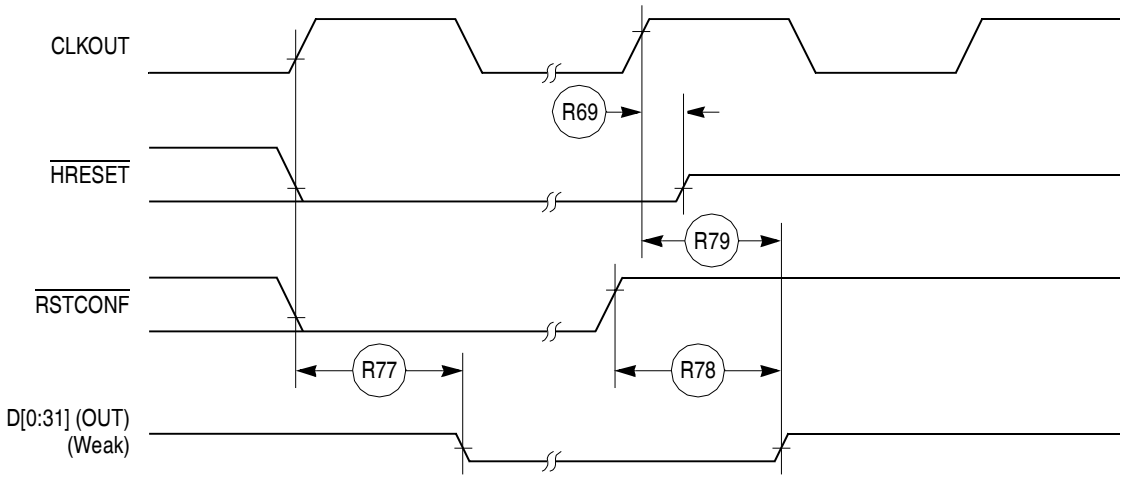

Figure 34. Reset Timing—Data Bus Weak Drive during Configuration

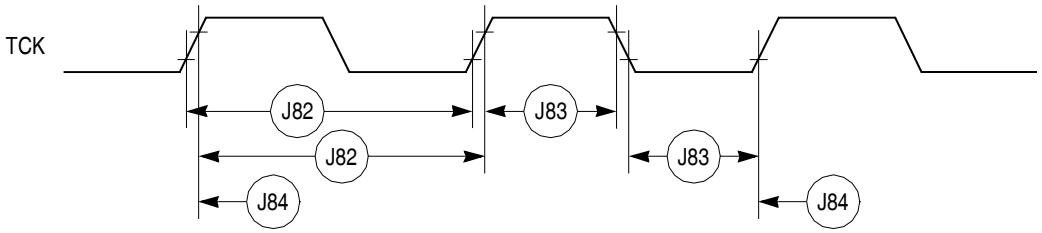

Figure 36. JTAG Test Clock Input Timing

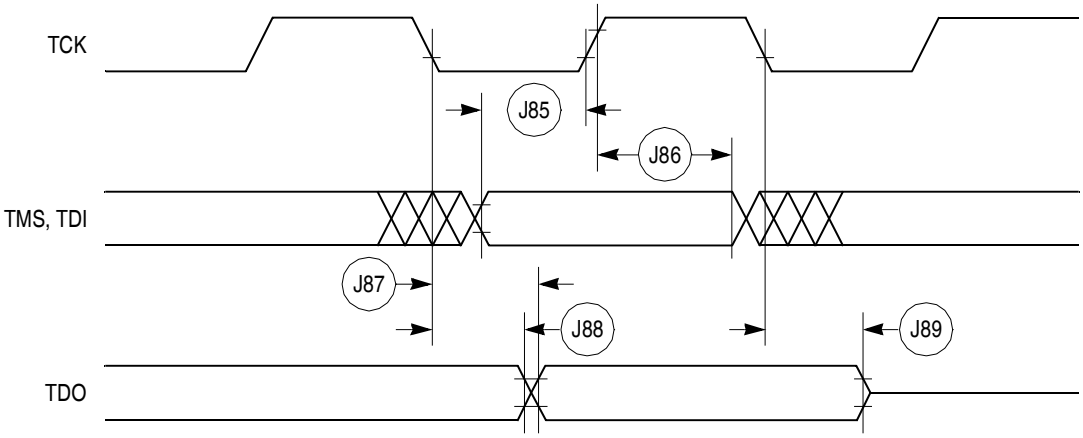

Figure 37. JTAG Test Access Port Timing Diagram

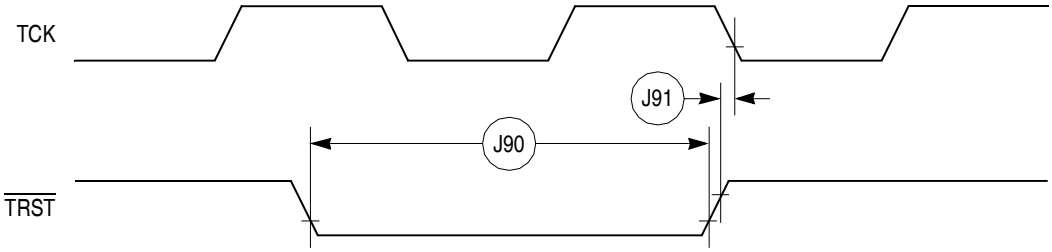

Figure 38. JTAG $\overline{\text{TRST}}$ Timing Diagram

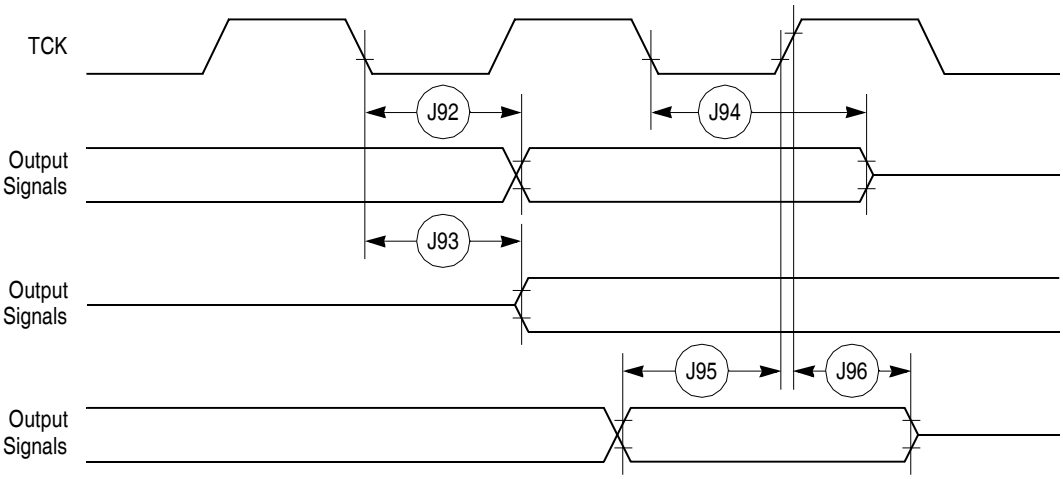

Figure 39. Boundary Scan (JTAG) Timing Diagram

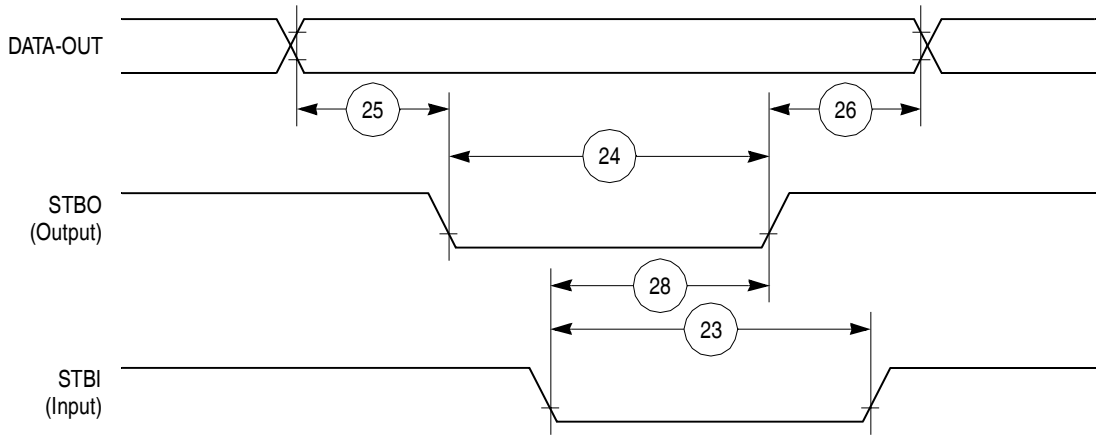

Figure 41. PIP Tx (Interlock Mode) Timing Diagram

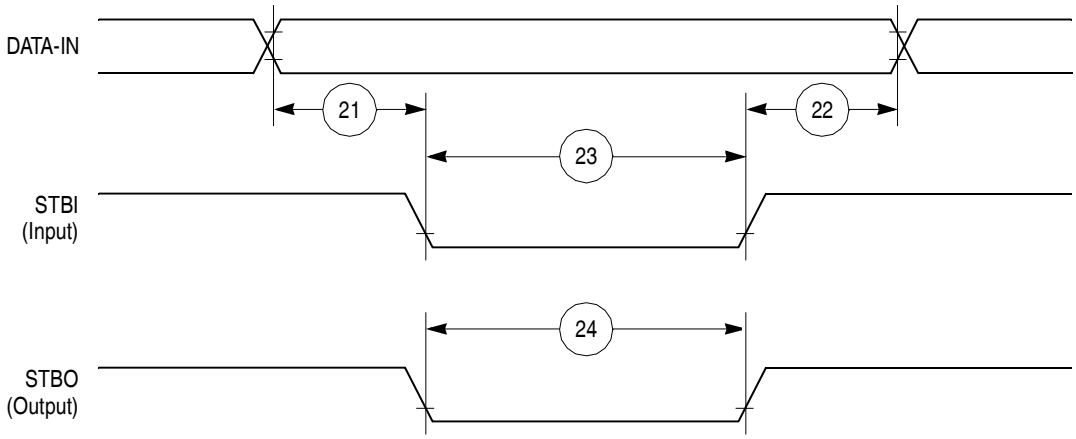

Figure 42. PIP Rx (Pulse Mode) Timing Diagram

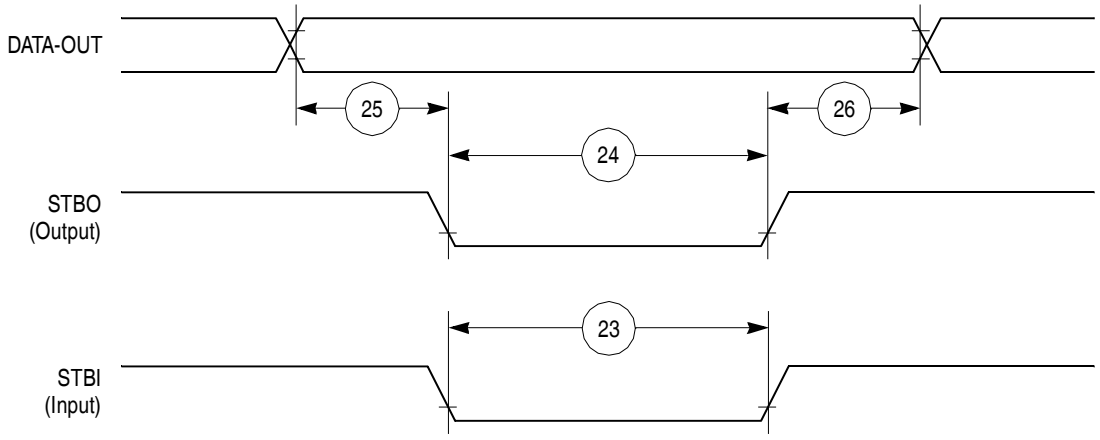

Figure 43. PIP TX (Pulse Mode) Timing Diagram

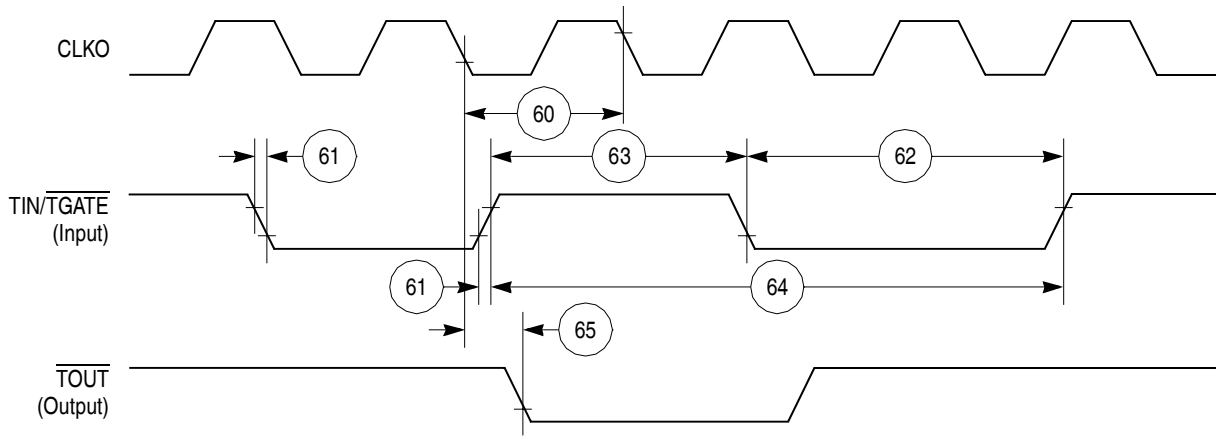

Figure 51. CPM General-Purpose Timers Timing Diagram

11.6 Serial Interface AC Electrical Specifications

Table 19 provides the serial interface timings as shown in Figure 52 though Figure 56.

Table 19. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLK, L1TCLK frequency (DSC = 0) [1, 2]	—	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0) [2]	P + 10	—	ns
71a	L1RCLK, L1TCLK width high (DSC = 0) [3]	P + 10	—	ns
72	L1TXD, L1ST(1–4), $\overline{\text{L1RQ}}$, L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20.00	—	ns
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1–4) valid [4]	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1–4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1–4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid [4]	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns

Table 19. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
83a	L1RCLK, L1TCLK width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4]	1.00	—	L1TCLK
86	L1GR setup time[2]	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

1 The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

2 These specs are valid for IDL mode only.

3 Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

4 These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.

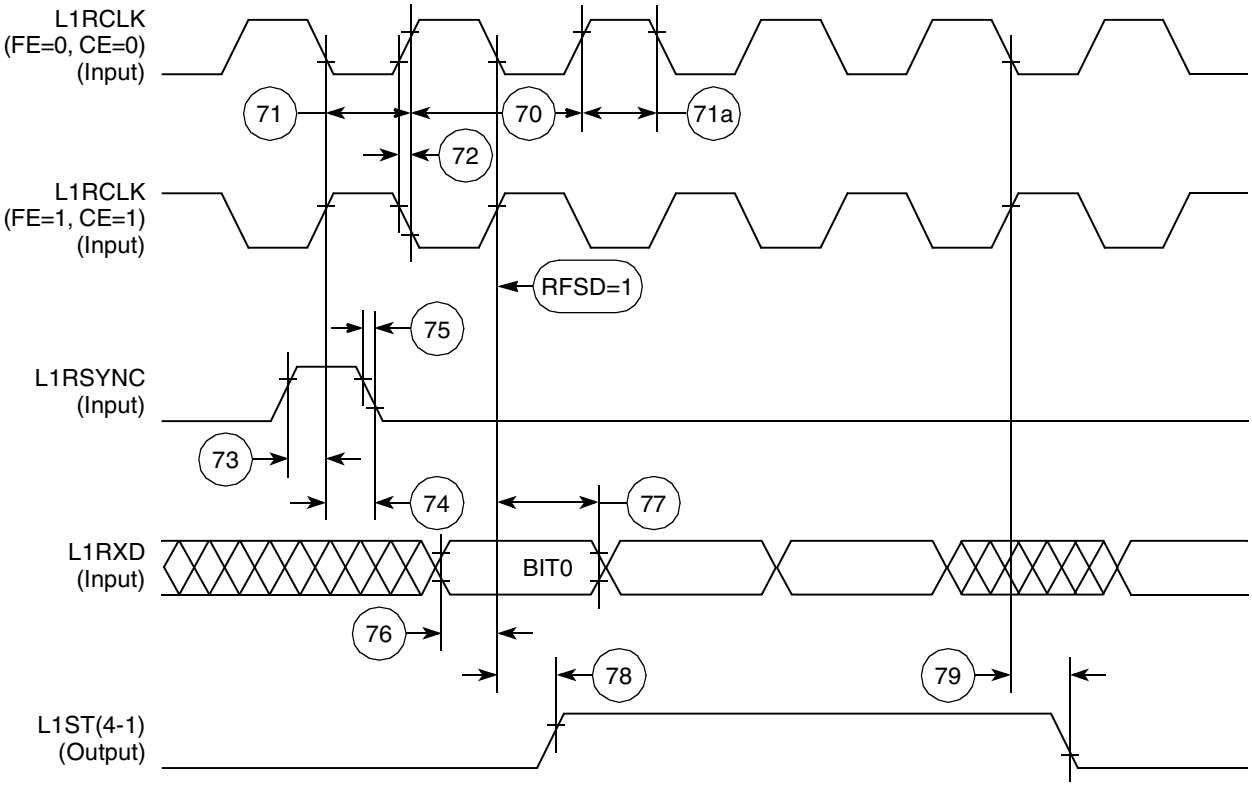

Figure 52. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

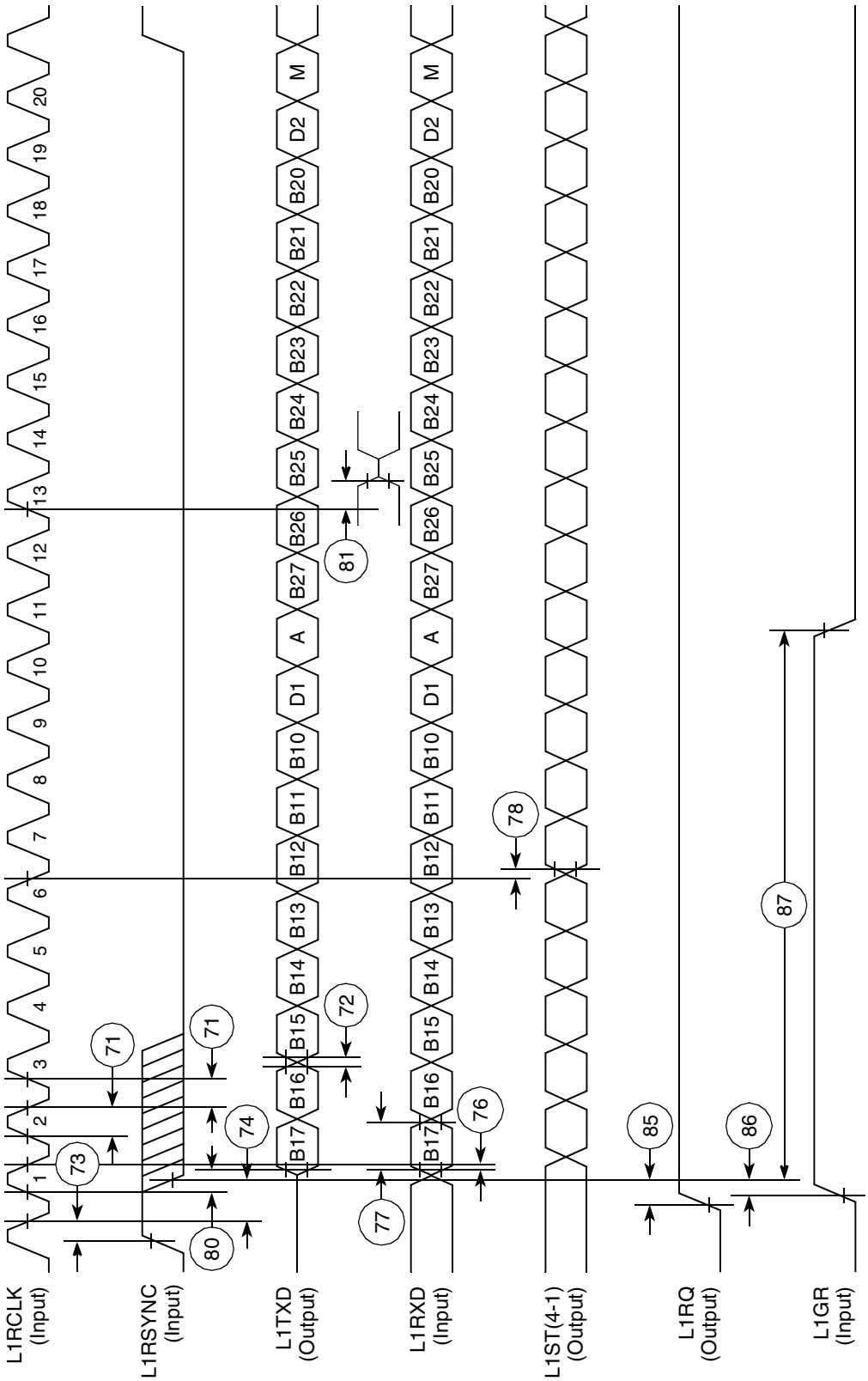

Figure 56. IDL Timing

Figure 57 through Figure 59 show the NMSI timings.

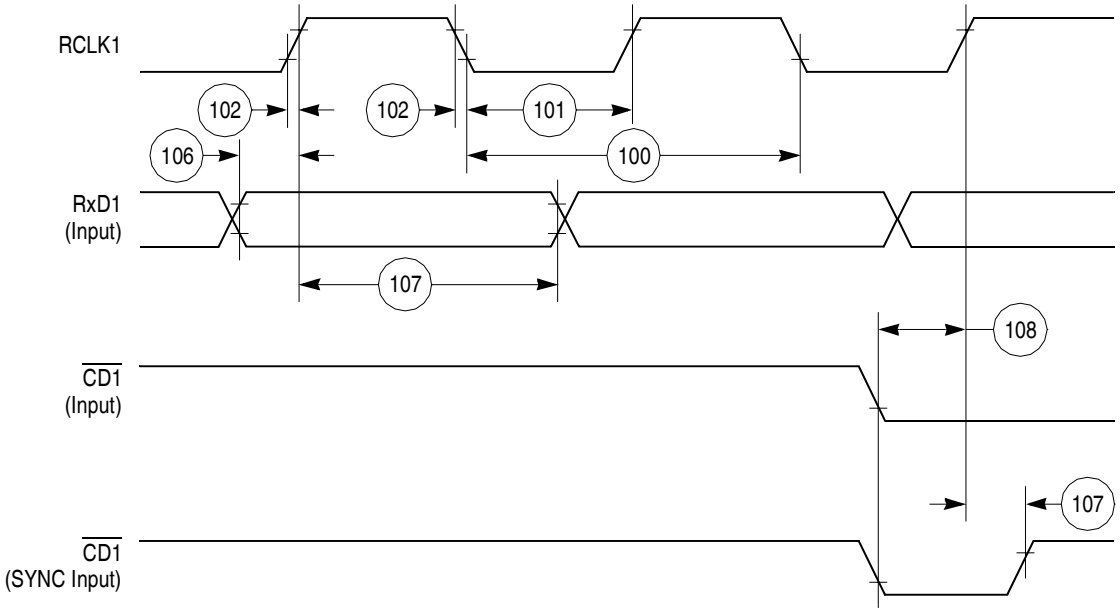

Figure 57. SCC NMSI Receive Timing Diagram

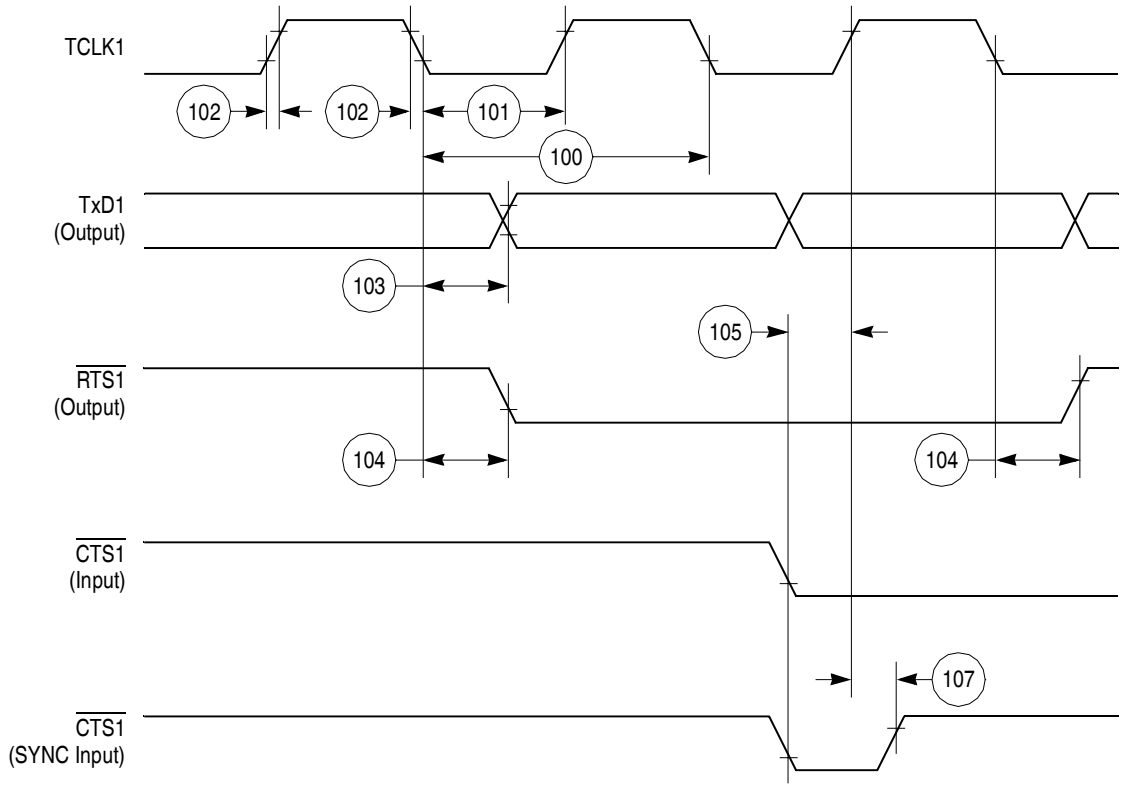

Figure 58. SCC NMSI Transmit Timing Diagram

11.10 SPI Master AC Electrical Specifications

Table 24 provides the SPI master timings as shown in Figure 66 though Figure 67.

Table 24. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	15	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	10	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

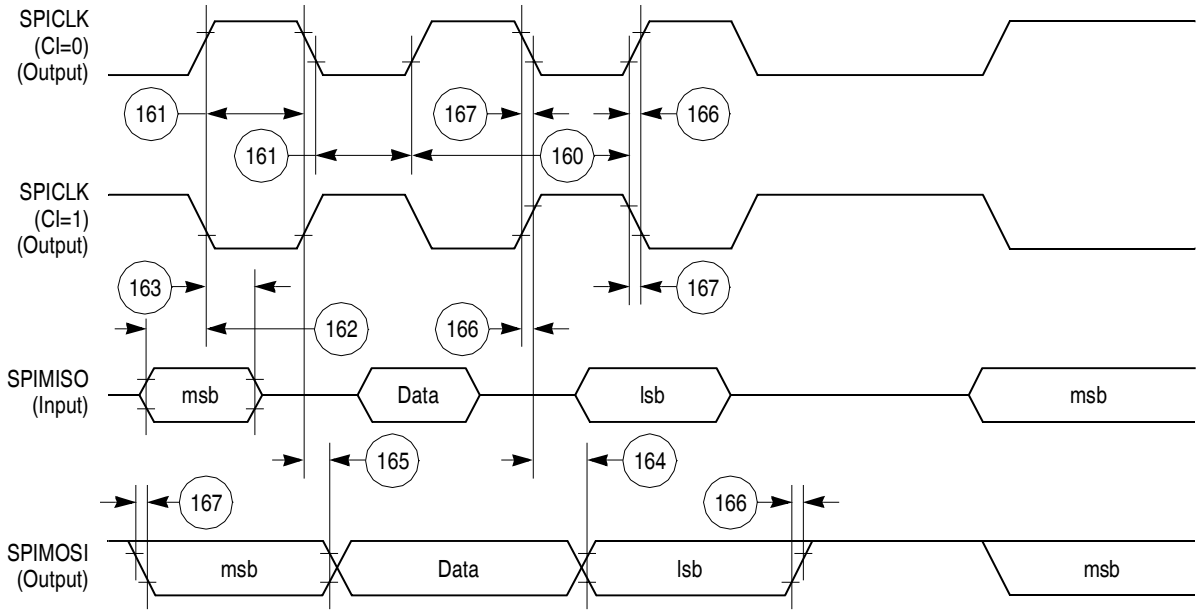

Figure 66. SPI Master (CP = 0) Timing Diagram

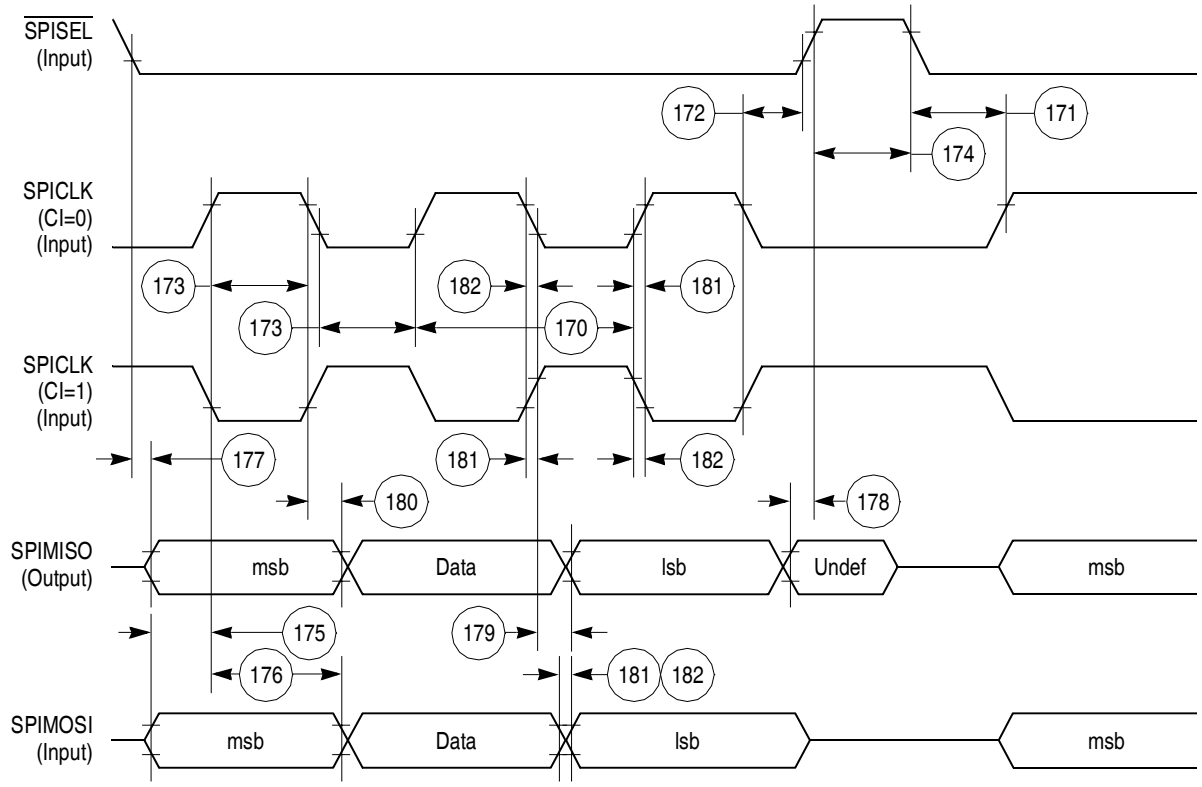

Figure 68. SPI Slave (CP = 0) Timing Diagram

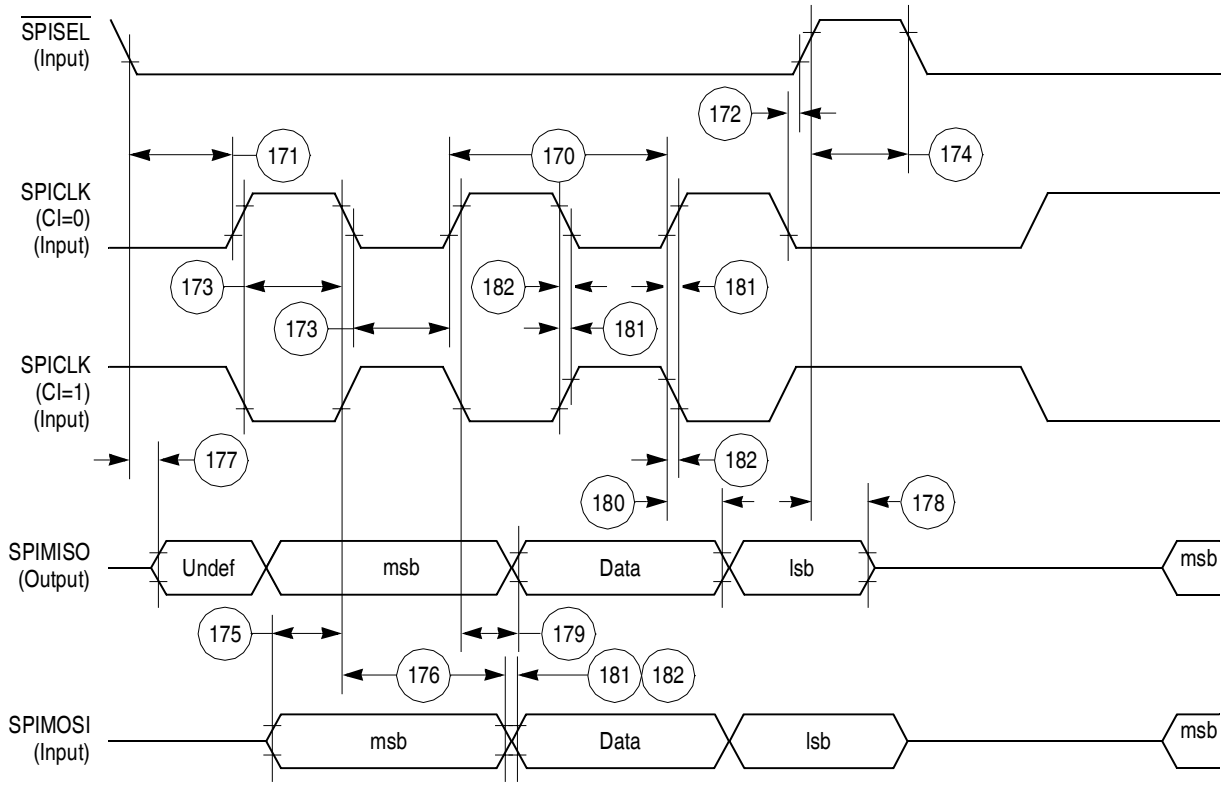

Figure 69. SPI Slave (CP = 1) Timing Diagram

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
$\overline{BR}$	G4	Bidirectional
$\overline{BG}$	E2	Bidirectional
$\overline{BB}$	E1	Bidirectional Active Pull-up
FRZ $\overline{IRQ6}$	G3	Bidirectional
$\overline{IRQ0}$	V14	Input
$\overline{IRQ1}$	U14	Input
M_TX_CLK $\overline{IRQ7}$	W15	Input
$\overline{CS}$[0:5]	C3, A2, D4, E4, A4, B4	Output
$\overline{CS6}$ $\overline{CE1\_B}$	D5	Output
$\overline{CS7}$ $\overline{CE2\_B}$	C4	Output
$\overline{WE0}$ $\overline{BS\_B0}$ $\overline{IORD}$	C7	Output
$\overline{WE1}$ $\overline{BS\_B1}$ $\overline{IOWR}$	A6	Output
$\overline{WE2}$ $\overline{BS\_B2}$ $\overline{PCOE}$	B6	Output
$\overline{WE3}$ $\overline{BS\_B3}$ $\overline{PCWE}$	A5	Output
$\overline{BS\_A}$[0:3]	D8, C8, A7, B8	Output
$\overline{GPL\_A0}$ $\overline{GPL\_B0}$	D7	Output
$\overline{OE}$ $\overline{GPL\_A1}$ $\overline{GPL\_B1}$	C6	Output
$\overline{GPL\_A}$[2:3] $\overline{GPL\_B}$[2:3] $\overline{CS}$[2–3]	B5, C5	Output
UPWAITA $\overline{GPL\_A4}$	C1	Bidirectional
UPWAITB $\overline{GPL\_B4}$	B1	Bidirectional

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
IP_A6 UTPB_Split6[2] MII-TXERR	T6	Input
IP_A7 UTPB_Split7[2] MII-RXDV	T3	Input
ALE_B DSCK/AT1	J1	Bidirectional Three-state
IP_B[0:1] IWP[0:1] VFLS[0:1]	H2, J3	Bidirectional
IP_B2 IOIS16_B AT2	J2	Bidirectional Three-state
IP_B3 IWP2 VF2	G1	Bidirectional
IP_B4 LWP0 VF0	G2	Bidirectional
IP_B5 LWP1 VF1	J4	Bidirectional
IP_B6 DSDI AT0	K3	Bidirectional Three-state
IP_B7 PTR AT3	H1	Bidirectional Three-state
OP0 MII-TXD0 UtpClk_Split[2]	L4	Bidirectional
OP1	L2	Output
OP2 MODCK1 STS	L1	Bidirectional
OP3 MODCK2 DSDO	M4	Bidirectional
BADDR30 REG	K4	Output
BADDR[28:29]	M3, M2	Output
AS	L3	Input

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
PA2 CLK6 TOUT3 L1RCLKB	R18	Bidirectional
PA1 CLK7 BRGO4 TIN4	T19	Bidirectional
PA0 CLK8 TOUT4 L1TCLKB	U19	Bidirectional
PB31 SPISEL REJECT1	C17	Bidirectional (Optional: Open-drain)
PB30 SPICLK RSTRT2	C19	Bidirectional (Optional: Open-drain)
PB29 SPIMOSI	E16	Bidirectional (Optional: Open-drain)
PB28 SPIMISO BRGO4	D19	Bidirectional (Optional: Open-drain)
PB27 I2CSDA BRGO1	E19	Bidirectional (Optional: Open-drain)
PB26 I2CSCL BRGO2	F19	Bidirectional (Optional: Open-drain)
PB25 RXADDR3[2] SMTXD1	J16	Bidirectional (Optional: Open-drain)
PB24 TXADDR3[2] SMRXD1	J18	Bidirectional (Optional: Open-drain)
PB23 TXADDR2[2] SDACK1 SMSYN1	K17	Bidirectional (Optional: Open-drain)
PB22 TXADDR4[2] SDACK2 SMSYN2	L19	Bidirectional (Optional: Open-drain)

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
PC13 L1RQb L1ST3 RTS3	E18	Bidirectional
PC12 L1RQa L1ST4 RTS4	F18	Bidirectional
PC11 CTS1	J19	Bidirectional
PC10 CD1 TGATE1	K19	Bidirectional
PC9 CTS2	L18	Bidirectional
PC8 CD2 TGATE2	M18	Bidirectional
PC7 CTS3 L1TSYNCB SDACK2	M16	Bidirectional
PC6 CD3 L1RSYNCB	R19	Bidirectional
PC5 CTS4 L1TSYNCA SDACK1	T18	Bidirectional
PC4 CD4 L1RSYNCA	T17	Bidirectional
PD15 L1TSYNCA MII-RXD3 UTPB0	U17	Bidirectional
PD14 L1RSYNCA MII-RXD2 UTPB1	V19	Bidirectional
PD13 L1TSYNCB MII-RXD1 UTPB2	V18	Bidirectional

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
PD12 L1RSYNCB MII-MDC UTPB3	R16	Bidirectional
PD11 RXD3 MII-TXERR $\overline{\text{RXENB}}$	T16	Bidirectional
PD10 TXD3 MII-RXD0 $\overline{\text{TXENB}}$	W18	Bidirectional
PD9 RXD4 MII-TXD0 UTPCLK	V17	Bidirectional
PD8 TXD4 MII-MDC MII-RXCLK	W17	Bidirectional
PD7 $\overline{\text{RTS3}}$ MII-RXERR UTPB4	T15	Bidirectional
PD6 $\overline{\text{RTS4}}$ MII-RXDV UTPB5	V16	Bidirectional
PD5 $\overline{\text{REJECT2}}$ MII-TXD3 UTPB6	U15	Bidirectional
PD4 $\overline{\text{REJECT3}}$ MII-TXD2 UTPB7	U16	Bidirectional
PD3 $\overline{\text{REJECT4}}$ MII-TXD1 SOC	W16	Bidirectional
TMS	G18	Input
TDI DSDI	H17	Input
TCK DSCK	H16	Input

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