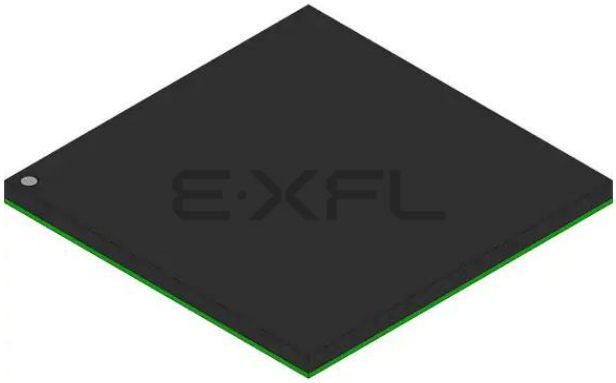

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc857tzq100b

  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels) (The MPC857DSL has one SMC, SMC1 for UART)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division multiplexed (TDM) channels
- One serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multiple-master operation on the same bus
- One inter-integrated circuit (I^2C) port
  - Supports master and slave modes
  - Multiple-master environment support
- Time-slot assigner (TSA) (The MPC857DSL does not have the TSA)
  - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, clocking
  - Allows dynamic changes
  - On the MPC862P and MPC862T, can be internally connected to six serial channels (four SCCs and two SMCs); on the MPC857T, can be connected to three serial channels (one SCC and two SMCs)
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on MPC862/857T/857DSL or MC68360
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports one or two PCMCIA sockets dependent upon whether ESAR functionality is enabled
  - 8 memory or I/O windows supported
- Low power support
  - Full on—All units fully powered
  - Doze—Core functional units disabled except time base decrementer, PLL, memory controller, RTC, and CPM in low-power standby

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature; see Figure 3.

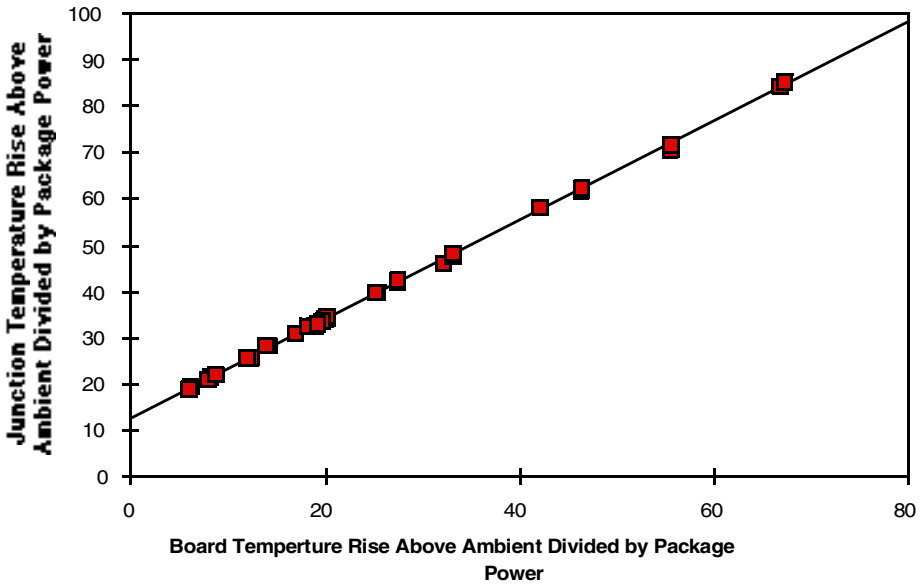


Figure 3. Effect of Board Temperature Rise on Thermal Behavior

7.6 References

Semiconductor Equipment and Materials International 805 East Middlefield Rd. Mountain View, CA 94043	(415) 964-5111
MIL-SPEC and EIA/JESD (JEDEC) Specifications (Available from Global Engineering Documents)	800-854-7179 or 303-397-7956
JEDEC Specifications	http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

8 Layout Practices

Each V_{CC} pin on the MPC862/857T/857DSL should be provided with a low-impedance path to the board’s supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC862/857T/857DSL have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

9 Bus Signal Timing

The maximum bus speed supported by the MPC862/857T/857DSL is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC862/857T/857DSL used at 80MHz must be configured for a 40 MHz bus). Table 6 shows the period ranges for standard part frequencies.

Table 6. Period Range for Standard Part Frequencies

Freq	50 MHz		66 MHz		80 MHz		100 MHz	
	Min	Max	Min	Max	Min	Max	Min	Max
Period	20.00	30.30	15.15	30.30	25.00	30.30	20.00	30.30

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B32c	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 x B1 + 6.60)	9.40	18.00	7.60	16.00	13.30	14.10	11.30	12.30	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid - as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{GPL}$ Valid - as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by CST2 in the corresponding word in UPM (MIN = 0.75 x B1 - 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid - as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - As Requested by BST1 in the corresponding word in the UPM (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 x B1 - 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns

Figure 8 provides the timing for the synchronous input signals.

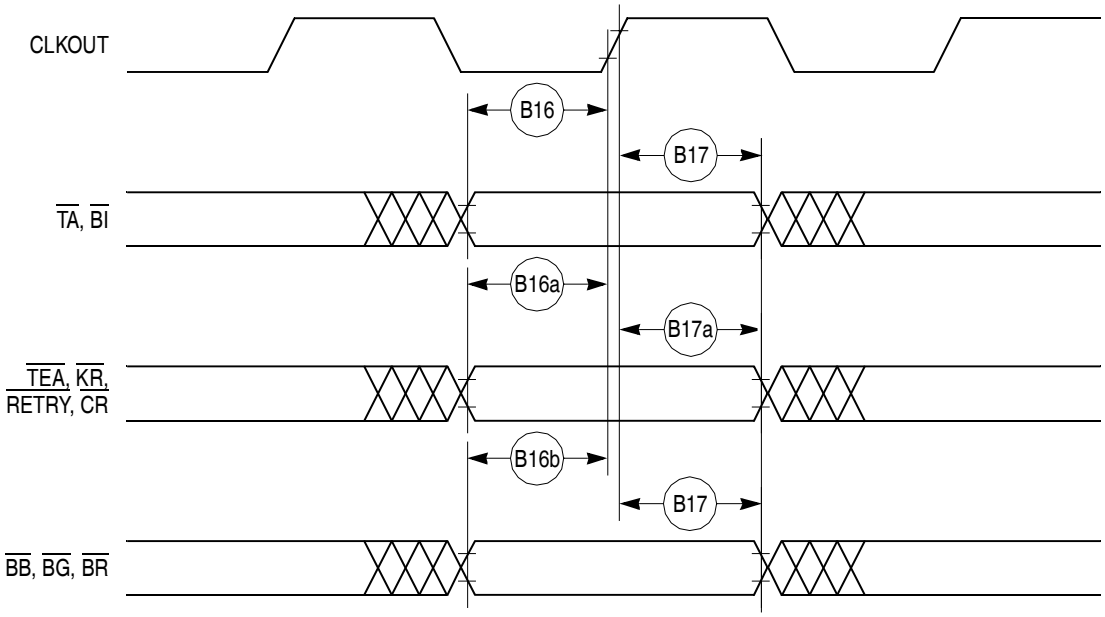


Figure 8. Synchronous Input Signals Timing

Figure 9 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

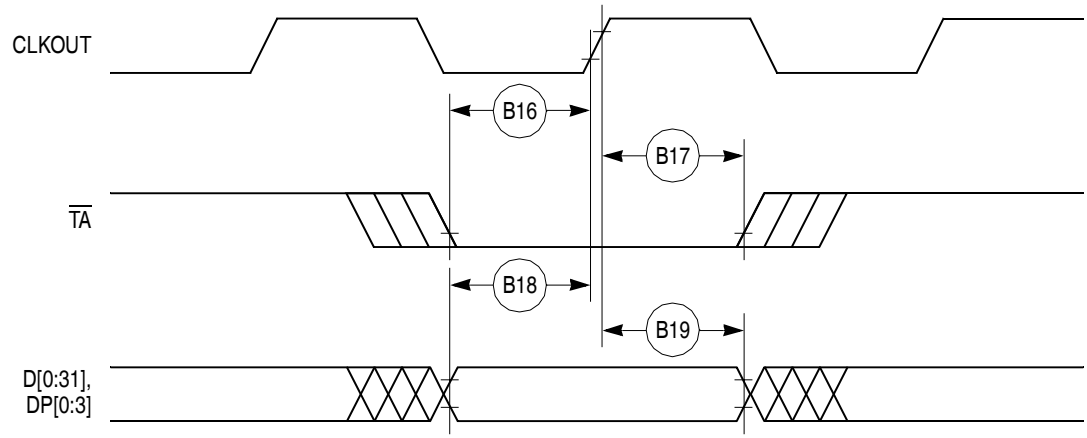


Figure 9. Input Data Timing in Normal Case

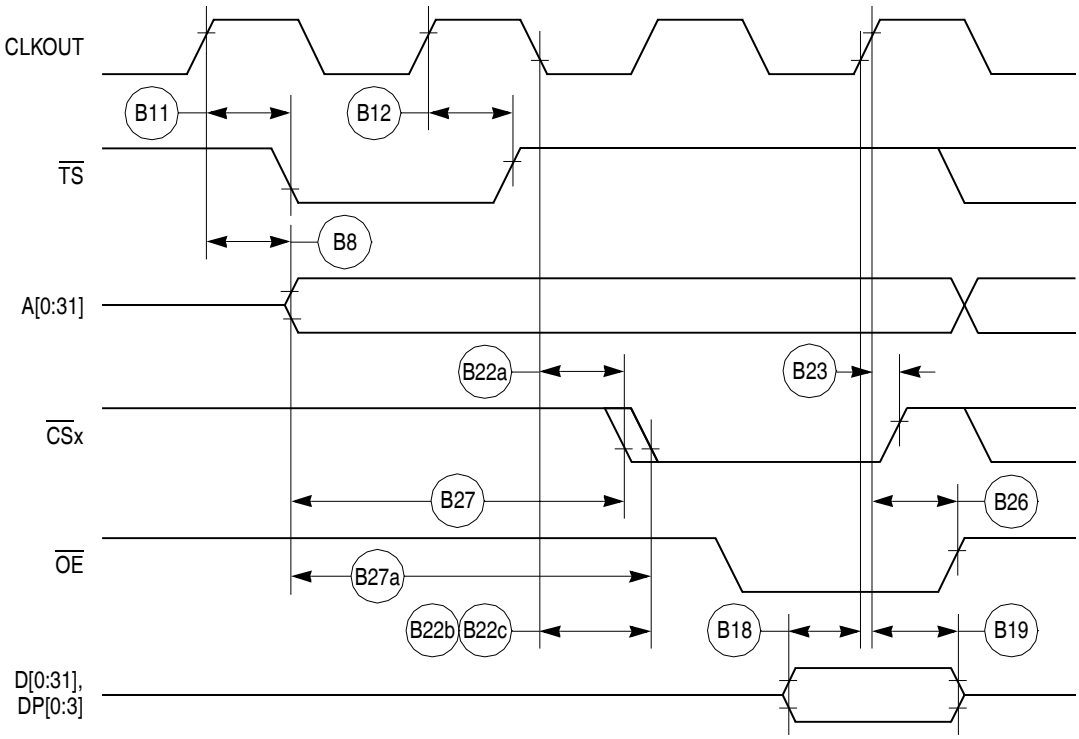


Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

Figure 15 through Figure 17 provide the timing for the external bus write controlled by various GPCM factors.

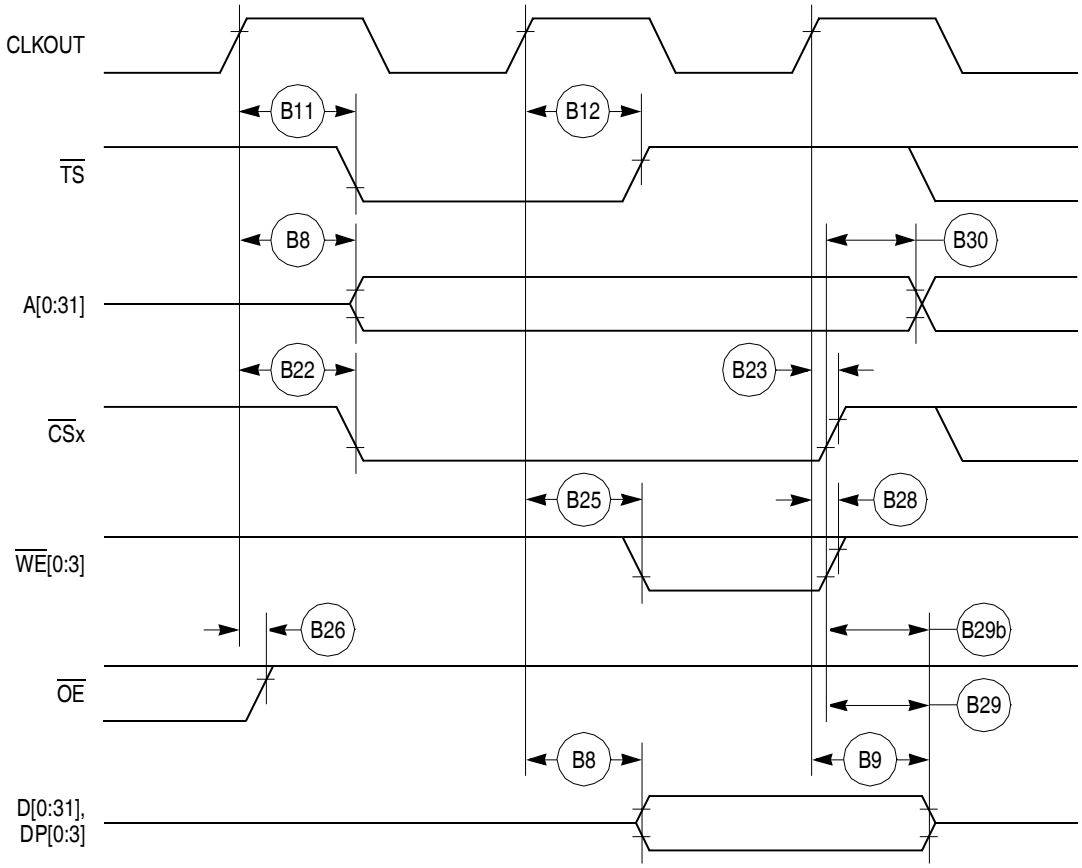


Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0,1 CSNT = 0)

Figure 18 provides the timing for the external bus controlled by the UPM.

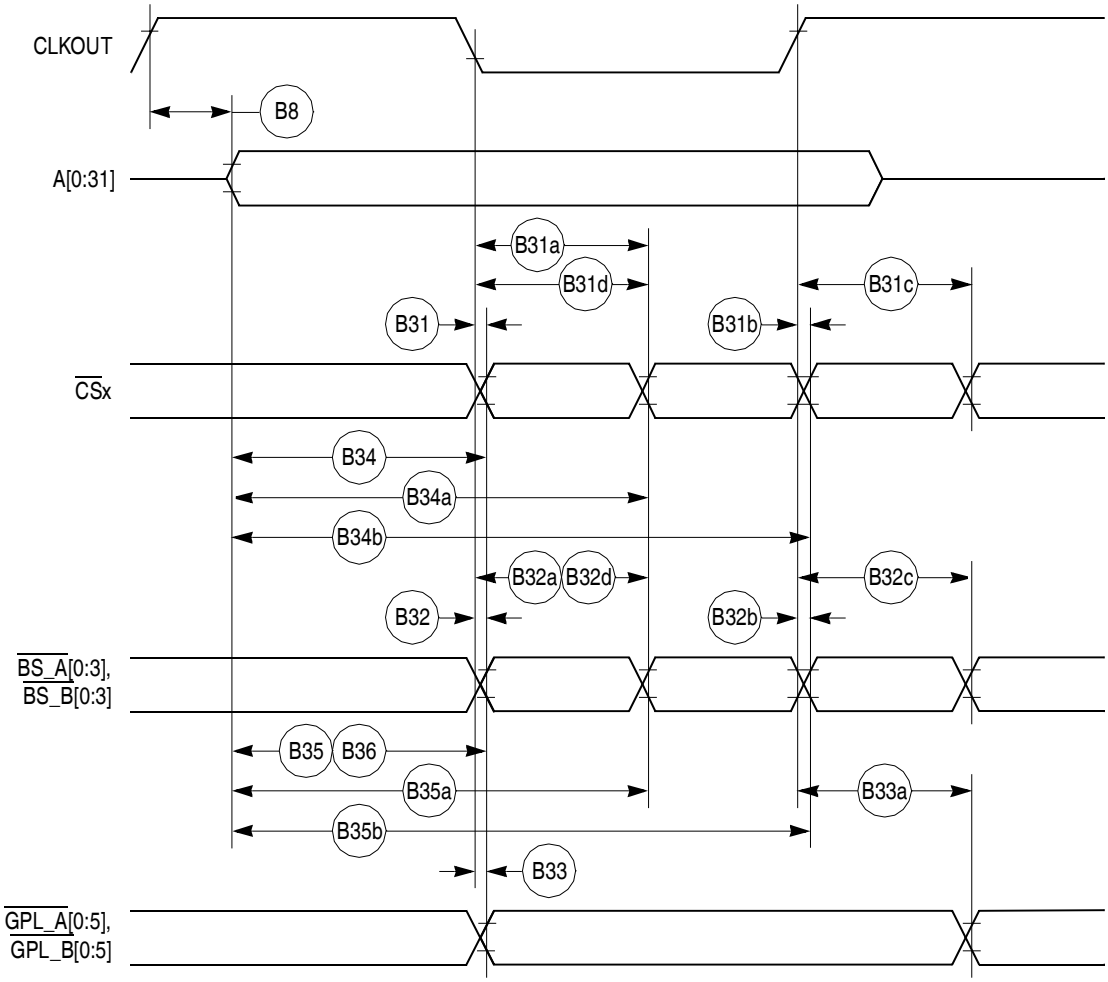


Figure 18. External Bus Timing (UPM Controlled Signals)

Figure 21 provides the timing for the synchronous external master access controlled by the GPCM.

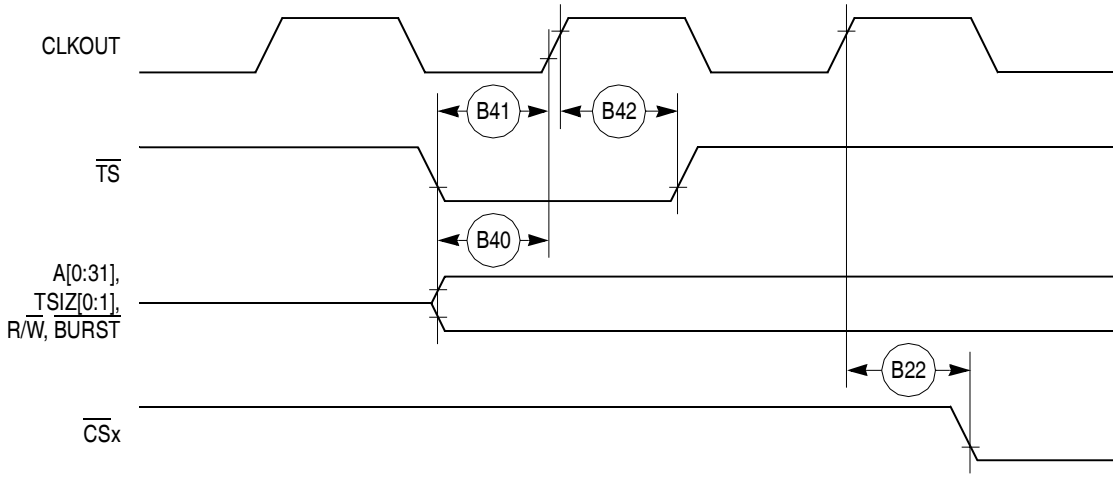


Figure 21. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 22 provides the timing for the asynchronous external master memory access controlled by the GPCM.

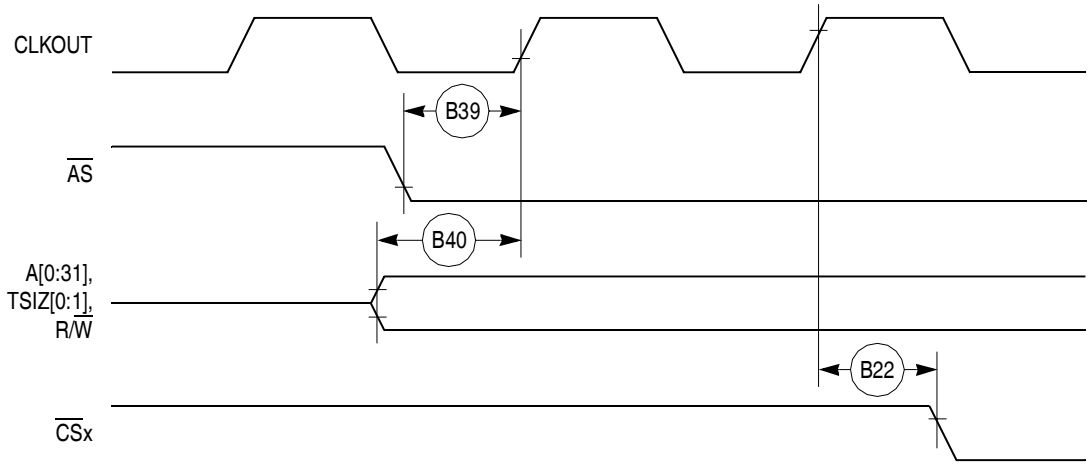


Figure 22. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 23 provides the timing for the asynchronous external master control signals negation.

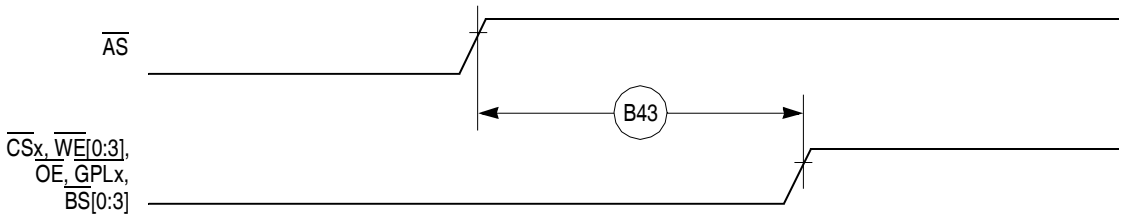


Figure 23. Asynchronous External Master—Control Signals Negation Timing

Figure 27 provides the PCMCIA access cycle timing for the external bus write.

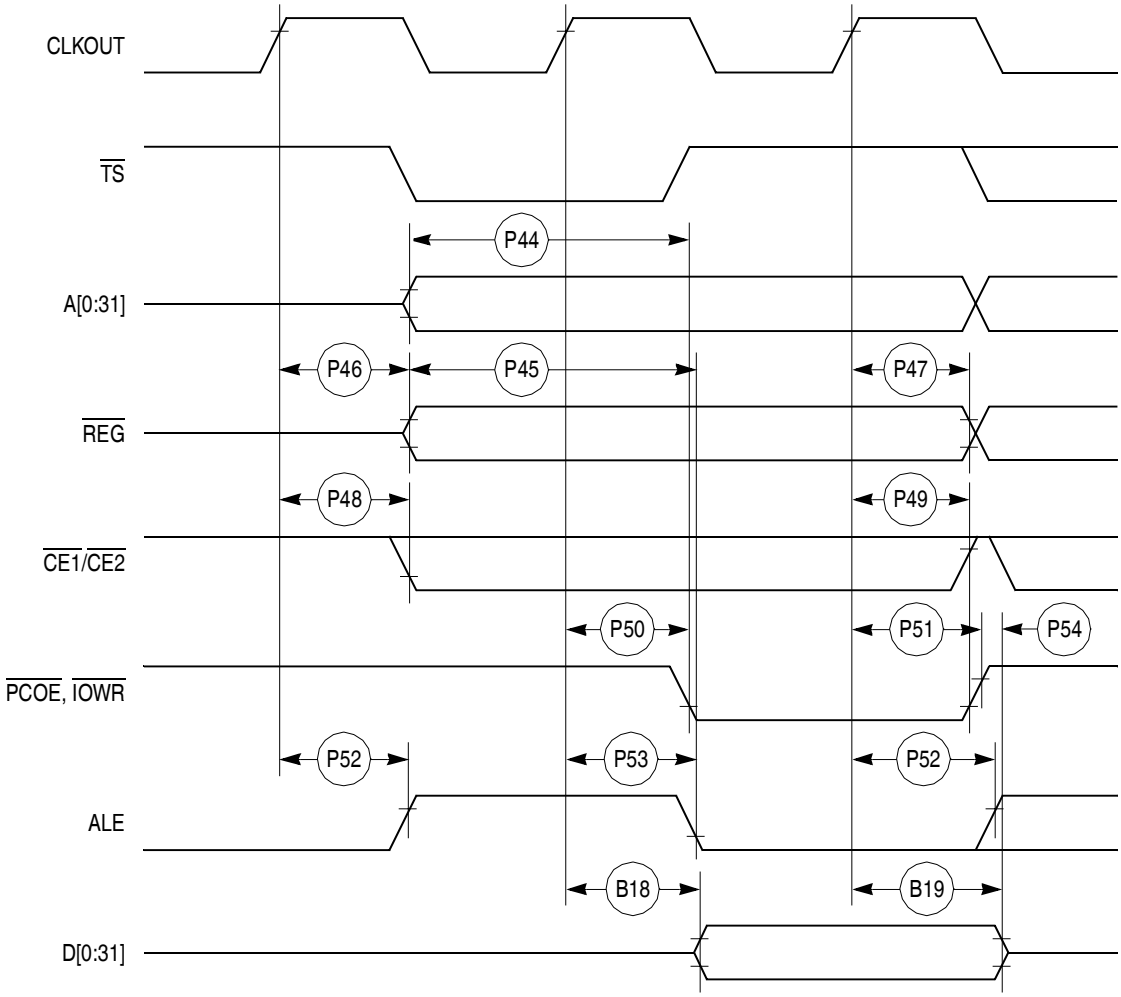


Figure 27. PCMCIA Access Cycles Timing External Bus Write

Figure 28 provides the PCMCIA $\overline{\text{WAIT}}$ signals detection timing.

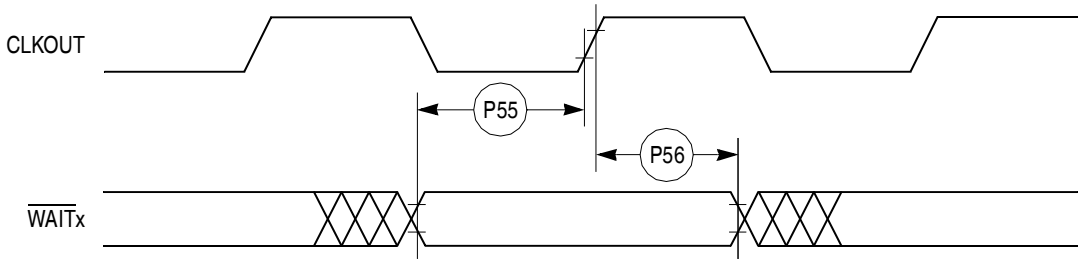


Figure 28. PCMCIA $\overline{\text{WAIT}}$ Signals Detection Timing

Table 11 shows the debug port timing for the MPC862/857T/857DSL.

Table 11. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
D61	DSCK cycle time	3 x $T_{CLOCKOUT}$		-
D62	DSCK clock pulse width	1.25 x $T_{CLOCKOUT}$		-
D63	DSCK rise and fall times	0.00	3.00	ns
D64	DSDI input data setup time	8.00		ns
D65	DSDI data hold time	5.00		ns
D66	DSCK low to DSDO data valid	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 31 provides the input timing for the debug port clock.

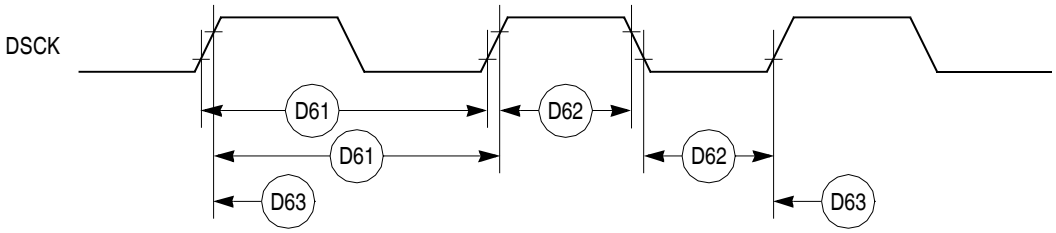


Figure 31. Debug Port Clock Input Timing

Figure 32 provides the timing for the debug port.

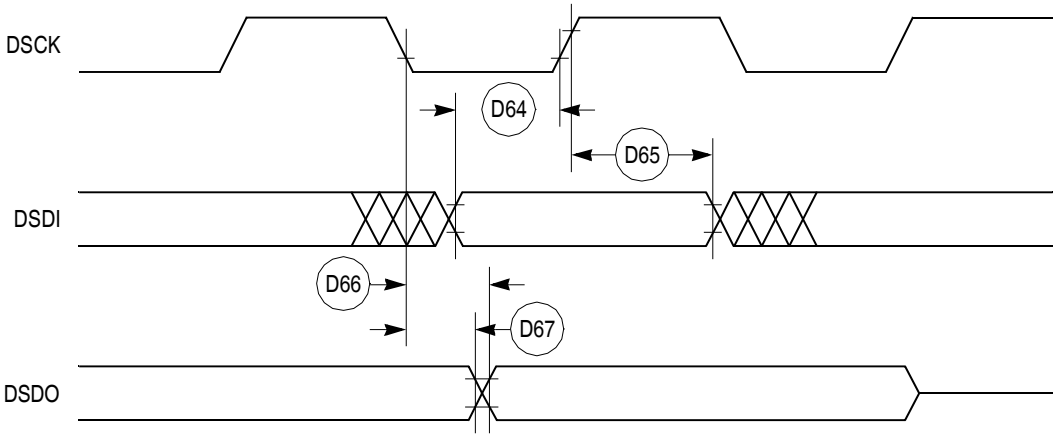


Figure 32. Debug Port Timings

11 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC862/857T/857DSL.

11.1 PIP/PIO AC Electrical Specifications

Table 14 provides the PIP/PIO AC timings as shown in Figure 40 though Figure 44.

Table 14. PIP/PIO Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
21	Data-in setup time to STBI low	0	—	ns
22	Data-in hold time to STBI high	2.5 – t3 [1]	—	clk
23	STBI pulse width	1.5	—	clk
24	STBO pulse width	1 clk – 5 ns	—	ns
25	Data-out setup time to STBO low	2	—	clk
26	Data-out hold time from STBO high	5	—	clk
27	STBI low to STBO low (Rx interlock)	—	2	clk
28	STBI low to STBO high (Tx interlock)	2	—	clk
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns

1 t3 = Specification 23

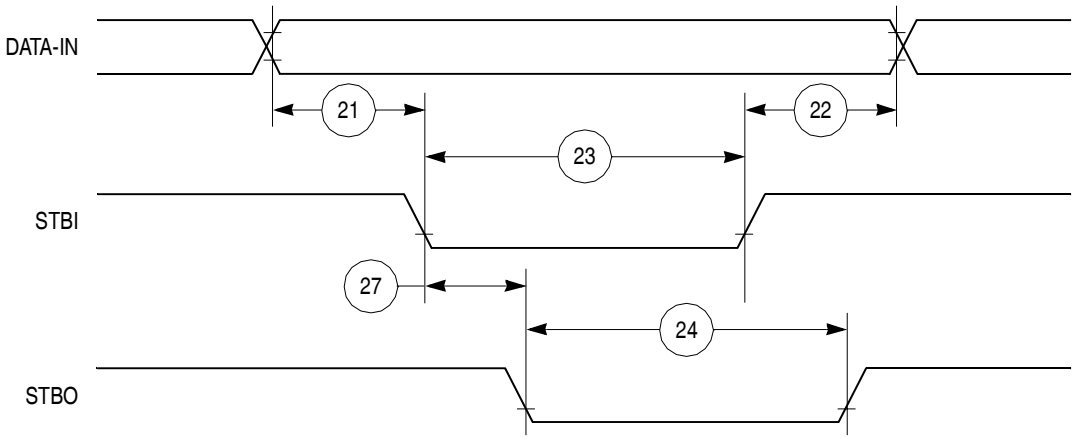


Figure 40. PIP Rx (Interlock Mode) Timing Diagram

Table 16. IDMA Controller Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

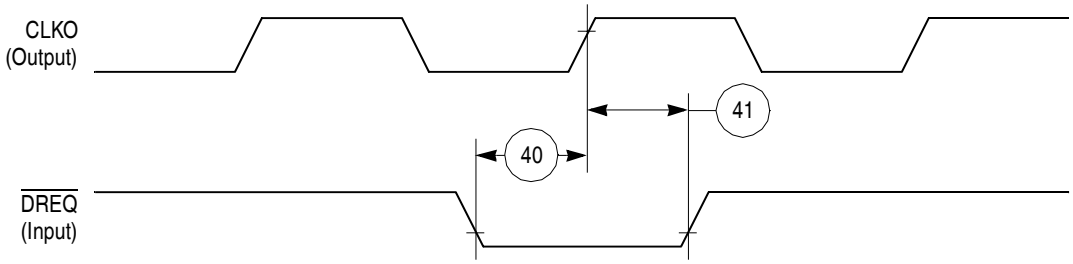


Figure 46. IDMA External Requests Timing Diagram

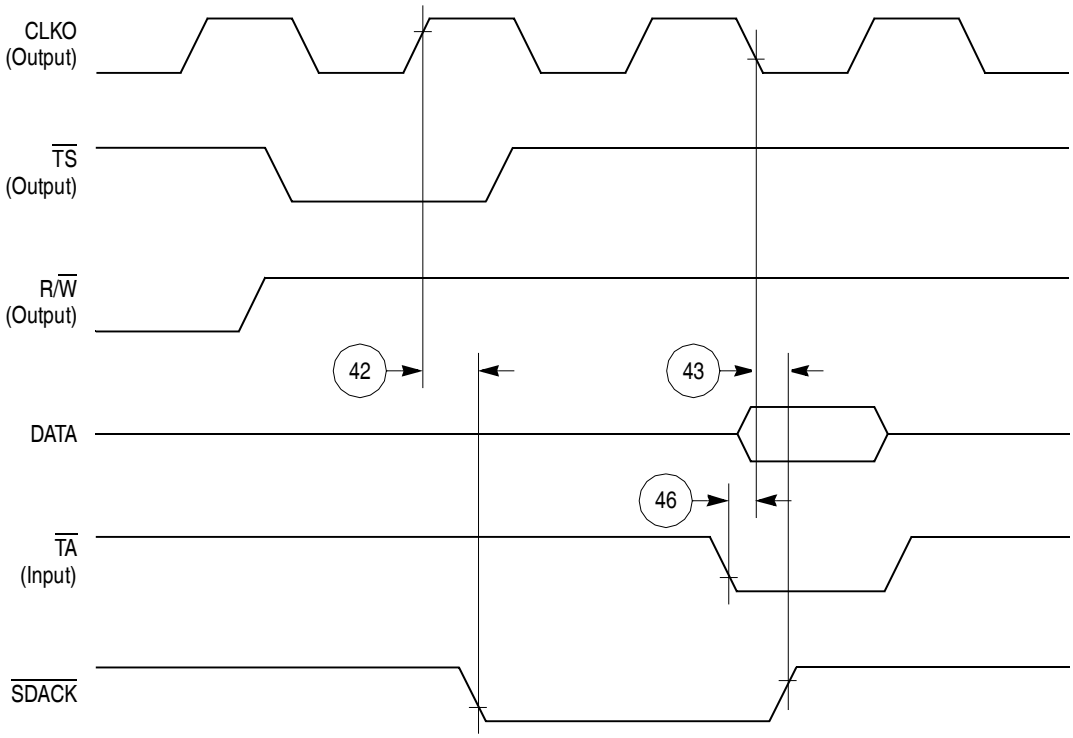


Figure 47. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Externally-Generated $\overline{\text{TA}}$

11.4 Baud Rate Generator AC Electrical Specifications

Table 17 provides the baud rate generator timings as shown in Figure 50.

Table 17. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

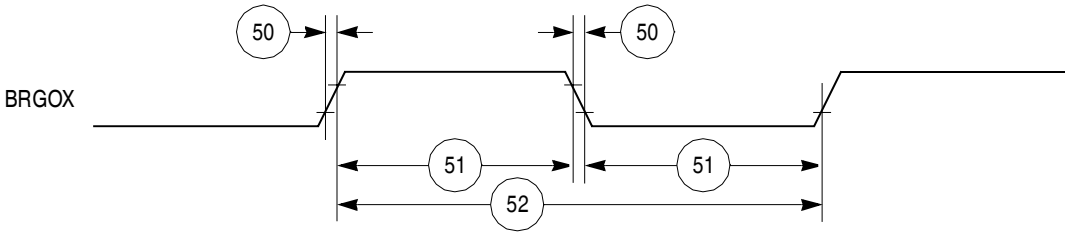


Figure 50. Baud Rate Generator Timing Diagram

11.5 Timer AC Electrical Specifications

Table 18 provides the general-purpose timer timings as shown in Figure 51.

Table 18. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1	—	clk
63	TIN/$\overline{\text{TGATE}}$ high time	2	—	clk
64	TIN/$\overline{\text{TGATE}}$ cycle time	3	—	clk
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

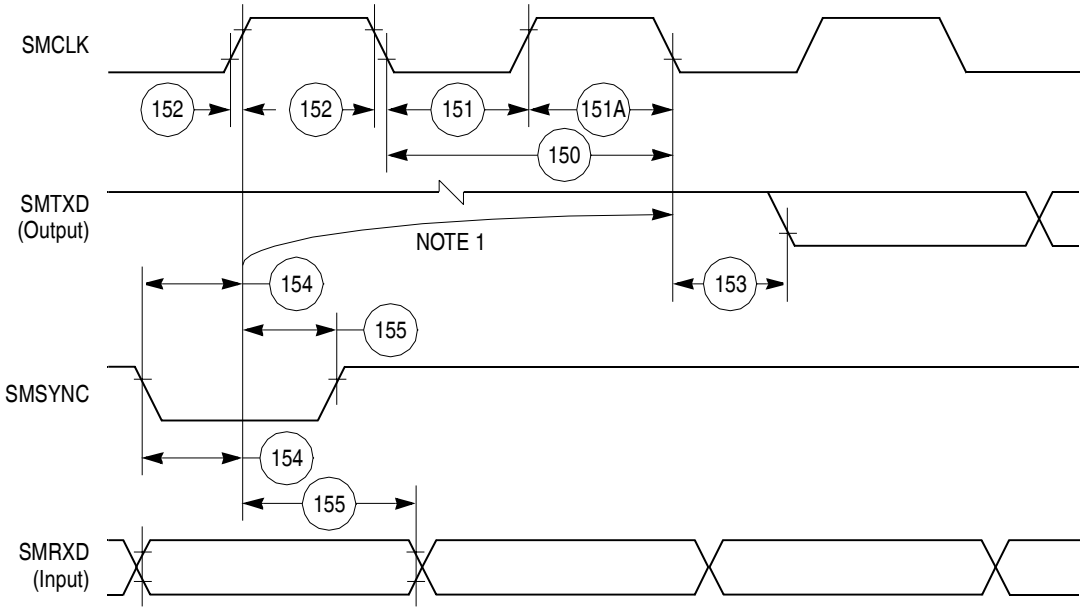
11.9 SMC Transparent AC Electrical Specifications

Table 23 provides the SMC transparent timings as shown in Figure 65.

Table 23. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period [1]	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

1 SyncCLK must be at least twice as fast as SMCLK.



NOTE:
1. This delay is equal to an integer number of character-length clocks.

Figure 65. SMC Transparent Timing Diagram

Figure 70 shows the I^{2}C bus timing.

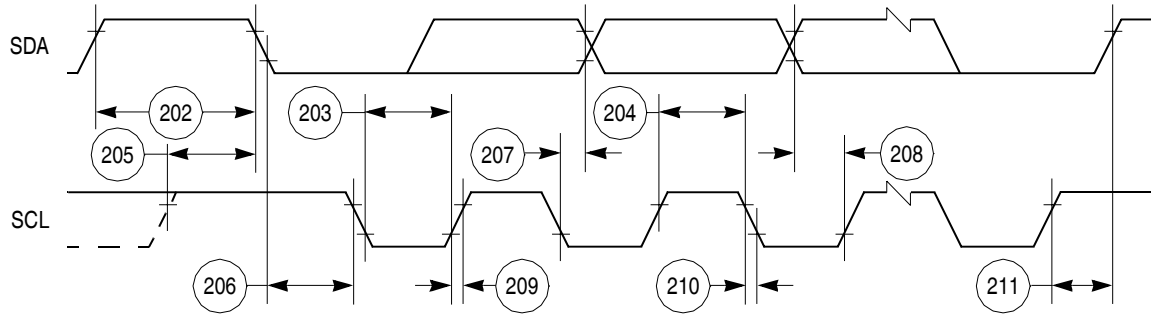


Figure 70. I^{2}C Bus Timing Diagram

12 UTOPIA AC Electrical Specifications

Table 28 shows the AC electrical specifications for the UTOPIA interface.

Table 28. UTOPIA AC Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (Internal clock option)	Output		4 ns	ns
	Duty cycle		50	50	%
	Frequency			33	MHz
U1a	UtpClk rise/fall time (external clock option)	Input		4ns	ns
	Duty cycle		40	60	%
	Frequency			33	MHz
U2	$\overline{\text{RxEnb}}$ and $\overline{\text{TxEnb}}$ active delay	Output	2 ns	16 ns	ns
U3	UTPB, SOC, Rxclav and Txclav setup time	Input	4 ns		ns
U4	UTPB, SOC, Rxclav and Txclav hold time	Input	1 ns		ns
U5	UTPB, SOC active delay (and PHREQ and PHSEL active delay in MPHY mode)	Output	2 ns	16 ns	ns

Table 33. MPC862/857T/857DSL Derivatives (continued)

Device	Number of SCCs [1]	Ethernet Support	Multi-Channel HDLC Support	ATM Support	Cache Size	
					Instruction	Data
MPC857T	One (SCC1)	10/100 Mbps	Yes	Yes	4 Kbytes	4 Kbytes
MPC857DSL	One (SCC1)	10/100 Mbps	No	Up to 4 addresses	4 Kbytes	4 Kbytes

1 Serial communications controller (SCC)

Table 34 identifies the packages and operating frequencies orderable for the MPC862/857T/857DSL derivative devices.

Table 34. MPC862/857T/857DSL Package/Frequency Orderable

Package Type	Temperature (Tj)	Frequency (MHz)	Order Number
Plastic ball grid array (ZP suffix)	0°C to 105°C	50	XPC862PZP50B XPC862TZP50B XPC857TZP50B XPC857DSLZP50B
		66	XPC862PZP66B XPC862TZP66B XPC857TZP66B XPC857DSLZP66B
		80	XPC862PZP80B XPC862TZP80B XPC857TZP80B
		100	XPC862PZP100B XPC862TZP100B XPC857TZP100B
Plastic ball grid array (CZP suffix)	-40°C to 115°C	66 [1]	XPC862PCZP66B XPC857TCZP66B

1 Additional extended temperature devices can be made available at 50MHz, 66MHz, and 80MHz

14.1 .Pin Assignments

Figure 77 shows the top view pinout of the PBGA package. For additional information, see the *MPC862 PowerQUICC Family User s Manual*.

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
$\overline{BR}$	G4	Bidirectional
$\overline{BG}$	E2	Bidirectional
$\overline{BB}$	E1	Bidirectional Active Pull-up
FRZ $\overline{IRQ6}$	G3	Bidirectional
$\overline{IRQ0}$	V14	Input
$\overline{IRQ1}$	U14	Input
M_TX_CLK $\overline{IRQ7}$	W15	Input
$\overline{CS}$[0:5]	C3, A2, D4, E4, A4, B4	Output
$\overline{CS6}$ $\overline{CE1\_B}$	D5	Output
$\overline{CS7}$ $\overline{CE2\_B}$	C4	Output
$\overline{WE0}$ $\overline{BS\_B0}$ $\overline{IORD}$	C7	Output
$\overline{WE1}$ $\overline{BS\_B1}$ $\overline{IOWR}$	A6	Output
$\overline{WE2}$ $\overline{BS\_B2}$ $\overline{PCOE}$	B6	Output
$\overline{WE3}$ $\overline{BS\_B3}$ $\overline{PCWE}$	A5	Output
$\overline{BS\_A}$[0:3]	D8, C8, A7, B8	Output
$\overline{GPL\_A0}$ $\overline{GPL\_B0}$	D7	Output
$\overline{OE}$ $\overline{GPL\_A1}$ $\overline{GPL\_B1}$	C6	Output
$\overline{GPL\_A}$[2:3] $\overline{GPL\_B}$[2:3] $\overline{CS}$[2–3]	B5, C5	Output
UPWAITA $\overline{GPL\_A4}$	C1	Bidirectional
UPWAITB $\overline{GPL\_B4}$	B1	Bidirectional

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
IP_A6 UTPB_Split6[2] MII-TXERR	T6	Input
IP_A7 UTPB_Split7[2] MII-RXDV	T3	Input
ALE_B DSCK/AT1	J1	Bidirectional Three-state
IP_B[0:1] IWP[0:1] VFLS[0:1]	H2, J3	Bidirectional
IP_B2 IOIS16_B AT2	J2	Bidirectional Three-state
IP_B3 IWP2 VF2	G1	Bidirectional
IP_B4 LWP0 VF0	G2	Bidirectional
IP_B5 LWP1 VF1	J4	Bidirectional
IP_B6 DSDI AT0	K3	Bidirectional Three-state
IP_B7 PTR AT3	H1	Bidirectional Three-state
OP0 MII-TXD0 UtpClk_Split[2]	L4	Bidirectional
OP1	L2	Output
OP2 MODCK1 STS	L1	Bidirectional
OP3 MODCK2 DSDO	M4	Bidirectional
BADDR30 REG	K4	Output
BADDR[28:29]	M3, M2	Output
AS	L3	Input

15 Document Revision History

Table 36 lists significant changes between revisions of this document.

Table 36. Document Revision History

Rev. No.	Date	Substantive Changes
0	2001	Initial revision
0.1	9/2001	Change extended temperature from 95 to 105
0.2	11/2001	Revised for new template, changed Table 7 B23 max value @ 66 MHz from 2 ns to 8 ns.
0.3	4/2002	• Timing modified and equations added, for Rev. A and B devices. • Modified power numbers and temperature ranges. Added ESAR UTOPIA timing.
1.0	9/2002	• Specification changed to include the MPC857T and MPC857DSL. • Changed maximum operating frequency from 80 MHz to 100 MHz. • Removed MPC862DP, DT, and SR derivatives and part numbers. • Corrected power dissipation numbers. • Changed UTOPIA maximum frequency from 50 MHz to 33 MHz. • Changed part number ordering information to Rev. B devices only. • To maximum ratings for temperature, added frequency ranges.
1.1	5/2003	Changed SPI Master Timing Specs. 162 and 164
1.2	8/2003	• Changed B28a through B28d and B29b to show that TRLX can be 0 or 1. • Non-technical reformatting
2.0	11/2004	• Added a table footnote to Table 5 DC Electrical Specifications about meeting the VIL Max of the I2C Standard. • Updated document template.
3.0	2/2006	• Changed Tj from 95C to 105C in table 34