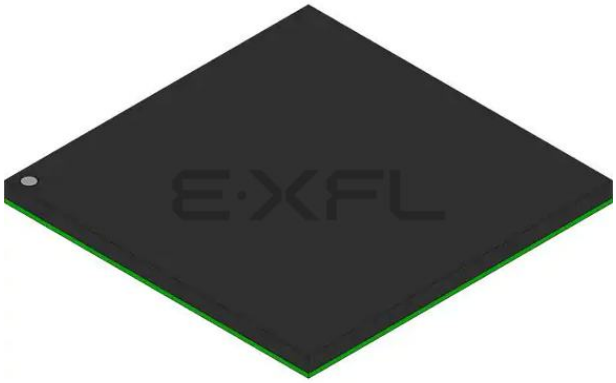

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 115°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc862pczq66b

  - Sleep—All units disabled except RTC, PIT, time base, and decrementer with PLL active for fast wake up
  - Deep sleep—All units disabled including PLL except RTC, PIT, time base, and decrementer.
  - Power down mode— All units powered down except PLL, RTC, PIT, time base and decrementer
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally
- 3.3 V operation with 5-V TTL compatibility except EXTAL and EXTCLK
- 357-pin plastic ball grid array (PBGA) package
- Operation up to 100MHz

The MPC862/857T/857DSL is comprised of three modules that each use the 32-bit internal bus: the MPC8xx core, the system integration unit (SIU), and the communication processor module (CPM). The MPC862P/862T block diagram is shown in Figure 1. The MPC857T/857DSL block diagram is shown in Figure 2.

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC862/857T/857DSL.

Table 3. MPC862/857T/857DSL Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction to ambient [1]	Natural Convection	Single layer board (1s)	$R_{\theta JA}$ [2]	37	°C/W
		Four layer board (2s2p)	$R_{\theta JMA}$ [3]	23	
	Air flow (200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$ [3]	30	
		Four layer board (2s2p)	$R_{\theta JMA}$ [3]	19	
Junction to board [4]			$R_{\theta JB}$	13	
Junction to case [5]			$R_{\theta JC}$	6	
Junction to package top [6]	Natural Convection		Ψ_{JT}	2	
	Air flow (200 ft/min)		Ψ_{JT}	2	

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5 Power Dissipation

Table 4 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice bus speed.

Table 4. Power Dissipation (P_D)

Die Revision	Frequency	Typical [1]	Maximum [2]	Unit
0 (1:1 Mode)	50 MHz	656	735	mW
	66 MHz	TBD	TBD	mW
A.1, B.0 (1:1 Mode)	50 MHz	630	760	mW
	66 MHz	890	1000	mW

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B30c	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1 (MIN = 0.375 x B1 - 3.00)	8.40	—	6.40	—	4.50	—	2.70	—	ns
B30d	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 X B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid- as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 x B1 + 6.6)	9.40	18.00	7.60	16.00	13.30	14.10	11.30	12.30	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns

Figure 6 provides the timing for the synchronous output signals.

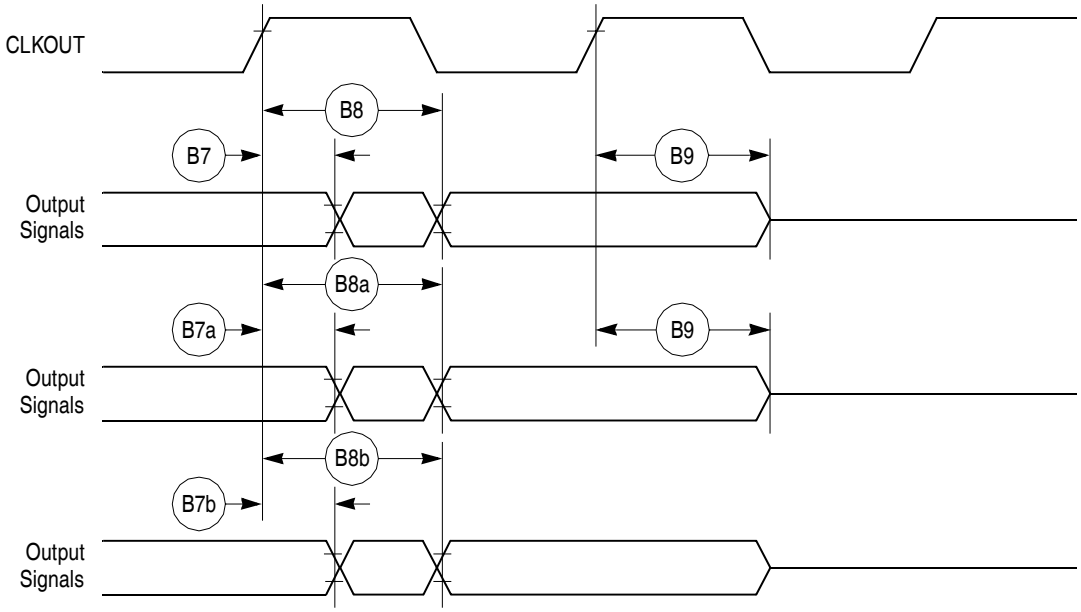


Figure 6. Synchronous Output Signals Timing

Figure 7 provides the timing for the synchronous active pull-up and open-drain output signals.

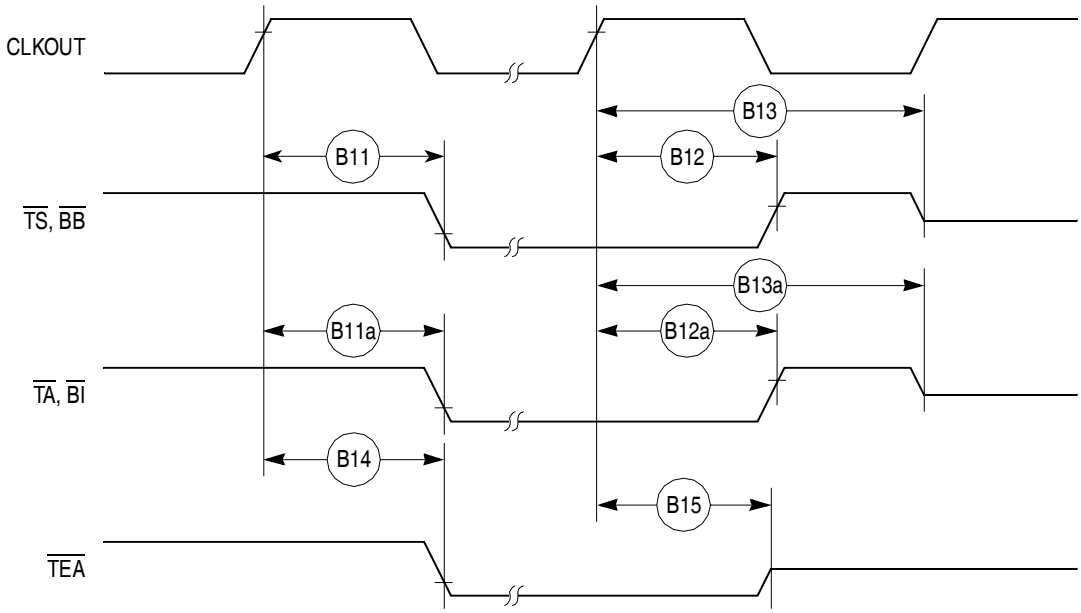


Figure 7. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

Figure 10 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

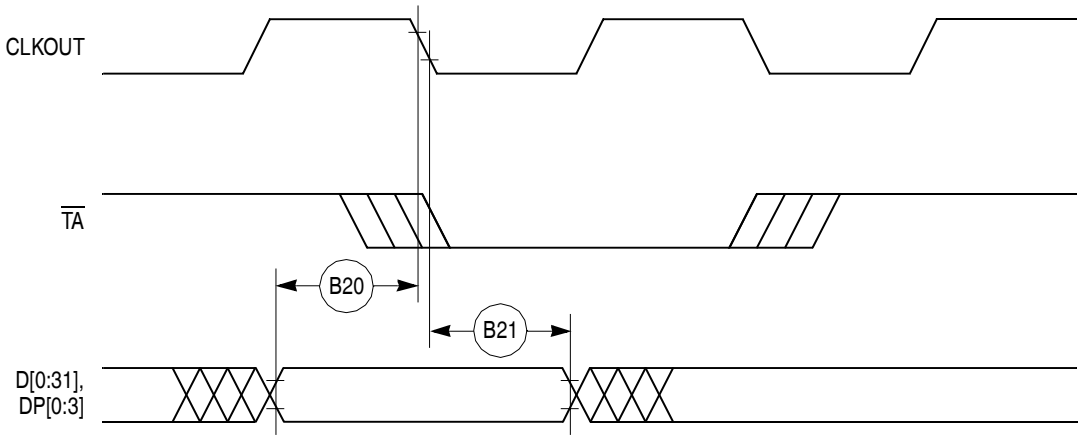


Figure 10. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 11 through Figure 14 provide the timing for the external bus read controlled by various GPCM factors.

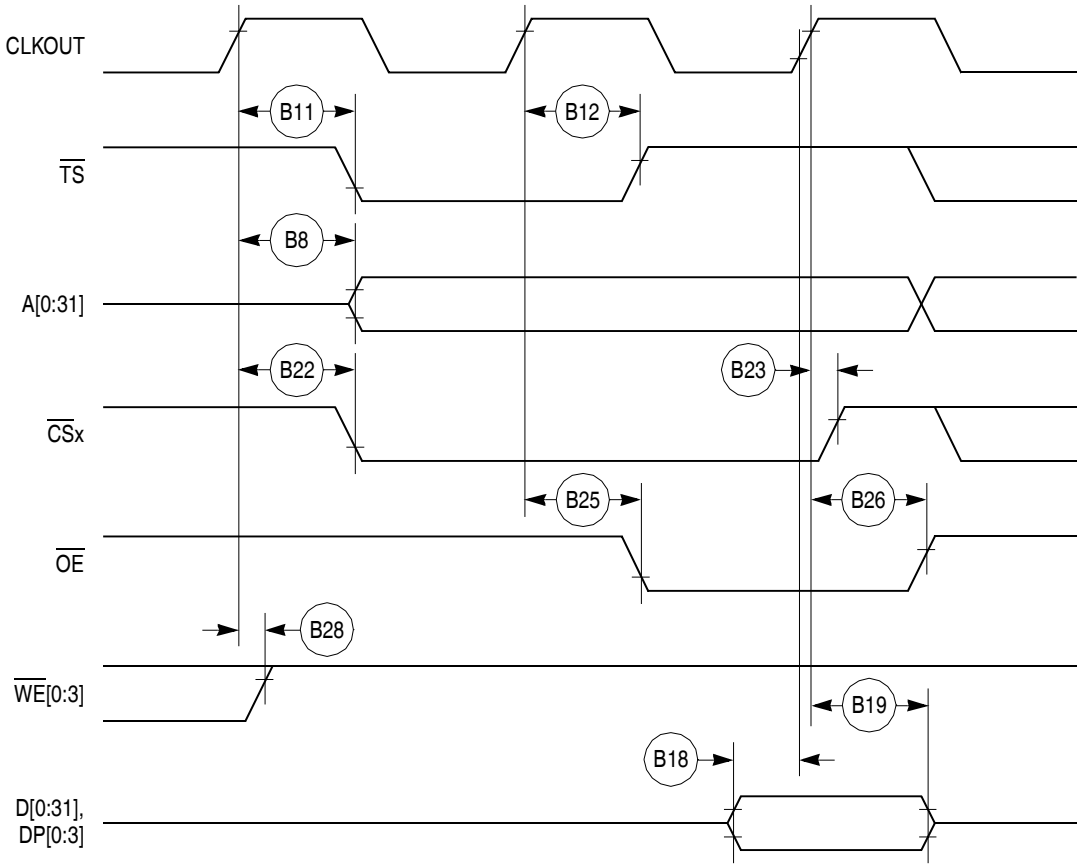


Figure 11. External Bus Read Timing (GPCM Controlled—ACS = 00)

Table 8 provides interrupt timing for the MPC862/857T/857DSL.

Table 8. Interrupt Timing

Num	Characteristic [1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{IRQ}$x valid to CLKOUT rising edge (set up time)	6.00		ns
I40	$\overline{IRQ}$x hold time after CLKOUT	2.00		ns
I41	$\overline{IRQ}$x pulse width low	3.00		ns
I42	$\overline{IRQ}$x pulse width high	3.00		ns
I43	$\overline{IRQ}$x edge-to-edge time	$4xT_{CLOCKOUT}$		—

1 The timings I39 and I40 describe the testing conditions under which the $\overline{IRQ}$ lines are tested when being defined as level sensitive. The $\overline{IRQ}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{IRQ}$ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC862/857T/857DSL is able to support.

Figure 24 provides the interrupt detection timing for the external level-sensitive lines.

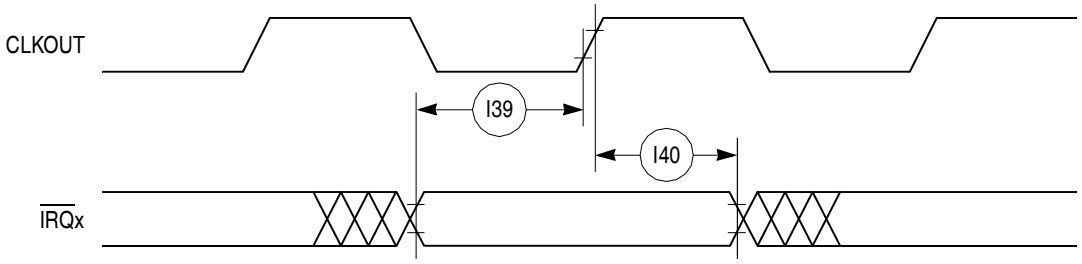


Figure 24. Interrupt Detection Timing for External Level Sensitive Lines

Figure 25 provides the interrupt detection timing for the external edge-sensitive lines.

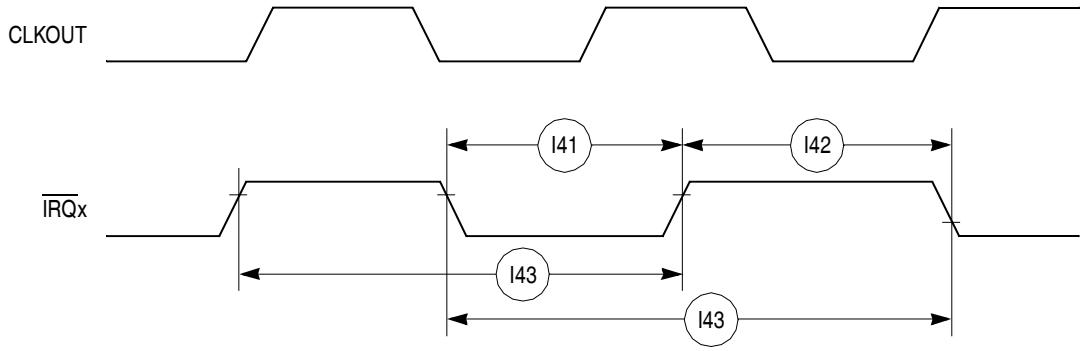


Figure 25. Interrupt Detection Timing for External Edge Sensitive Lines

Table 9 shows the PCMCIA timing for the MPC862/857T/857DSL.

Table 9. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA Strobe asserted. [1] (MIN = 0.75 x B1 - 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation.[1] (MIN = 1.00 x B1 - 2.00)	28.30	—	23.00	—	18.00	—	13.20	—	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P47	CLKOUT to $\overline{\text{REG}}$ Invalid. (MIN = 0.25 x B1 + 1.00)	8.60	—	7.30	—	6.00	—	4.80	—	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted. (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated. (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time. (MAX = 0.00 x B1 + 11.00)	—	11.00	—	11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time. (MAX = 0.00 x B1 + 11.00)	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time (MAX = 0.25 x B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
P53	CLKOUT to ALE negate time (MAX = 0.25 x B1 + 8.00)	—	15.60	—	14.30	—	13.00	—	11.80	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid.[1] (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
P55	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge.[1] (MIN = 0.00 x B1 + 8.00)	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid.[1] (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns

[1] PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAITx}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITx}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the *MPC862 PowerQUICC User s Manual*.

Figure 33 shows the reset timing for the data bus configuration.

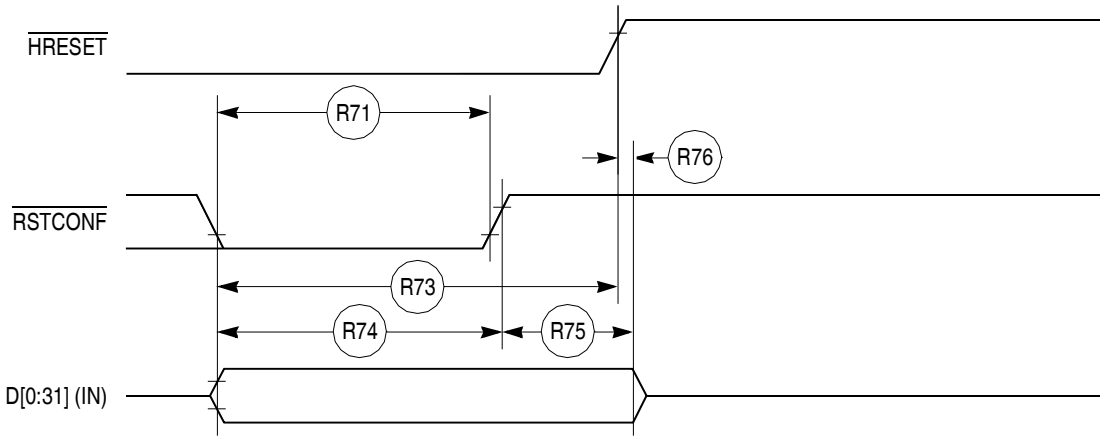


Figure 33. Reset Timing—Configuration from Data Bus

Figure 34 provides the reset timing for the data bus weak drive during configuration.

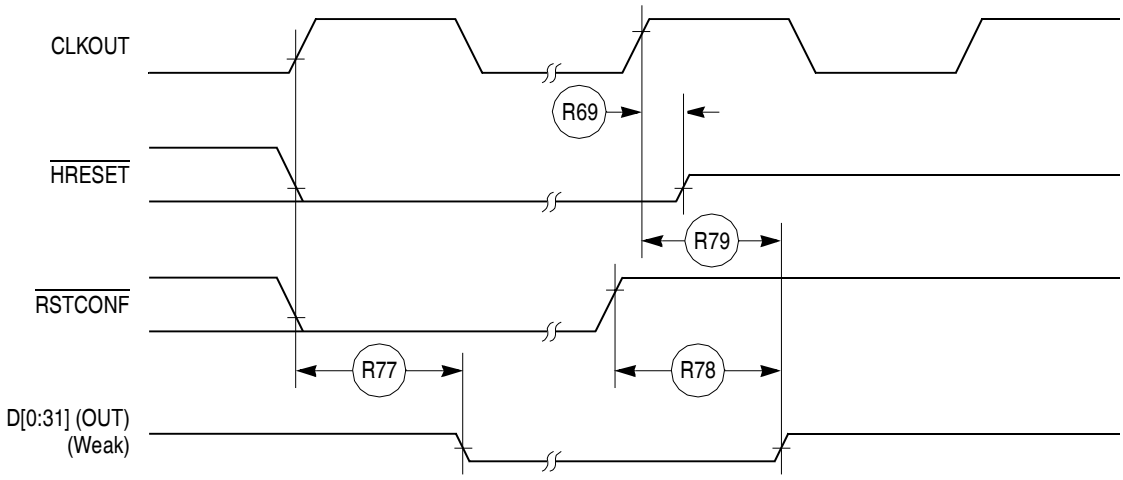


Figure 34. Reset Timing—Data Bus Weak Drive during Configuration

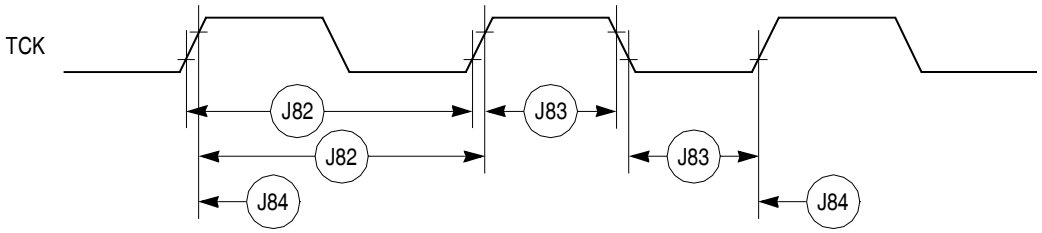


Figure 36. JTAG Test Clock Input Timing

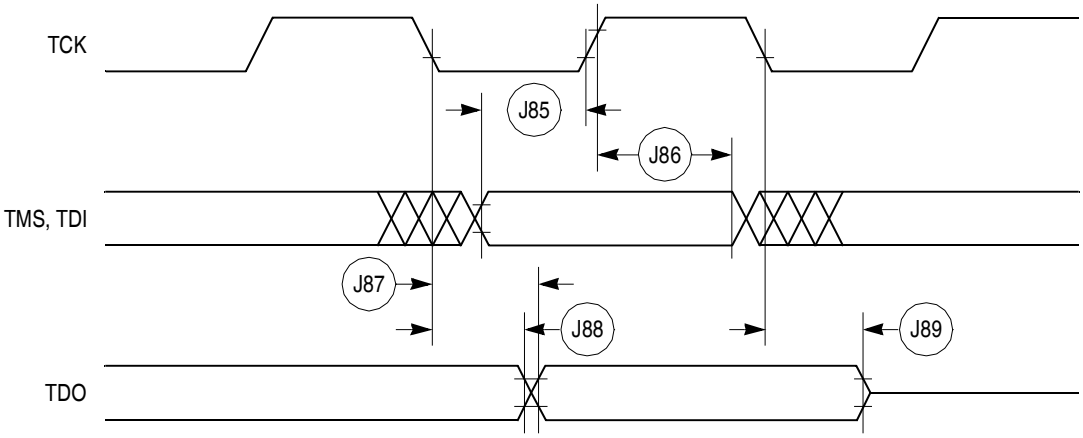


Figure 37. JTAG Test Access Port Timing Diagram

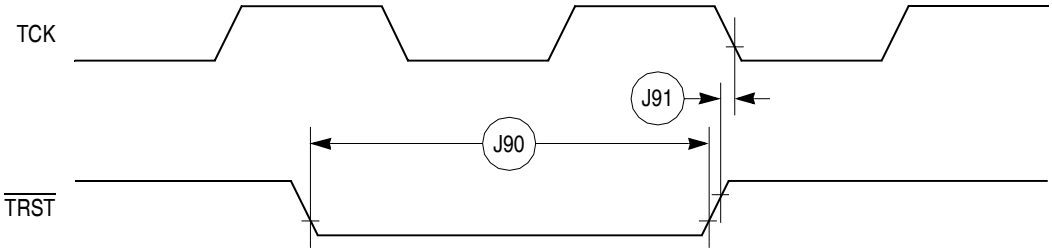


Figure 38. JTAG $\overline{\text{TRST}}$ Timing Diagram

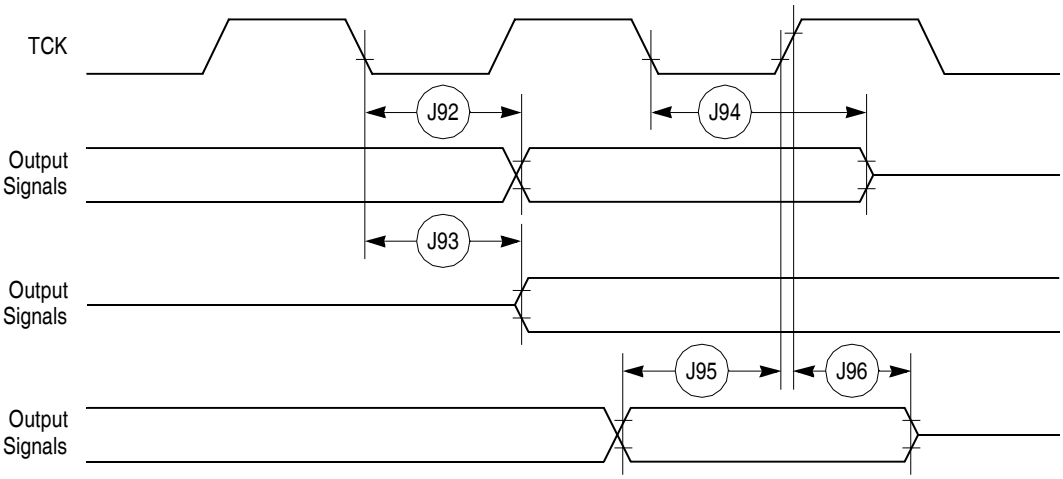


Figure 39. Boundary Scan (JTAG) Timing Diagram

Table 16. IDMA Controller Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

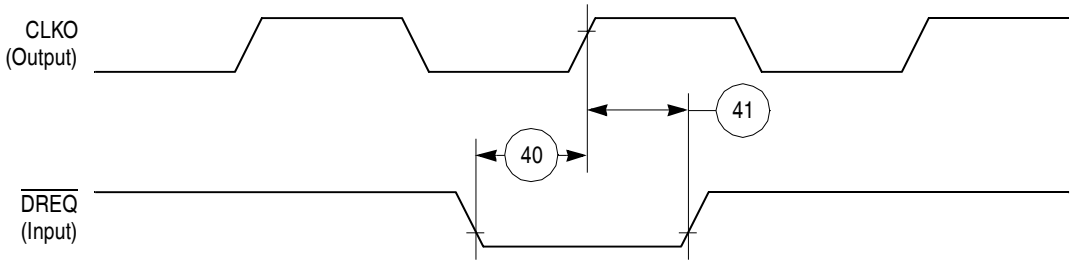


Figure 46. IDMA External Requests Timing Diagram

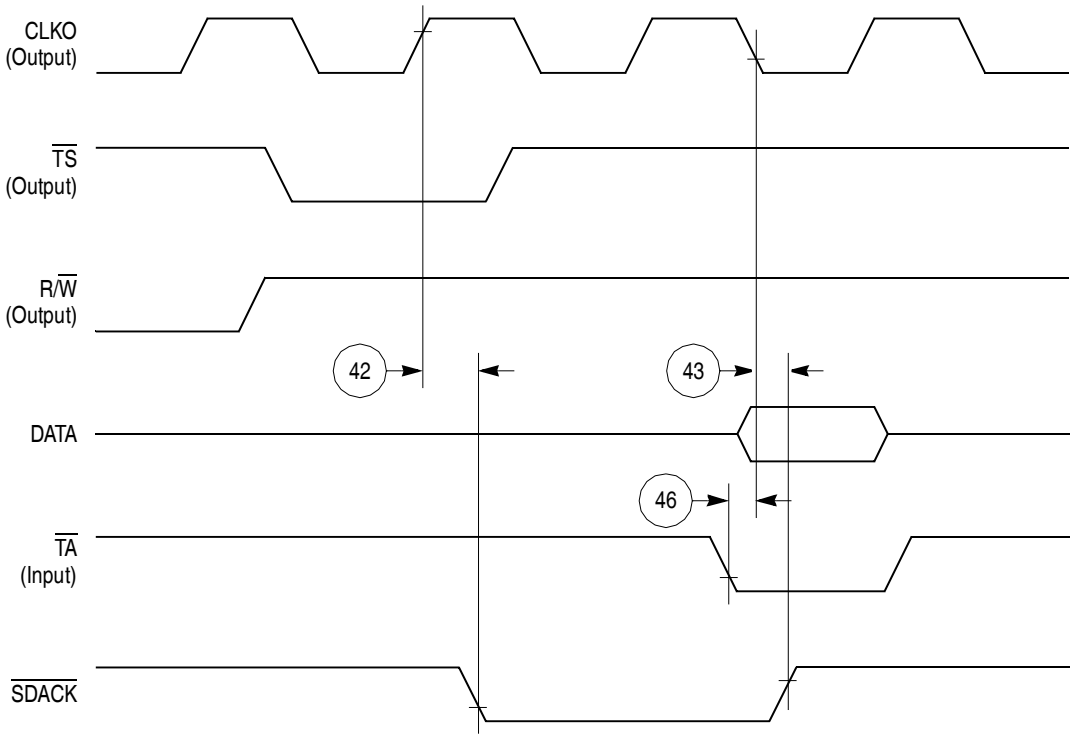


Figure 47. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Externally-Generated $\overline{\text{TA}}$

Table 19. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
83a	L1RCLK, L1TCLK width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4]	1.00	—	L1TCLK
86	L1GR setup time[2]	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

1 The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

2 These specs are valid for IDL mode only.

3 Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

4 These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.

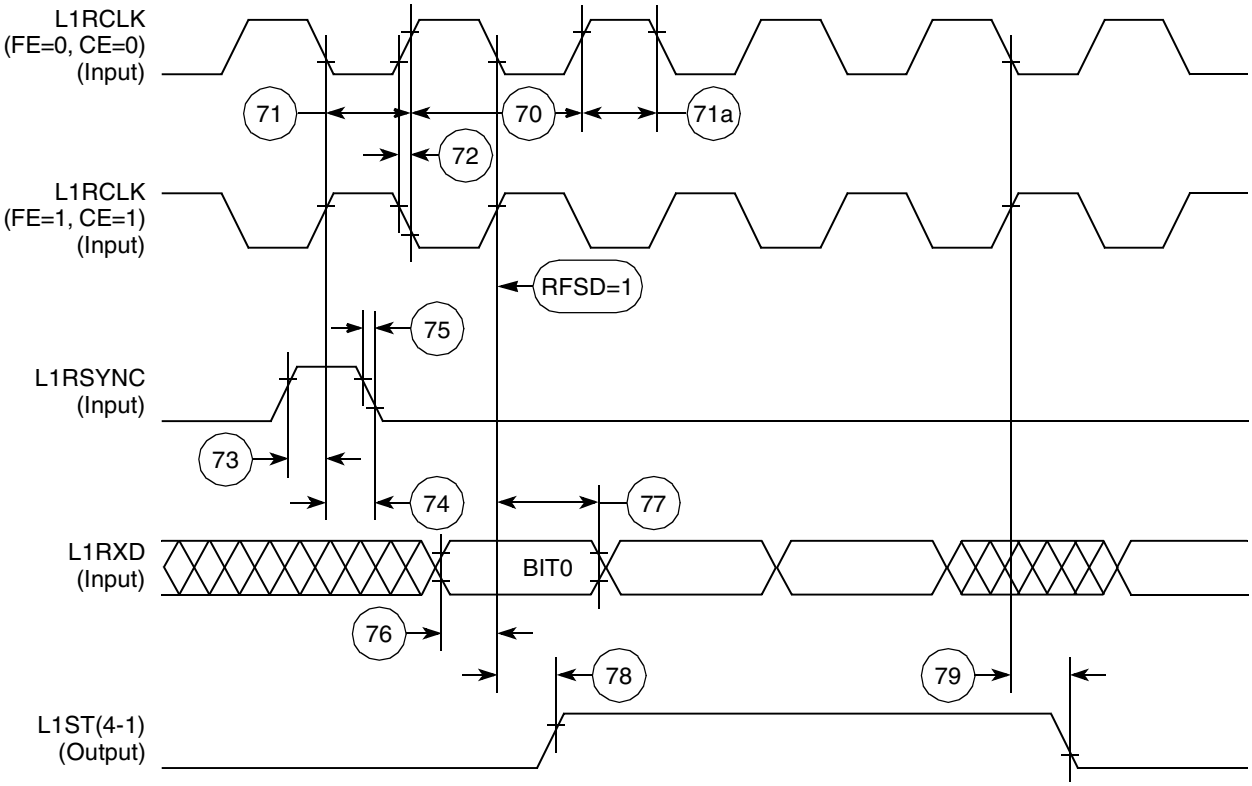


Figure 52. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

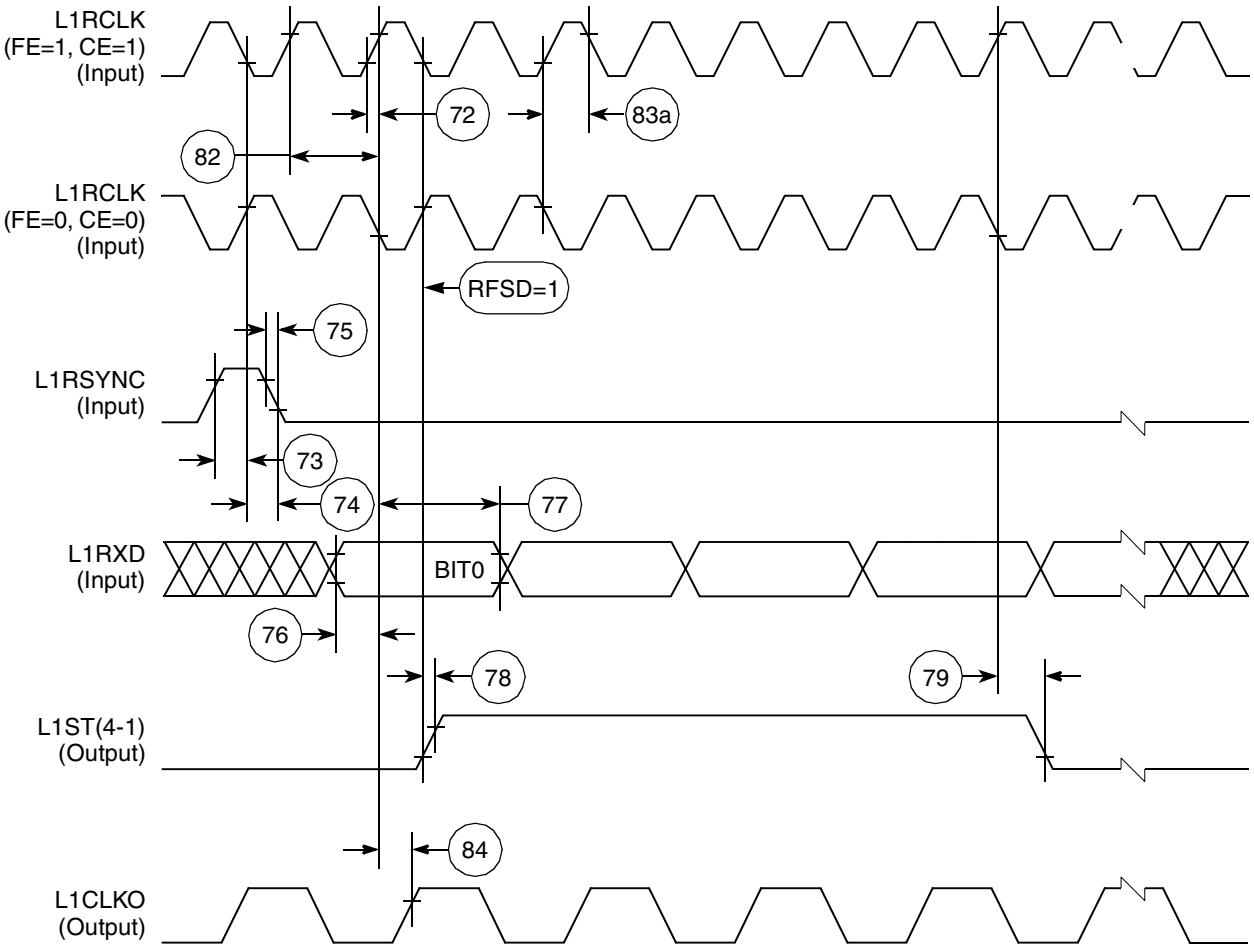


Figure 53. SI Receive Timing with Double-Speed Clocking (DSC = 1)

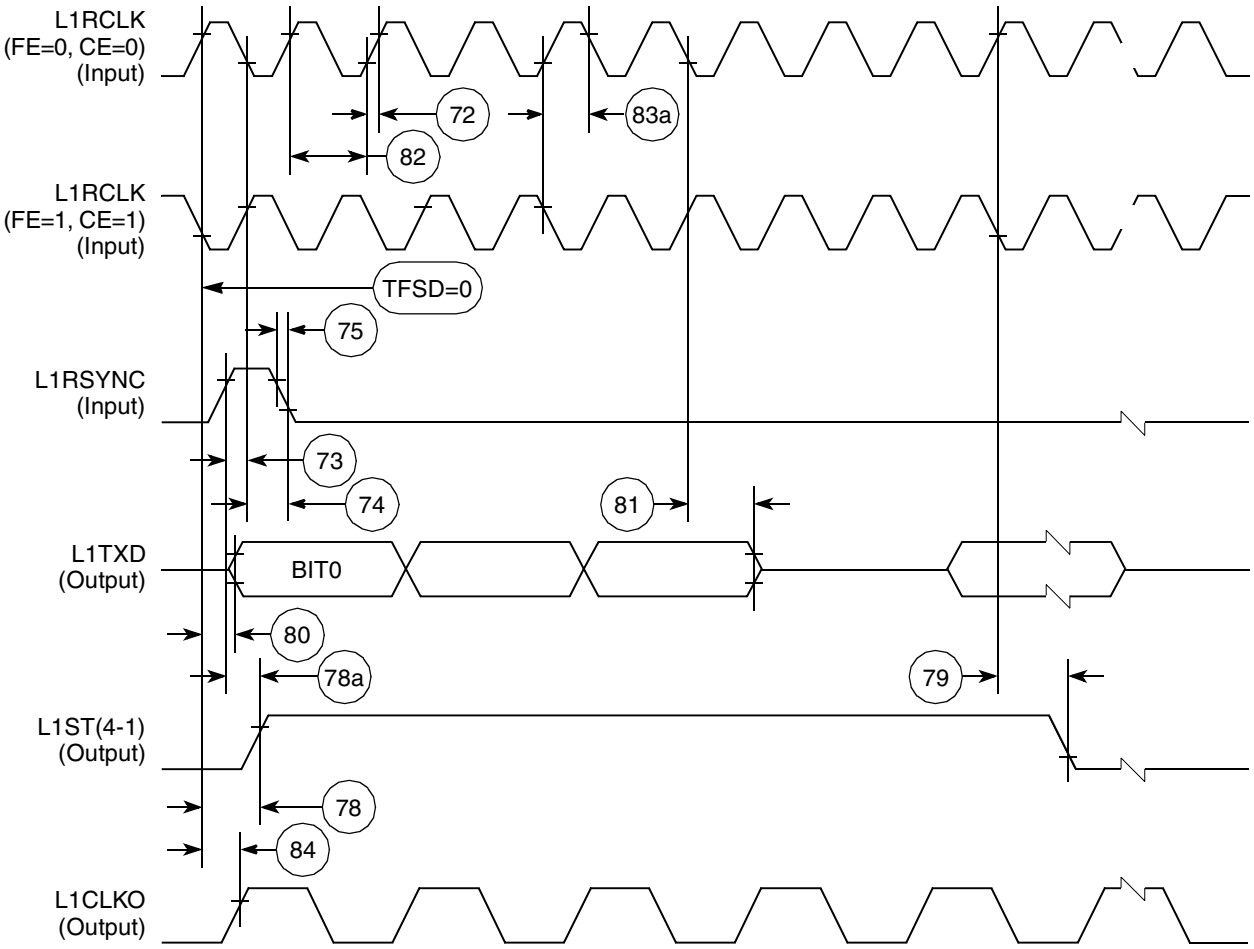


Figure 55. SI Transmit Timing with Double Speed Clocking (DSC = 1)

11.7 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

Table 20. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 width high [1]	1/SYNCCLK	—	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK +5	—	ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	—	ns
107	RXD1 hold time from RCLK1 rising edge [2]	5.00	—	ns
108	$\overline{\text{CD1}}$ setup Time to RCLK1 rising edge	5.00	—	ns

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 frequency [1]	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge [2]	0.00	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	40.00	—	ns

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 3/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

Table 22. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns
135	$\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted [2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2/1.

2 $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

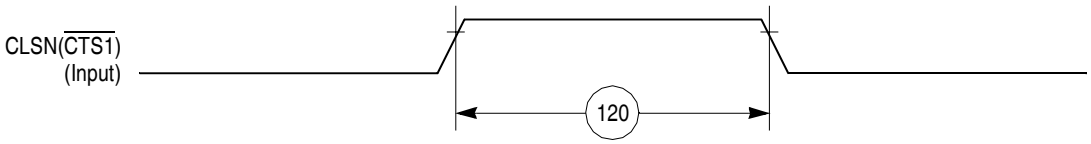


Figure 60. Ethernet Collision Timing Diagram

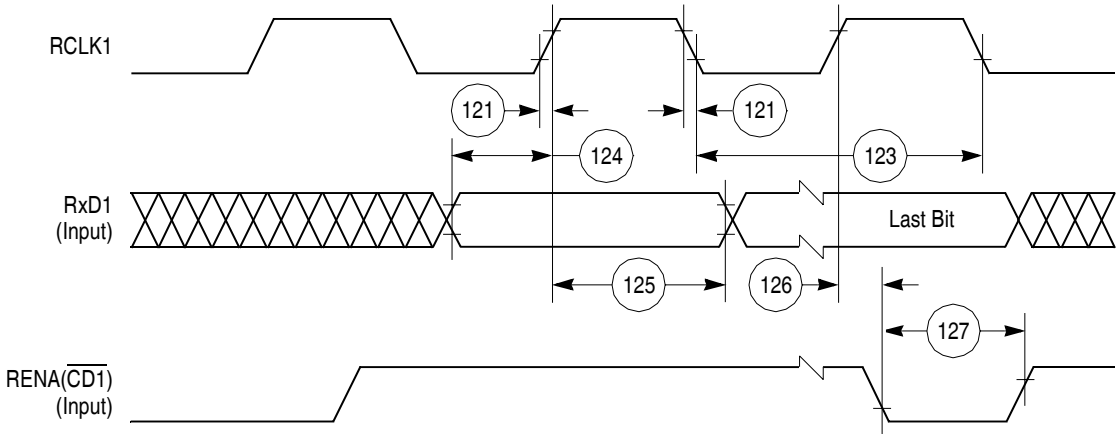


Figure 61. Ethernet Receive Timing Diagram

11.12 I²C AC Electrical Specifications

Table 26 provides the I²C (SCL < 100 KHz) timings.

Table 26. I²C Timing (SCL < 100 KHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master) [1]	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	µs
203	Low period of SCL	4.7	—	µs
204	High period of SCL	4.0	—	µs
205	Start condition setup time	4.7	—	µs
206	Start condition hold time	4.0	—	µs
207	Data hold time	0	—	µs
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	µs
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	µs

1 SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) * pre_scaler * 2).
The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 27 provides the I²C (SCL > 100 kHz) timings.

Table 27. I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) [1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	—	1/(2.2 * fSCL)	—	s
203	Low period of SCL	—	1/(2.2 * fSCL)	—	s
204	High period of SCL	—	1/(2.2 * fSCL)	—	s
205	Start condition setup time	—	1/(2.2 * fSCL)	—	s
206	Start condition hold time	—	1/(2.2 * fSCL)	—	s
207	Data hold time	—	0	—	s
208	Data setup time	—	1/(40 * fSCL)	—	s
209	SDL/SCL rise time	—	—	1/(10 * fSCL)	s
210	SDL/SCL fall time	—	—	1/(33 * fSCL)	s
211	Stop condition setup time	—	1/2(2.2 * fSCL)	—	s

1 SCL frequency is given by SCL = BrgClk_frequency / ((BRG register + 3) * pre_scaler * 2).
The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 70 shows the I^{2}C bus timing.

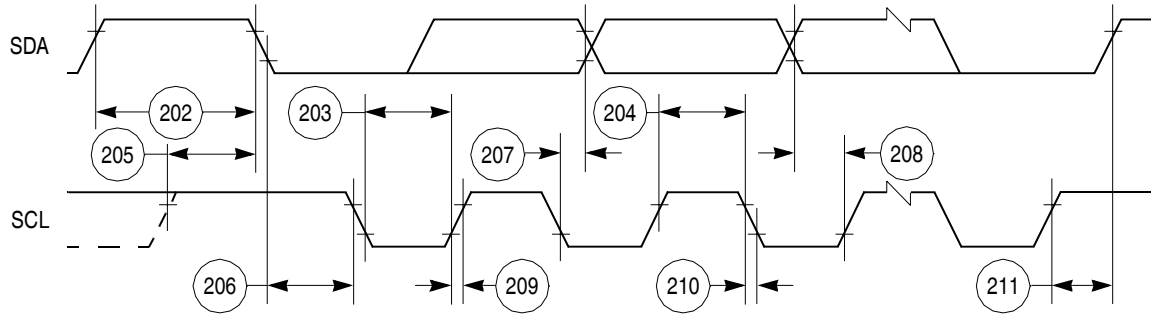


Figure 70. I^{2}C Bus Timing Diagram

12 UTOPIA AC Electrical Specifications

Table 28 shows the AC electrical specifications for the UTOPIA interface.

Table 28. UTOPIA AC Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (Internal clock option)	Output		4 ns	ns
	Duty cycle		50	50	%
	Frequency			33	MHz
U1a	UtpClk rise/fall time (external clock option)	Input		4ns	ns
	Duty cycle		40	60	%
	Frequency			33	MHz
U2	$\overline{\text{RxEnb}}$ and $\overline{\text{TxEnb}}$ active delay	Output	2 ns	16 ns	ns
U3	UTPB, SOC, Rxclav and Txclav setup time	Input	4 ns		ns
U4	UTPB, SOC, Rxclav and Txclav hold time	Input	1 ns		ns
U5	UTPB, SOC active delay (and PHREQ and PHSEL active delay in MPHY mode)	Output	2 ns	16 ns	ns

Figure 71 shows signal timings during UTOPIA receive operations.

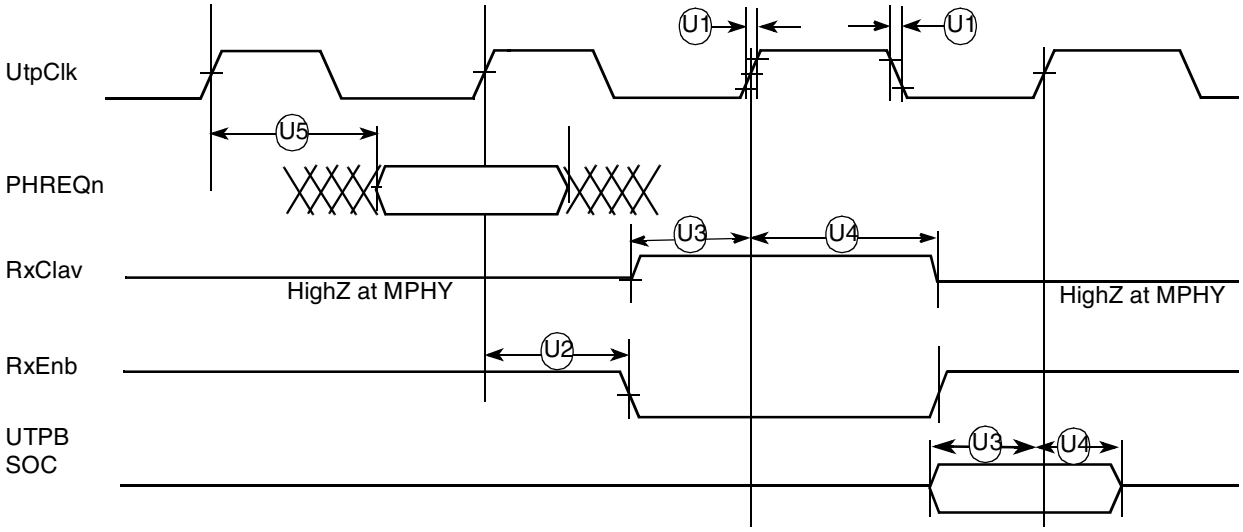


Figure 71. UTOPIA Receive Timing

Figure 72 shows signal timings during UTOPIA transmit operations.

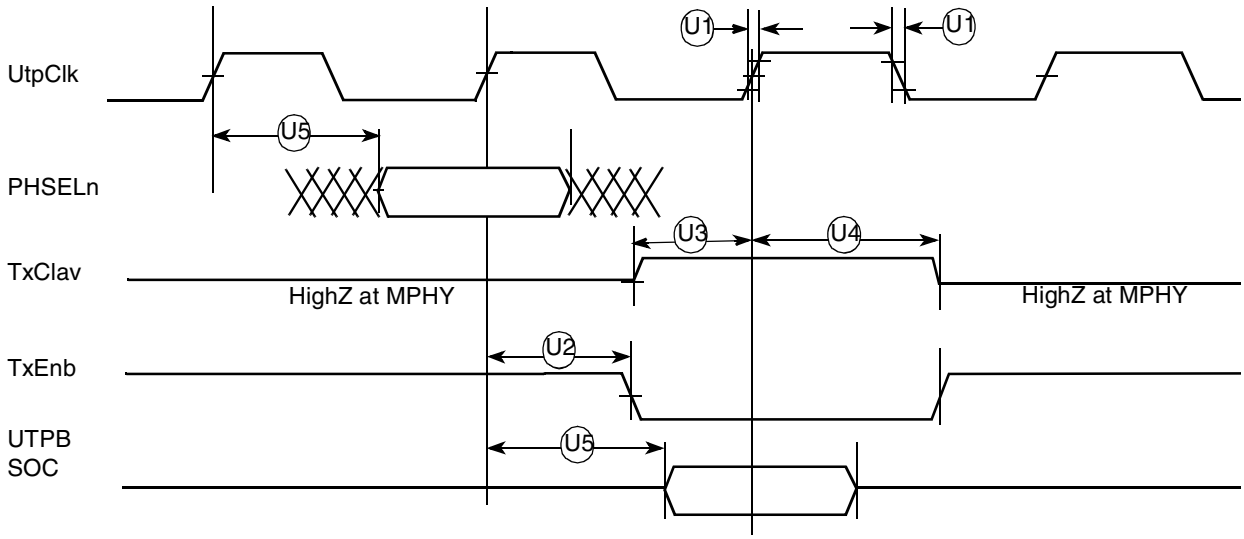


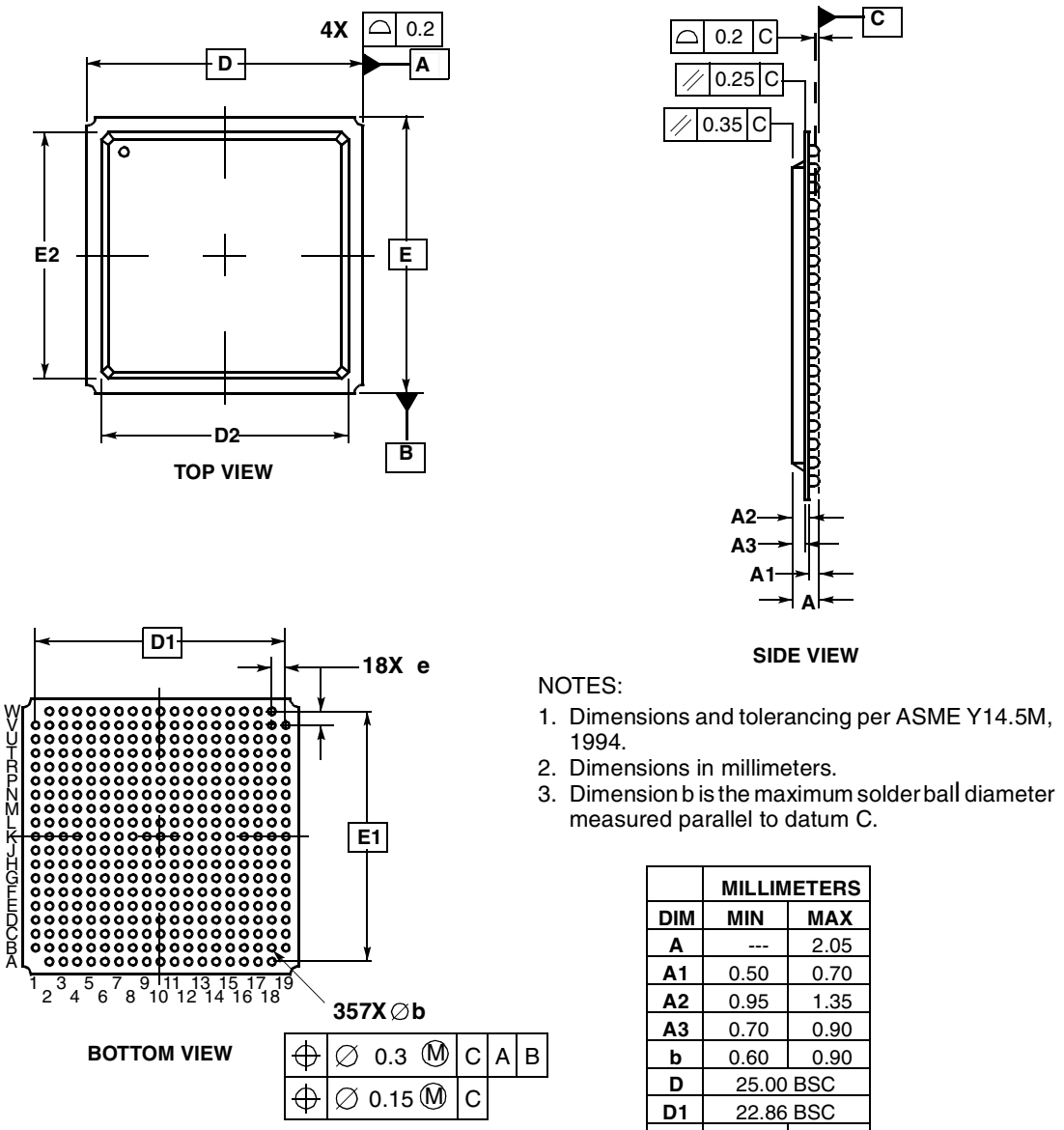
Figure 72. UTOPIA Transmit Timing

13 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Furthermore, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
$\overline{BR}$	G4	Bidirectional
$\overline{BG}$	E2	Bidirectional
$\overline{BB}$	E1	Bidirectional Active Pull-up
FRZ $\overline{IRQ6}$	G3	Bidirectional
$\overline{IRQ0}$	V14	Input
$\overline{IRQ1}$	U14	Input
M_TX_CLK $\overline{IRQ7}$	W15	Input
$\overline{CS}$[0:5]	C3, A2, D4, E4, A4, B4	Output
$\overline{CS6}$ $\overline{CE1\_B}$	D5	Output
$\overline{CS7}$ $\overline{CE2\_B}$	C4	Output
$\overline{WE0}$ $\overline{BS\_B0}$ $\overline{IORD}$	C7	Output
$\overline{WE1}$ $\overline{BS\_B1}$ $\overline{IOWR}$	A6	Output
$\overline{WE2}$ $\overline{BS\_B2}$ $\overline{PCOE}$	B6	Output
$\overline{WE3}$ $\overline{BS\_B3}$ $\overline{PCWE}$	A5	Output
$\overline{BS\_A}$[0:3]	D8, C8, A7, B8	Output
$\overline{GPL\_A0}$ $\overline{GPL\_B0}$	D7	Output
$\overline{OE}$ $\overline{GPL\_A1}$ $\overline{GPL\_B1}$	C6	Output
$\overline{GPL\_A}$[2:3] $\overline{GPL\_B}$[2:3] $\overline{CS}$[2–3]	B5, C5	Output
UPWAITA $\overline{GPL\_A4}$	C1	Bidirectional
UPWAITB $\overline{GPL\_B4}$	B1	Bidirectional



NOTES:
1. Dimensions and tolerancing per ASME Y14.5M, 1994.
2. Dimensions in millimeters.
3. Dimension b is the maximum solder ball diameter measured parallel to datum C.

	MILLIMETERS	
DIM	MIN	MAX
A	---	2.05
A1	0.50	0.70
A2	0.95	1.35
A3	0.70	0.90
b	0.60	0.90
D	25.00 BSC	
D1	22.86 BSC	
D2	22.40	22.60
e	1.27 BSC	
E	25.00 BSC	
E1	22.86 BSC	
E2	22.40	22.60

Case No. 1103-01

Figure 78. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package