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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 115°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc862pczq80b

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Features

- System integration unit (SIU)
 - Bus monitor
 - Software watchdog
 - Periodic interrupt timer (PIT)
 - Low-power stop mode
 - Clock synthesizer
 - Decrementer, time base, and real-time clock (RTC) from the PowerPC architecture
 - Reset controller
 - IEEE 1149.1 test access port (JTAG)
- Interrupts
 - Seven external interrupt request (IRQ) lines
 - 12 port pins with interrupt capability
 - The MPC862P and MPC862T have 23 internal interrupt sources; the MPC857T and MPC857DSL have 20 internal interrupt sources
 - Programmable priority between SCCs (MPC862P and MPC862T)
 - Programmable highest priority request
- Communications processor module (CPM)
 - RISC controller
 - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
 - Supports continuous mode transmission and reception on all serial channels
 - Up to 8-Kbytes of dual-port RAM
 - The MPC862P and MPC862T have 16 serial DMA (SDMA) channels; the MPC857T and MPC857DSL have 10 serial DMA (SDMA) channels
 - Three parallel I/O registers with open-drain capability
- Four baud rate generators
 - Independent (can be connected to any SCC or SMC)
 - Allow changes during operation
 - Autobaud support option
- The MPC862P and MPC862T have four SCCs (serial communication controller) The MPC857T and MPC857DSL have one SCC, SCC1; the MPC857DSL supports ethernet only
 - Serial ATM capability on all SCCs
 - Optional UTOPIA port on SCC4
 - Ethernet/IEEE 802.3 optional on SCC1–4, supporting full 10-Mbps operation
 - HDLC/SDLC
 - HDLC bus (implements an HDLC-based local area network (LAN))
 - Asynchronous HDLC to support PPP (point-to-point protocol)
 - AppleTalk



Thermal Calculation and Measurement

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

 $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

 $R_{\theta IC}$ = junction-to-case thermal resistance (°C/W)

 $R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature; see Figure 3.



Figure 3. Effect of Board Temperature Rise on Thermal Behavior



Num	Chavastavistia	33	MHz	40	MHz	50 I	MHz	66 I	ЛНz	l l m it
NUM	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
B29d	$\overline{\text{WE}}(0:3)$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 x B1 - 2.00)	43.50	_	35.50	_	28.00	_	20.70	_	ns
B29e	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 1.50 x B1 - 2.00)	43.50	_	35.50	_	28.00	_	20.70	_	ns
B29f	WE(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 6.30)	5.00	_	3.00	_	1.10	_	0.00	_	ns
B29g	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 - 6.30)	5.00		3.00	_	1.10	_	0.00	_	ns
B29h	WE(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 3.30)	38.40	_	31.10	_	24.20	_	17.50	_	ns
B29i	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 - 3.30)	38.40	_	31.10	_	24.20	_	17.50	_	ns
B30	\overline{CS} , \overline{WE} (0:3) negated to A(0:31), BADDR(28:30) Invalid GPCM write access ¹¹ (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	_	3.00	_	1.80	—	ns
B30a	$\label{eq:weighted} \begin{array}{l} \overline{\text{WE}}(0:3) \text{ negated to A}(0:31),\\ \text{BADDR}(28:30) \text{ Invalid GPCM}, \text{ write}\\ \text{access, TRLX} = 0, \text{ CSNT} = 1, \overline{\text{CS}}\\ \text{negated to A}(0:31) \text{ invalid GPCM write}\\ \text{access TRLX} = 0, \text{ CSNT} = 1 \text{ ACS} = 10,\\ \text{or ACS} == 11, \text{ EBDF} = 0 (\text{MIN} = 0.50)\\ \text{x B1} - 2.00) \end{array}$	13.20	_	10.50		8.00		5.60	_	ns
B30b	$\overline{WE}(0:3) \text{ negated to } A(0:31) \text{ Invalid} \\ \text{GPCM BADDR}(28:30) \text{ invalid GPCM} \\ \text{write access, TRLX = 1, CSNT = 1.} \\ \overline{CS} \text{ negated to } A(0:31) \text{ Invalid GPCM} \\ \text{write access TRLX = 1, CSNT = 1,} \\ \text{ACS = 10, or ACS == 11 EBDF = 0} \\ (\text{MIN = 1.50 x B1 - 2.00)} \\ \end{array}$	43.50		35.50		28.00	_	20.70		ns

Table 7. Bus Operation Timings (continued)



Figure 4 is the control timing diagram.



Figure 5 provides the timing for the external clock.



Figure 5. External Clock Timing



Figure 8 provides the timing for the synchronous input signals.



Figure 8. Synchronous Input Signals Timing

Figure 9 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.



Figure 9. Input Data Timing in Normal Case





Figure 18 provides the timing for the external bus controlled by the UPM.

Figure 18. External Bus Timing (UPM Controlled Signals)



Figure 19 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.



Cycles Timing

Figure 20 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.





Figure 26 provides the PCMCIA access cycle timing for the external bus read.



Figure 26. PCMCIA Access Cycles Timing External Bus Read



Table 12 shows the reset timing for the MPC862/857T/857DSL.

Table 12. Reset Timing

Num Characteristic –		33 N	/IHz	40 M	40 MHz		50 MHz		66 MHz	
Num	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
R69	CLKOUT to HRESET high impedance (MAX = 0.00 x B1 + 20.00)		20.00	_	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to SRESET high impedance (MAX = 0.00 x B1 + 20.00)	_	20.00		20.00	_	20.00	_	20.00	ns
R71	RSTCONF pulse width (MIN = 17.00 x B1)	515.20	—	425.00	_	340.00	_	257.60		ns
R72	_		—		—	—	—	—	_	—
R73	Configuration data to HRESET rising edge set up time (MIN = 15.00 x B1 + 50.00)	504.50		425.00	_	350.00	_	277.30	-	ns
R74	Configuration data to RSTCONF rising edge set up time (MIN = 0.00 x B1 + 350.00)	350.00	—	350.00	_	350.00	_	350.00	_	ns
R75	Configuration data hold time after RSTCONF negation (MIN = 0.00 x B1 + 0.00)	0.00		0.00	—	0.00	—	0.00		ns
R76	Configuration data hold time after HRESET negation (MIN = 0.00 x B1 + 0.00)	0.00	_	0.00	_	0.00	—	0.00		ns
R77	HRESET and RSTCONF asserted to data out drive (MAX = 0.00 x B1 + 25.00)		25.00		25.00	_	25.00	—	25.00	ns
R78	RSTCONF negated to data out high impedance. (MAX = 0.00 x B1 + 25.00)	_	25.00	_	25.00	_	25.00	_	25.00	ns
R79	CLKOUT of last rising edge before chip three-states $\overrightarrow{\text{HRESET}}$ to data out high impedance. (MAX = 0.00 x B1 + 25.00)	_	25.00	_	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK set up (MIN = 3.00 x B1)	90.90	_	75.00	—	60.00	—	45.50	_	ns
R81	DSDI, DSCK hold time (MIN = 0.00 x B1 + 0.00)	0.00	_	0.00	_	0.00	_	0.00	_	ns
R82	SRESET negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 x B1)	242.40		200.00	_	160.00	_	121.20	_	ns







Figure 33. Reset Timing—Configuration from Data Bus

Figure 34 provides the reset timing for the data bus weak drive during configuration.



Figure 34. Reset Timing—Data Bus Weak Drive during Configuration









11 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC862/857T/857DSL.

11.1 PIP/PIO AC Electrical Specifications

Table 14 provides the PIP/PIO AC timings as shown in Figure 40 though Figure 44.

Table 14. PIP/PIO Timing

Num	Characteristic	All Freq	Unit	
Num	Characteristic	Min	Мах	Onit
21	Data-in setup time to STBI low	0	_	ns
22	Data-in hold time to STBI high	2.5 – t3 ¹	_	clk
23	STBI pulse width	1.5	-	clk
24	STBO pulse width	1 clk – 5 ns	-	ns
25	Data-out setup time to STBO low	2	-	clk
26	Data-out hold time from STBO high	5	-	clk
27	STBI low to STBO low (Rx interlock)	—	2	clk
28	STBI low to STBO high (Tx interlock)	2	-	clk
29	Data-in setup time to clock high	15	-	ns
30	Data-in hold time from clock high	7.5	_	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	_	25	ns

¹ t3 = Specification 23



Figure 40. PIP Rx (Interlock Mode) Timing Diagram





Figure 49. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA





Figure 51. CPM General-Purpose Timers Timing Diagram

11.6 Serial Interface AC Electrical Specifications

Table 19 provides the serial interface timings as shown in Figure 52 though Figure 56.

Num	Characteristic	All Freq	Unit	
Num	Characteristic	Min	Мах	Onit
70	L1RCLK, L1TCLK frequency (DSC = 0) ^{1, 2}	_	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0) 2	P + 10	—	ns
71a	L1RCLK, L1TCLK width high (DSC = 0) 3	P + 10	—	ns
72	L1TXD, L1ST(1–4), L1RQ, L1CLKO rise/fall time	_	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20.00	—	ns
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	_	ns
75	L1RSYNC, L1TSYNC rise/fall time	_	15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1-4) valid ⁴	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1-4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1-4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid ⁴	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC =1)	_	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns

Table 19. SI Timing



11.7 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

Table 20. NMSI External Clock Timing

Num	Characteristic	All Freq	Unit	
Num	Characteristic	Min	Мах	Om
100	RCLK1 and TCLK1 width high ¹	1/SYNCCLK	_	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK +5	_	ns
102	RCLK1 and TCLK1 rise/fall time	_	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	RTS1 active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	CTS1 setup time to TCLK1 rising edge	5.00		ns
106	RXD1 setup time to RCLK1 rising edge	5.00		ns
107	RXD1 hold time from RCLK1 rising edge ²	5.00	_	ns
108	CD1 setup Time to RCLK1 rising edge	5.00	_	ns

¹ The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 21 provides the NMSI internal clock timing.

Table 21. NMSI Internal Clock Timing

Num	Charactoristic	All Freq	Unit	
Num	Characteristic	Min	Мах	Onit
100	RCLK1 and TCLK1 frequency ¹	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	_	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	RTS1 active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	CTS1 setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	_	ns
107	RXD1 hold time from RCLK1 rising edge ²	0.00	—	ns
108	CD1 setup time to RCLK1 rising edge	40.00		ns

¹ The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 3/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.





Figure 59. HDLC Bus Timing Diagram

11.8 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 60 though Figure 64.

Table 22. Ethernet Timing

Num	Characteristic		uencies	Unit
Num			Мах	Omit
120	CLSN width high	40	—	ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period ¹	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	_	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period ¹	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	10	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	10	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns



Num	Characteristic	All Freq	Unit	
Num			Мах	Unit
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns
135	RSTRT active delay (from TCLK1 falling edge)	10	50	ns
136	RSTRT inactive delay (from TCLK1 falling edge)	10	50	ns
137	REJECT width low	1	—	CLK
138	CLKO1 low to SDACK asserted ²	—	20	ns
139	CLKO1 low to SDACK negated ²	—	20	ns

Table 22. Ethernet Timing (continued)

¹ The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2/1.

² SDACK is asserted whenever the SDMA writes the incoming frame DA into memory.









Figure 64. CAM Interface REJECT Timing Diagram



Num	Characteristic	Min	Max	Unit
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Table 30. MII Transmit Signal Timing (continued)

Figure 74 shows the MII transmit signal timing diagram.



Figure 74. MII Transmit Signal Timing Diagram

13.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 31 provides information on the MII async inputs signal timing.

Table 31. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 75 shows the MII asynchronous inputs signal timing diagram.



Figure 75. MII Async Inputs Timing Diagram

13.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 32 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.



Name	Pin Number	Туре
PA15 RXD1 RXD4	C18	Bidirectional
PA14 TXD1 TXD4	D17	Bidirectional (Optional: Open-drain)
PA13 RXD2	E17	Bidirectional
PA12 TXD2	F17	Bidirectional (Optional: Open-drain)
PA11 L1TXDB RXD3	G16	Bidirectional (Optional: Open-drain)
PA10 L1RXDB TXD3	J17	Bidirectional (Optional: Open-drain)
PA9 L1TXDA	К18	Bidirectional (Optional: Open-drain)
RXD4		
PA8 L1RXDA TXD4	L17	Bidirectional (Optional: Open-drain)
PA7 CLK1 L1RCLKA BRGO1 TIN1	M19	Bidirectional
PA6 CLK2 TOUT1	M17	Bidirectional
PA5 CLK3 L1TCLKA BRGO2 TIN2	N18	Bidirectional
PA4 CLK4 TOUT2	P19	Bidirectional
PA3 CLK5 BRGO3 TIN3	P17	Bidirectional

Table 35. Pin Assignments (continued)