



Welcome to [E-XFL.COM](#)

Understanding [Embedded - Microprocessors](#)

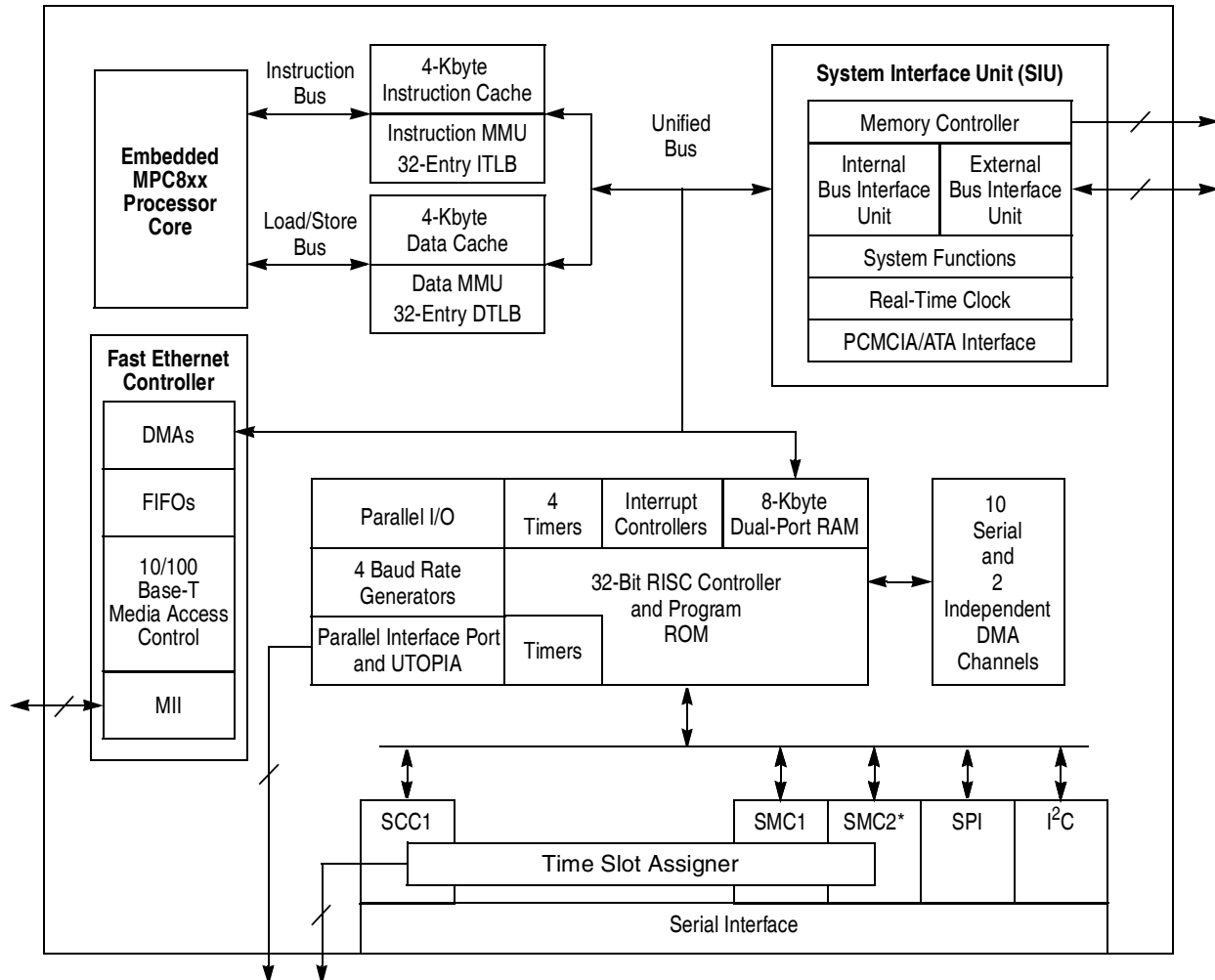
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc862tzq50b



*The MPC857DSL does not contain SMC2 nor the Time Slot Assigner, and provides eight SDMA controllers.

Figure 2. MPC857T/MPC857DSL Block Diagram

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC862/857T/857DSL. [Table 2](#) provides the maximum ratings.

Table 2. Maximum Tolerated Ratings
(GND = 0 V)

Rating	Symbol	Value	Unit	Max Freq (MHz)
Supply voltage ¹	VDDH	-0.3 to 4.0	V	-
	VDDL	-0.3 to 4.0	V	-
	KAPWR	-0.3 to 4.0	V	-
	VDDSYN	-0.3 to 4.0	V	-

Table 5. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Output Low Voltage IOL = 2.0 mA (CLKOUT) IOL = 3.2 mA ³ IOL = 5.3 mA ⁴ IOL = 7.0 mA (TXD1/PA14, TXD2/PA12) IOL = 8.9 mA ($\overline{TS}$, $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{HRESET}$, $\overline{SRESET}$)	VOL	—	0.5	V

¹ $V_{IL}(\text{max})$ for the I²C interface is 0.8 V rather than the 1.5 V as specified in the I²C standard.

² Input capacitance is periodically sampled.

³ A(0:31), $\overline{TSI0}/\overline{REG}$, $\overline{TSI1}$, D(0:31), DP(0:3)/ $\overline{IRQ}$ (3:6), $\overline{RD}/\overline{WR}$, $\overline{BURST}$, $\overline{RSV}/\overline{IRQ2}$, $\overline{IP_B}(0:1)/\overline{IWP}(0:1)/\overline{VFLS}(0:1)$, $\overline{IP_B2}/\overline{IOIS16_B}/\overline{AT2}$, $\overline{IP_B3}/\overline{IWP2}/\overline{VF2}$, $\overline{IP_B4}/\overline{LWP0}/\overline{VF0}$, $\overline{IP_B5}/\overline{LWP1}/\overline{VF1}$, $\overline{IP_B6}/\overline{DSDI}/\overline{AT0}$, $\overline{IP_B7}/\overline{PTR}/\overline{AT3}$, $\overline{RXD1}/\overline{PA15}$, $\overline{RXD2}/\overline{PA13}$, $\overline{L1TXDB}/\overline{PA11}$, $\overline{L1RXDB}/\overline{PA10}$, $\overline{L1TXDA}/\overline{PA9}$, $\overline{L1RXDA}/\overline{PA8}$, $\overline{TIN1}/\overline{L1RCLKA}/\overline{BRGO1}/\overline{CLK1}/\overline{PA7}$, $\overline{BRGCLK1}/\overline{TOUT1}/\overline{CLK2}/\overline{PA6}$, $\overline{TIN2}/\overline{L1TCLKA}/\overline{BRGO2}/\overline{CLK3}/\overline{PA5}$, $\overline{TOUT2}/\overline{CLK4}/\overline{PA4}$, $\overline{TIN3}/\overline{BRGO3}/\overline{CLK5}/\overline{PA3}$, $\overline{BRGCLK2}/\overline{L1RCLKB}/\overline{TOUT3}/\overline{CLK6}/\overline{PA2}$, $\overline{TIN4}/\overline{BRGO4}/\overline{CLK7}/\overline{PA1}$, $\overline{L1TCLKB}/\overline{TOUT4}/\overline{CLK8}/\overline{PA0}$, $\overline{REJECT1}/\overline{SPISEL}/\overline{PB31}$, $\overline{SPICLK}/\overline{PB30}$, $\overline{SPIMOSI}/\overline{PB29}$, $\overline{BRGO4}/\overline{SPIMISO}/\overline{PB28}$, $\overline{BRGO1}/\overline{I2CSDA}/\overline{PB27}$, $\overline{BRGO2}/\overline{I2CSCL}/\overline{PB26}$, $\overline{SMTXD1}/\overline{PB25}$, $\overline{SMRXD1}/\overline{PB24}$, $\overline{SMSYN1}/\overline{SDACK1}/\overline{PB23}$, $\overline{SMSYN2}/\overline{SDACK2}/\overline{PB22}$, $\overline{SMTXD2}/\overline{L1CLKOB}/\overline{PB21}$, $\overline{SMRXD2}/\overline{L1CLKOA}/\overline{PB20}$, $\overline{L1ST1}/\overline{RTS1}/\overline{PB19}$, $\overline{L1ST2}/\overline{RTS2}/\overline{PB18}$, $\overline{L1ST3}/\overline{L1RQB}/\overline{PB17}$, $\overline{L1ST4}/\overline{L1RQA}/\overline{PB16}$, $\overline{BRGO3}/\overline{PB15}$, $\overline{RSTR1}/\overline{PB14}$, $\overline{L1ST1}/\overline{RTS1}/\overline{DREQ0}/\overline{PC15}$, $\overline{L1ST2}/\overline{RTS2}/\overline{DREQ1}/\overline{PC14}$, $\overline{L1ST3}/\overline{L1RQB}/\overline{PC13}$, $\overline{L1ST4}/\overline{L1RQA}/\overline{PC12}$, $\overline{CTS1}/\overline{PC11}$, $\overline{TGATE1}/\overline{CD1}/\overline{PC10}$, $\overline{CTS2}/\overline{PC9}$, $\overline{TGATE2}/\overline{CD2}/\overline{PC8}$, $\overline{CTS3}/\overline{SDACK2}/\overline{L1TSYNCB}/\overline{PC7}$, $\overline{CD3}/\overline{L1RSYNCB}/\overline{PC6}$, $\overline{CTS4}/\overline{SDACK1}/\overline{L1TSYNCA}/\overline{PC5}$, $\overline{CD4}/\overline{L1RSYNCA}/\overline{PC4}$, $\overline{PD15}/\overline{L1TSYNCA}$, $\overline{PD14}/\overline{L1RSYNCA}$, $\overline{PD13}/\overline{L1TSYNCB}$, $\overline{PD12}/\overline{L1RSYNCB}$, $\overline{PD11}/\overline{RXD3}$, $\overline{PD10}/\overline{TXD3}$, $\overline{PD9}/\overline{RXD4}$, $\overline{PD8}/\overline{TXD4}$, $\overline{PD5}/\overline{REJECT2}$, $\overline{PD6}/\overline{RTS4}$, $\overline{PD7}/\overline{RTS3}$, $\overline{PD4}/\overline{REJECT3}$, $\overline{PD3}$, $\overline{MII_MDC}$, $\overline{MII_TX_ER}$, $\overline{MII_EN}$, $\overline{MII_MDIO}$, $\overline{MII_TXD}[0:3]$.

⁴ $\overline{BDIP}/\overline{GPL_B}(5)$, $\overline{BR}$, $\overline{BG}$, $\overline{FRZ}/\overline{IRQ6}$, $\overline{CS}(0:5)$, $\overline{CS}(6)/\overline{CE}(1)_B$, $\overline{CS}(7)/\overline{CE}(2)_B$, $\overline{WE0}/\overline{BS_B0}/\overline{IORD}$, $\overline{WE1}/\overline{BS_B1}/\overline{IOWR}$, $\overline{WE2}/\overline{BS_B2}/\overline{PCOE}$, $\overline{WE3}/\overline{BS_B3}/\overline{PCWE}$, $\overline{BS_A}(0:3)$, $\overline{GPL_A0}/\overline{GPL_B0}$, $\overline{OE}/\overline{GPL_A1}/\overline{GPL_B1}$, $\overline{GPL_A}(2:3)/\overline{GPL_B}(2:3)/\overline{CS}(2:3)$, $\overline{UPWAITA}/\overline{GPL_A4}$, $\overline{UPWAITB}/\overline{GPL_B4}$, $\overline{GPL_A5}$, $\overline{ALE_A}$, $\overline{CE1_A}$, $\overline{CE2_A}$, $\overline{ALE_B}/\overline{DSCK}/\overline{AT1}$, $\overline{OP}(0:1)$, $\overline{OP2}/\overline{MODCK1}/\overline{STS}$, $\overline{OP3}/\overline{MODCK2}/\overline{DSDO}$, $\overline{BADDR}(28:30)$.

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B8a	CLKOUT to TSIZ(0:1), $\overline{\text{REG}}$, $\overline{\text{RSV}}$, AT(0:3) $\overline{\text{BDIP}}$, PTR valid (MAX = $0.25 \times B1 + 6.3$)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B8b	CLKOUT to $\overline{\text{BR}}$, $\overline{\text{BG}}$, VFSL(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS Valid ⁴ (MAX = $0.25 \times B1 + 6.3$)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/ $\overline{\text{WR}}$, BURST, D(0:31), DP(0:3), TSIZ(0:1), $\overline{\text{REG}}$, $\overline{\text{RSV}}$, AT(0:3), PTR High-Z (MAX = $0.25 \times B1 + 6.3$)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B11	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ assertion (MAX = $0.25 \times B1 + 6.0$)	7.60	13.60	6.30	12.30	5.00	11.00	3.80	11.30	ns
B11a	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = $0.00 \times B1 + 9.30$ ⁵)	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.80	ns
B12	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ negation (MAX = $0.25 \times B1 + 4.8$)	7.60	12.30	6.30	11.00	5.00	9.80	3.80	8.50	ns
B12a	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = $0.00 \times B1 + 9.00$)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B13	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ High-Z (MIN = $0.25 \times B1$)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns
B13a	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{BI}}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = $0.00 \times B1 + 2.5$)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to $\overline{\text{TEA}}$ assertion (MAX = $0.00 \times B1 + 9.00$)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B15	CLKOUT to $\overline{\text{TEA}}$ High-Z (MIN = $0.00 \times B1 + 2.50$)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{\text{TA}}$, $\overline{\text{BI}}$ valid to CLKOUT (setup time) (MIN = $0.00 \times B1 + 6.00$)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B16a	$\overline{\text{TEA}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, $\overline{\text{CR}}$ valid to CLKOUT (setup time) (MIN = $0.00 \times B1 + 4.5$)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	$\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$, valid to CLKOUT (setup time) ⁶ (4MIN = $0.00 \times B1 + 0.00$)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$ valid (hold time) (MIN = $0.00 \times B1 + 1.00$ ⁷)	1.00	—	1.00	—	1.00	—	2.00	—	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid (hold time) (MIN = $0.00 \times B1 + 2.00$)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) ⁸ (MIN = $0.00 \times B1 + 6.00$)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) ⁸ (MIN = $0.00 \times B1 + 1.00$ ⁹)	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) ¹⁰ (MIN = $0.00 \times B1 + 4.00$)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) ¹⁰ (MIN = $0.00 \times B1 + 2.00$)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 (MAX = $0.25 \times B1 + 6.3$)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = $0.00 \times B1 + 8.00$)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = $0.25 \times B1 + 6.3$)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = $0.375 \times B1 + 6.6$)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = $0.00 \times B1 + 8.00$)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = $0.25 \times B1 - 2.00$)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = $0.50 \times B1 - 2.00$)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$ (0:3) asserted (MAX = $0.00 \times B1 + 9.00$)	—	9.00		9.00		9.00		9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = $0.00 \times B1 + 9.00$)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns

Table 7. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 x B1 - 2.00)	35.90	—	29.30	—	23.00	—	16.90	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B28	CLKOUT rising edge to $\overline{WE}$ (0:3) negated GPCM write access CSNT = 0 (MAX = 0.00 x B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$ (0:3) negated GPCM write access TRLX = 0, 1, CSNT = 1, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	—	14.30	—	13.00	—	11.80	—	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}$ (0:3) negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0,1, CSNT = 1, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	—	18.00	—	18.00	—	14.30	—	12.30	ns
B29	$\overline{WE}$ (0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29a	$\overline{WE}$ (0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B29b	$\overline{CS}$ negated to D(0:31), DP(0:3), High Z GPCM write access, ACS = 00, TRLX = 0,1 & CSNT = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29c	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns

Figure 4 is the control timing diagram.

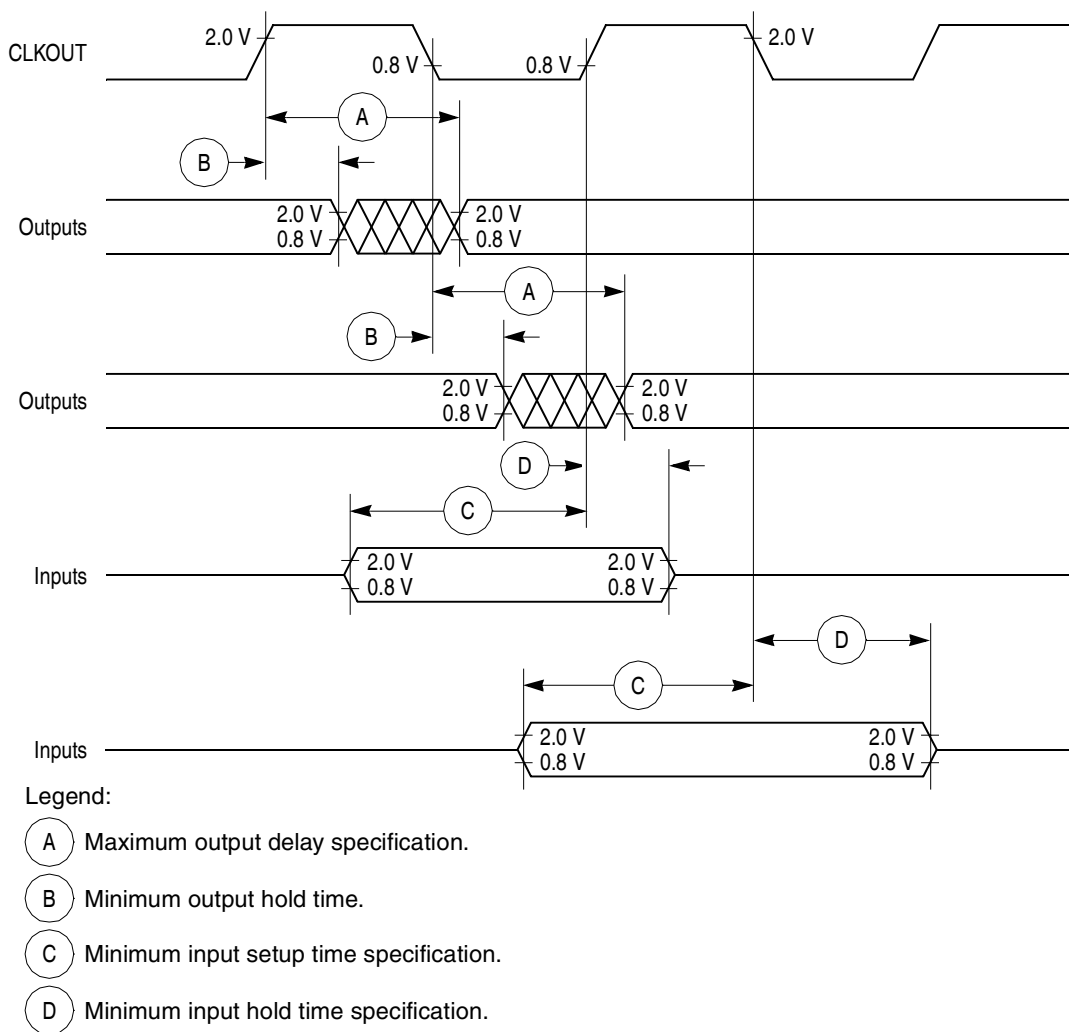


Figure 4. Control Timing

Figure 5 provides the timing for the external clock.

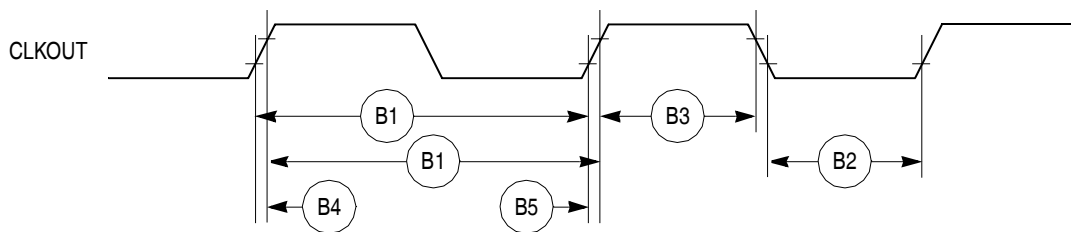


Figure 5. External Clock Timing

Figure 8 provides the timing for the synchronous input signals.

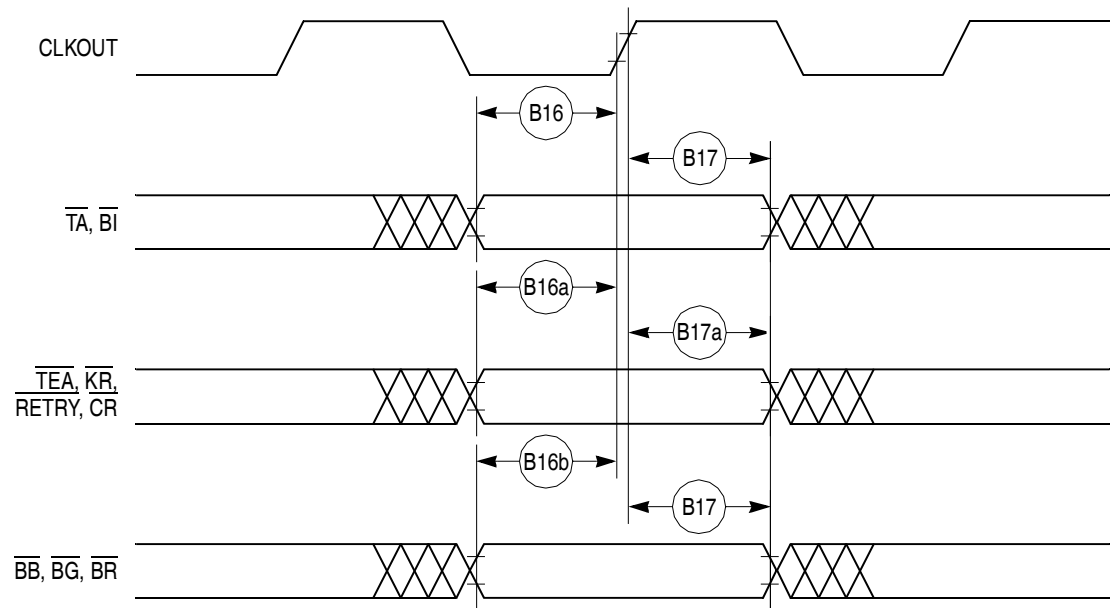


Figure 8. Synchronous Input Signals Timing

Figure 9 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

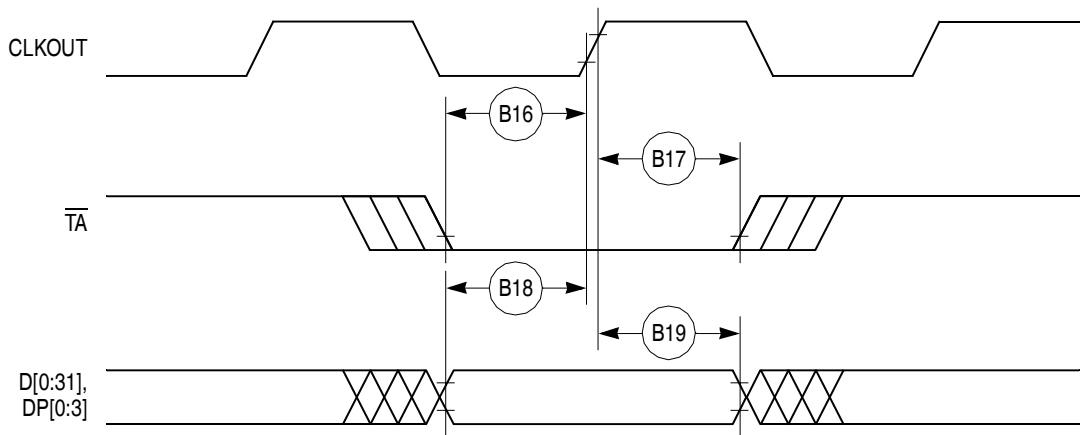


Figure 9. Input Data Timing in Normal Case

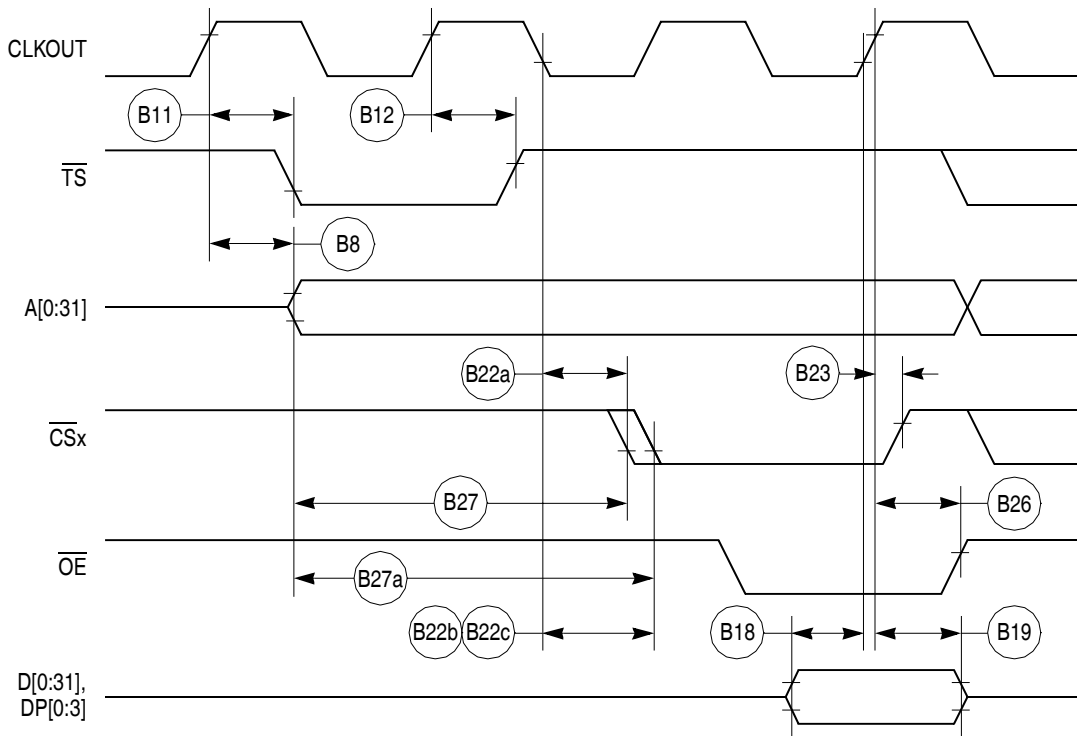


Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

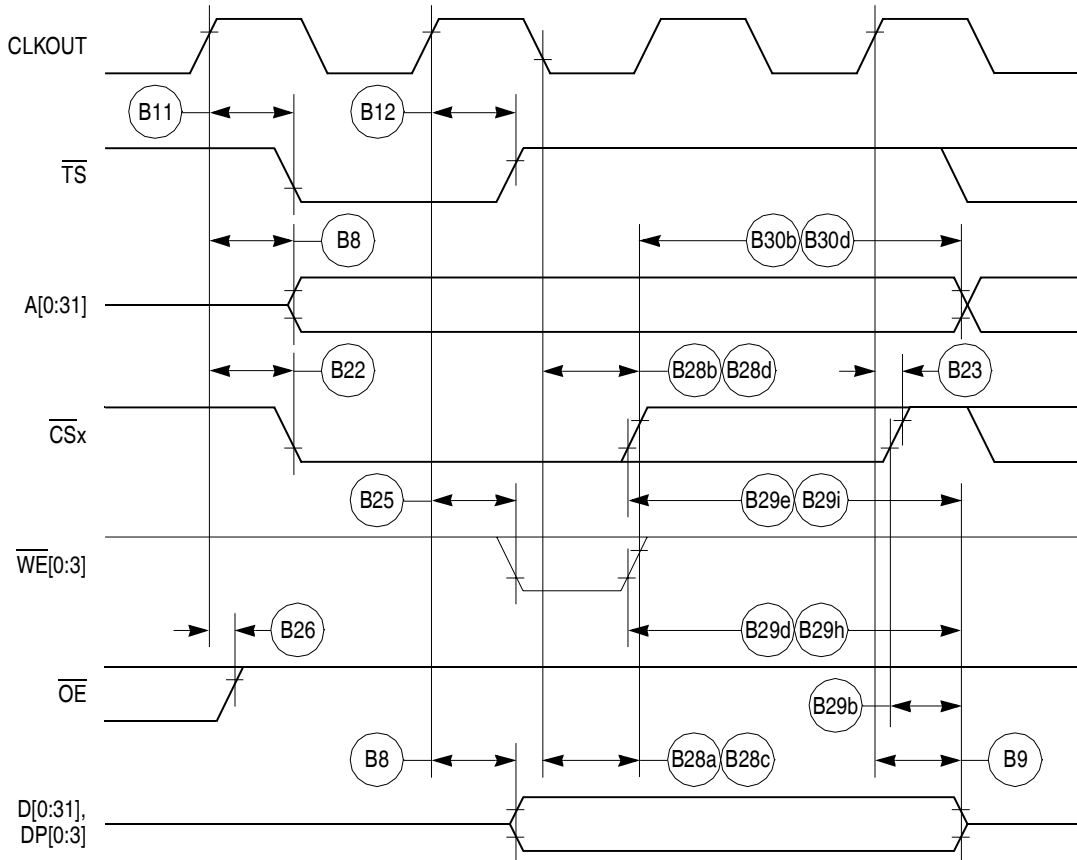


Figure 17. External Bus Write Timing (GPCM Controlled—TRLX = 0,1, CSNT = 1)

Figure 19 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

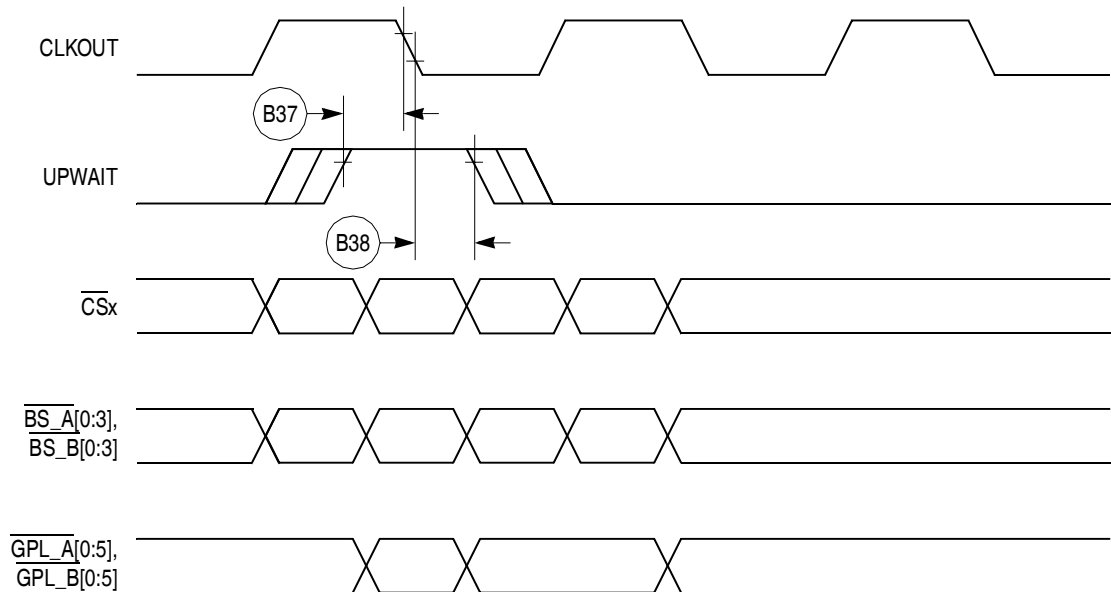


Figure 19. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

Figure 20 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

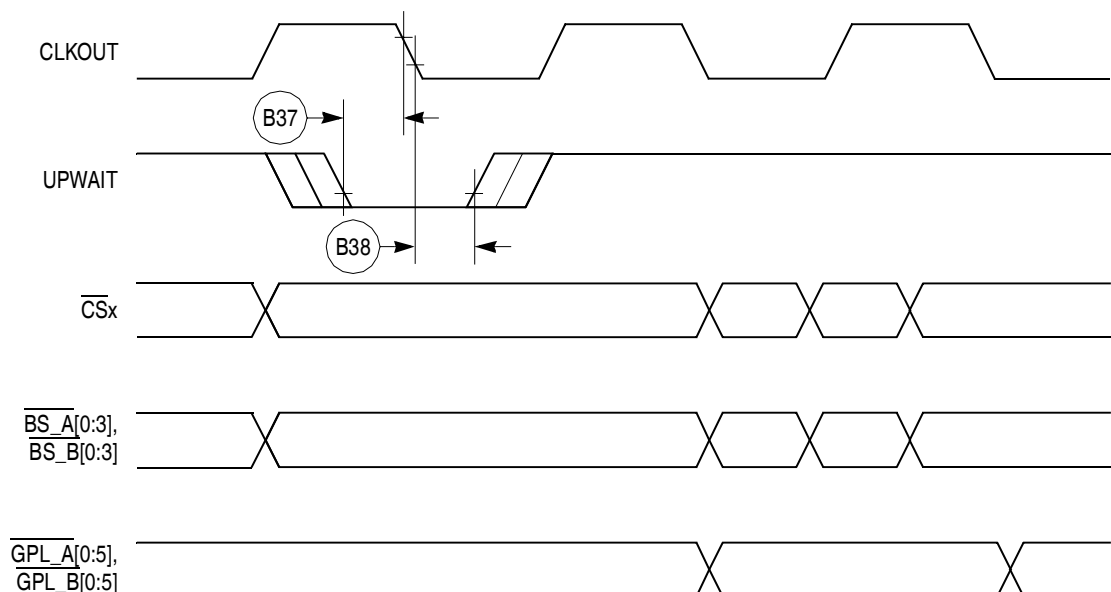
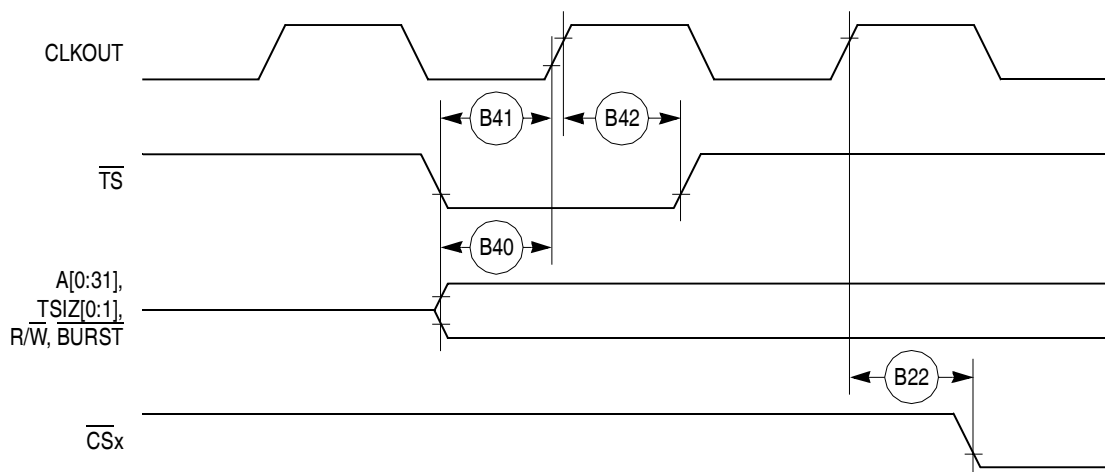


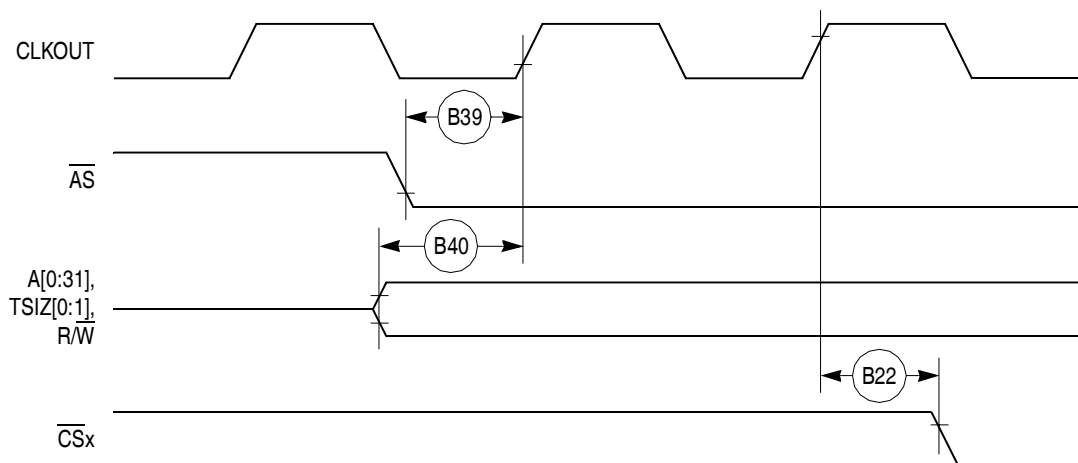
Figure 20. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing

Figure 21 provides the timing for the synchronous external master access controlled by the GPCM.



**Figure 21. Synchronous External Master Access Timing
(GPCM Handled ACS = 00)**

Figure 22 provides the timing for the asynchronous external master memory access controlled by the GPCM.



**Figure 22. Asynchronous External Master Memory Access Timing
(GPCM Controlled—ACS = 00)**

Figure 23 provides the timing for the asynchronous external master control signals negation.

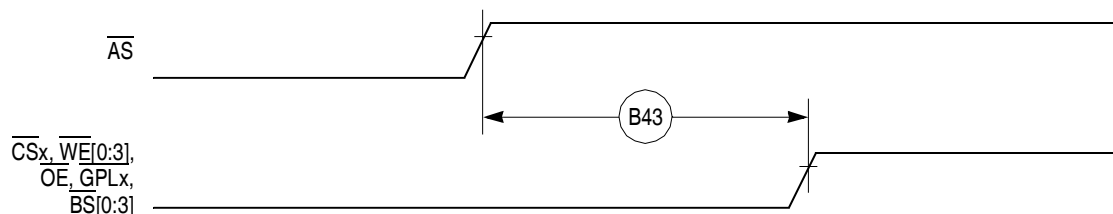


Figure 23. Asynchronous External Master—Control Signals Negation Timing

Figure 35 provides the reset timing for the debug port configuration.

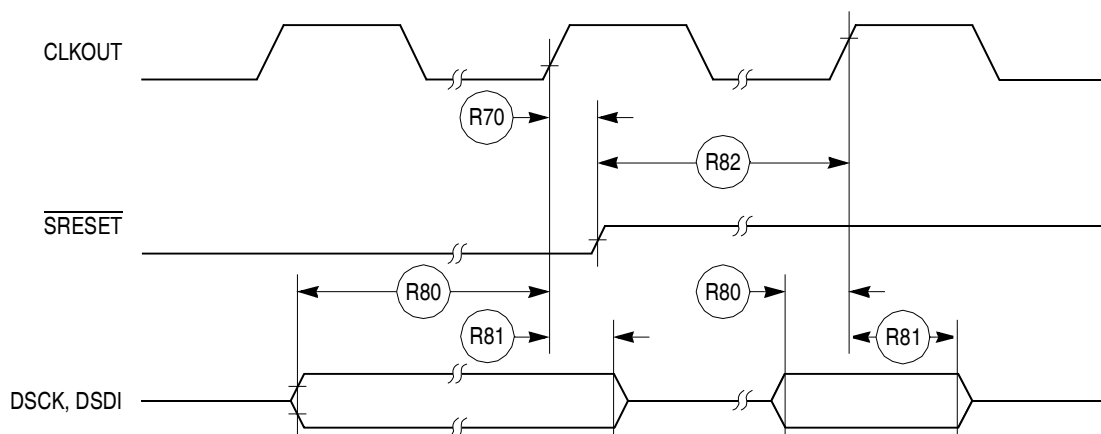


Figure 35. Reset Timing—Debug Port Configuration

10 IEEE 1149.1 Electrical Specifications

Table 13 provides the JTAG timings for the MPC862/857T/857DSL shown in Figure 36 though Figure 39.

Table 13. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

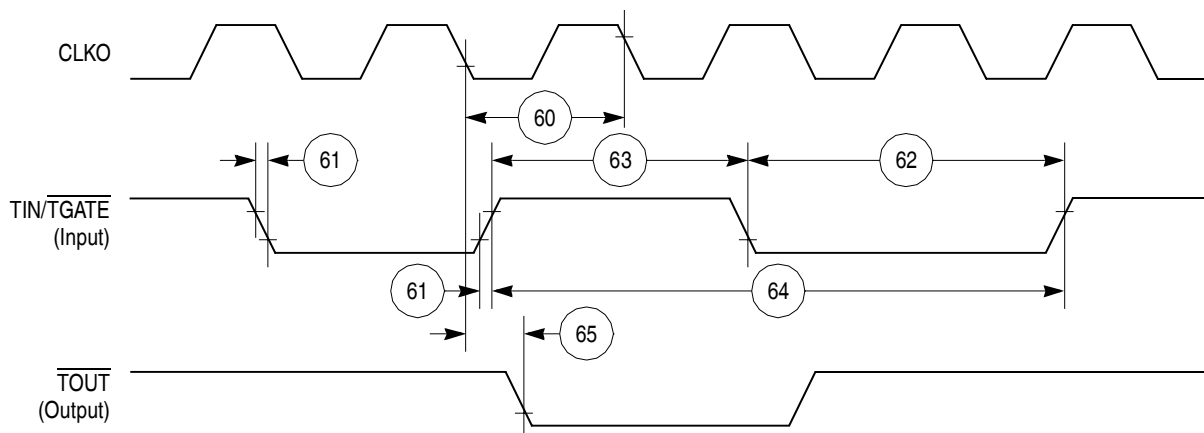


Figure 51. CPM General-Purpose Timers Timing Diagram

11.6 Serial Interface AC Electrical Specifications

Table 19 provides the serial interface timings as shown in Figure 52 through Figure 56.

Table 19. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLK, L1TCLK frequency (DSC = 0) ^{1, 2}	—	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0) ²	P + 10	—	ns
71a	L1RCLK, L1TCLK width high (DSC = 0) ³	P + 10	—	ns
72	L1TXD, L1ST(1–4), $\overline{\text{L1RQ}}$, L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20.00	—	ns
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1–4) valid ⁴	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1–4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1–4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid ⁴	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC = 1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC = 1)	P + 10	—	ns

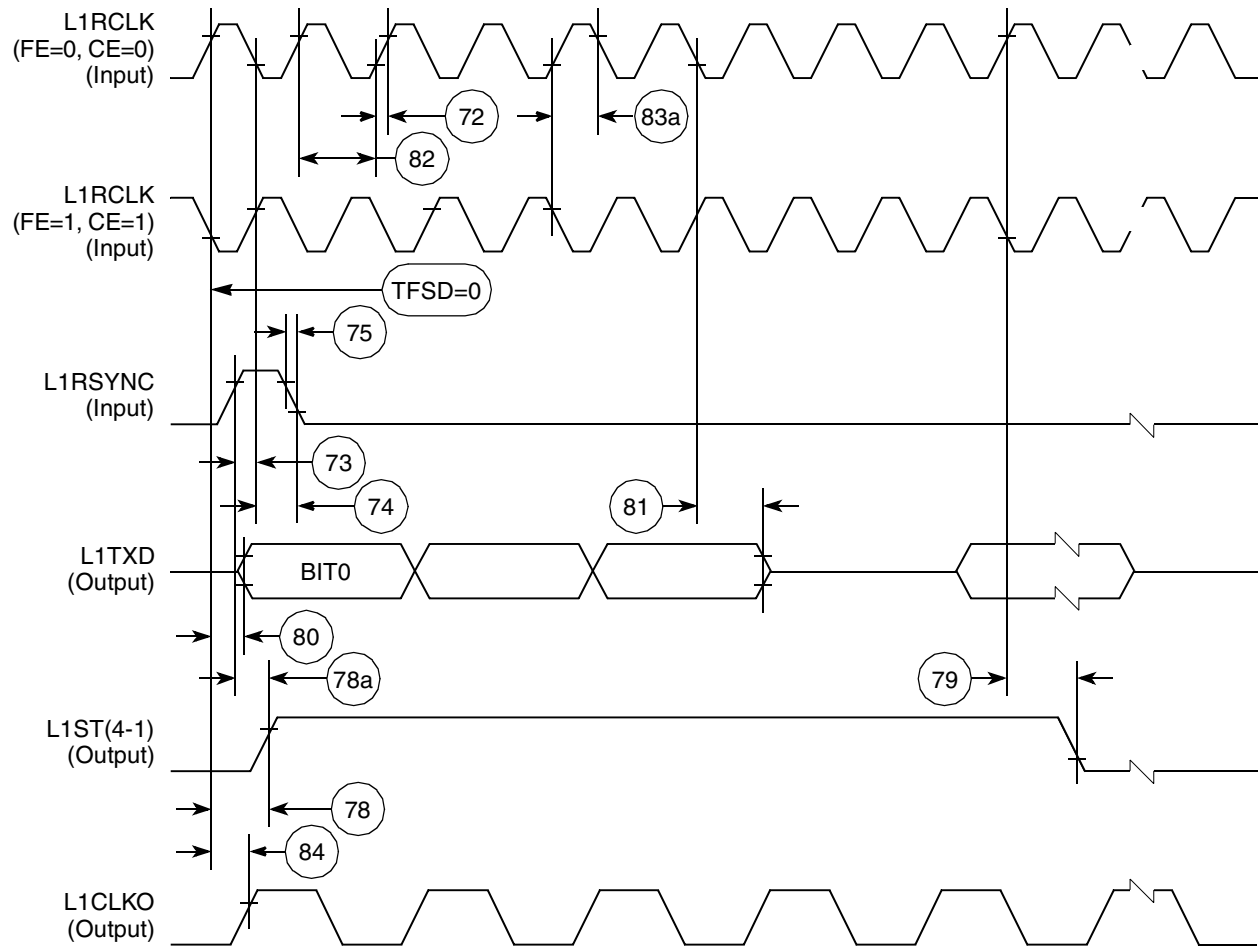


Figure 55. SI Transmit Timing with Double Speed Clocking (DSC = 1)

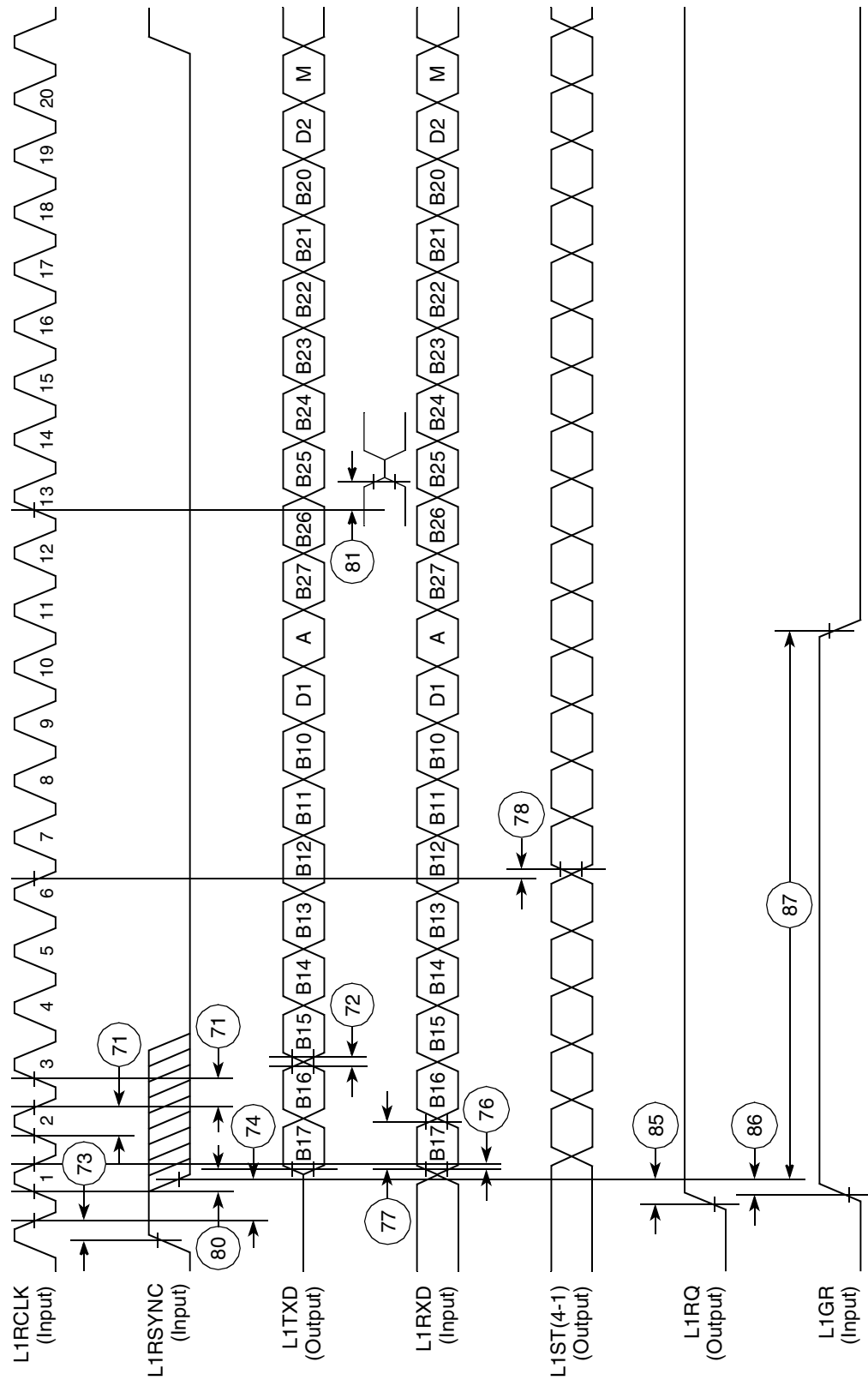


Figure 56. IDL Timing

11.12 I²C AC Electrical Specifications

Table 26 provides the I²C (SCL < 100 KHz) timings.

Table 26. I²C Timing (SCL < 100 KHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0	100	kHz
200	SCL clock frequency (master) ¹	1.5	100	kHz
202	Bus free time between transmissions	4.7	—	μs
203	Low period of SCL	4.7	—	μs
204	High period of SCL	4.0	—	μs
205	Start condition setup time	4.7	—	μs
206	Start condition hold time	4.0	—	μs
207	Data hold time	0	—	μs
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	μs
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	μs

¹ SCL frequency is given by $SCL = BRGCLK_frequency / ((BRG\ register + 3) * pre_scaler * 2)$.
The ratio $SyncClk/(BRGCLK/pre_scaler)$ must be greater or equal to 4/1.

Table 27 provides the I²C (SCL > 100 kHz) timings.

Table 27. I²C Timing (SCL > 100 kHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) ¹	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	—	1/(2.2 * fSCL)	—	s
203	Low period of SCL	—	1/(2.2 * fSCL)	—	s
204	High period of SCL	—	1/(2.2 * fSCL)	—	s
205	Start condition setup time	—	1/(2.2 * fSCL)	—	s
206	Start condition hold time	—	1/(2.2 * fSCL)	—	s
207	Data hold time	—	0	—	s
208	Data setup time	—	1/(40 * fSCL)	—	s
209	SDL/SCL rise time	—	—	1/(10 * fSCL)	s
210	SDL/SCL fall time	—	—	1/(33 * fSCL)	s
211	Stop condition setup time	—	1/2(2.2 * fSCL)	—	s

¹ SCL frequency is given by $SCL = BrgClk_frequency / ((BRG\ register + 3) * pre_scaler * 2)$.
The ratio $SyncClk/(Brg_Clk/pre_scaler)$ must be greater or equal to 4/1.

Figure 71 shows signal timings during UTOPIA receive operations.

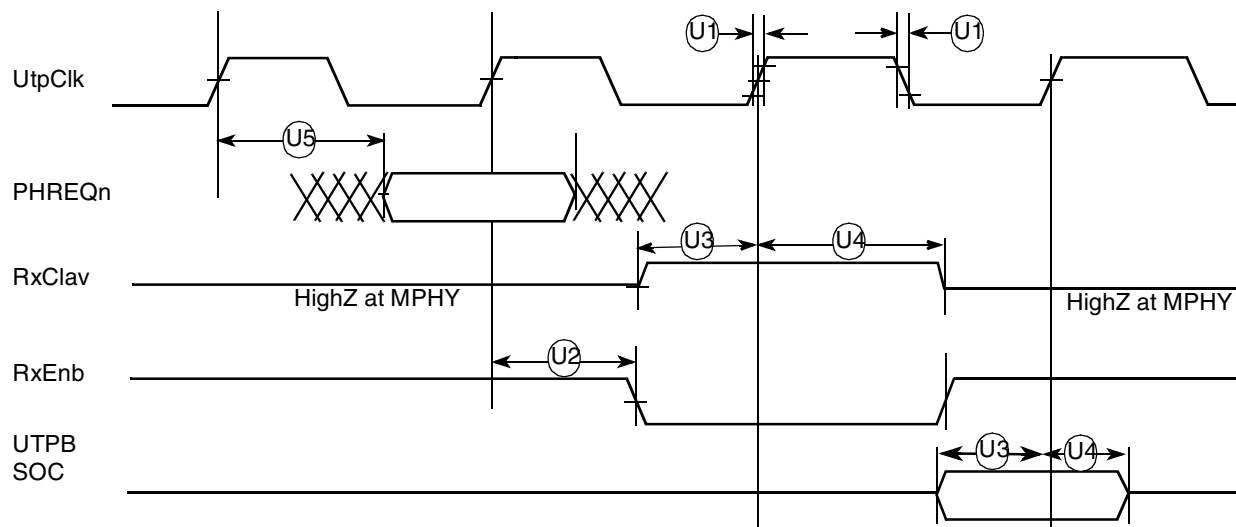


Figure 71. UTOPIA Receive Timing

Figure 72 shows signal timings during UTOPIA transmit operations.

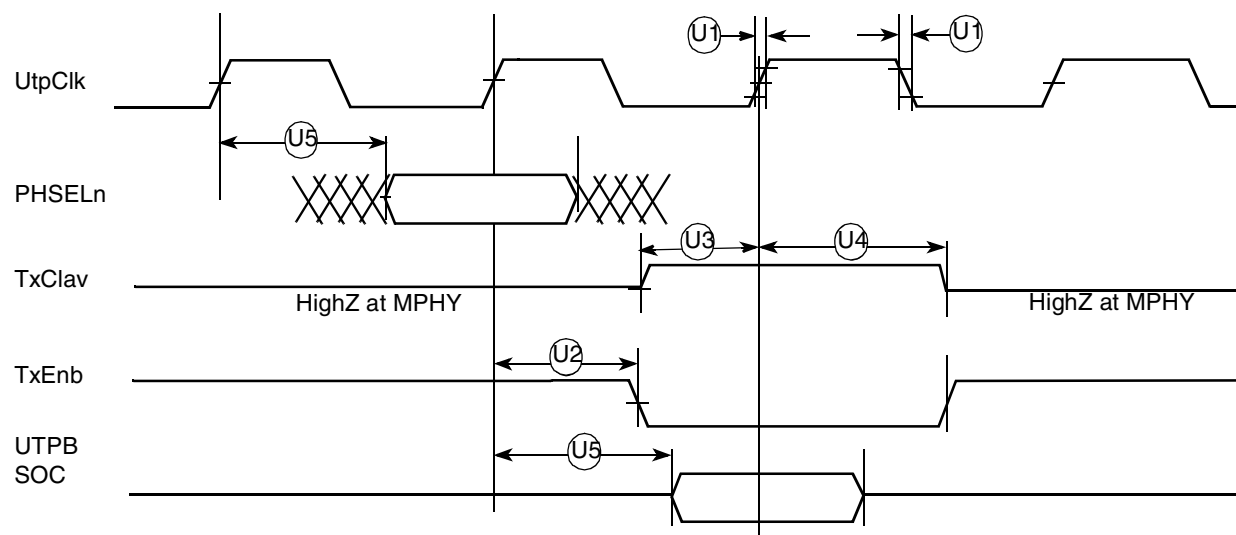


Figure 72. UTOPIA Transmit Timing

13 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Furthermore, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

13.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency - 1%.

Table 29 provides information on the MII receive signal timing.

Table 29. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Figure 73 shows MII receive signal timing.

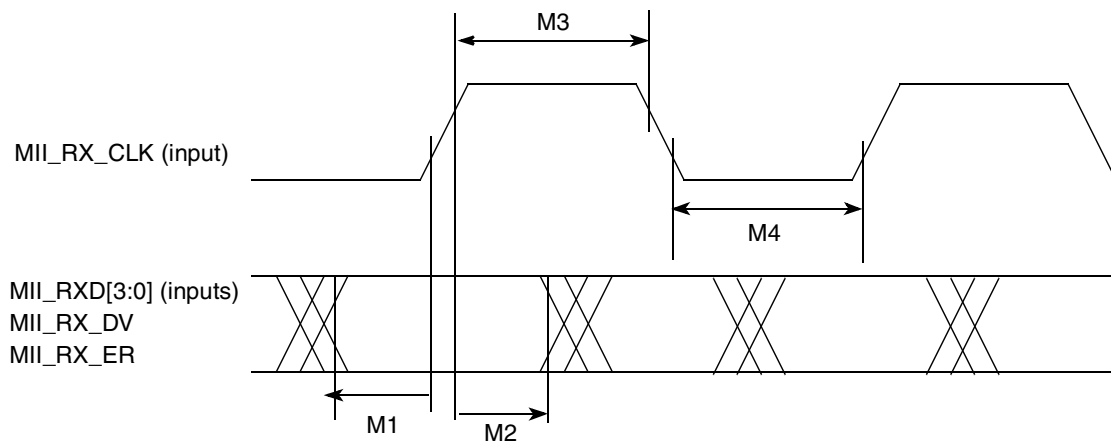


Figure 73. MII Receive Signal Timing Diagram

13.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency - 1%.

Table 30 provides information on the MII transmit signal timing.

Table 30. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
PD12 L1RSYNCB MII-MDC UTPB3	R16	Bidirectional
PD11 RXD3 MII-TXERR RXENB	T16	Bidirectional
PD10 TXD3 MII-RXD0 TXENB	W18	Bidirectional
PD9 RXD4 MII-TXD0 UTPCLK	V17	Bidirectional
PD8 TXD4 MII-MDC MII-RXCLK	W17	Bidirectional
PD7 RTS3 MII-RXERR UTPB4	T15	Bidirectional
PD6 RTS4 MII-RXDV UTPB5	V16	Bidirectional
PD5 REJECT2 MII-TXD3 UTPB6	U15	Bidirectional
PD4 REJECT3 MII-TXD2 UTPB7	U16	Bidirectional
PD3 REJECT4 MII-TXD1 SOC	W16	Bidirectional
TMS	G18	Input
TDI DSDI	H17	Input
TCK DSCK	H16	Input

Table 35. Pin Assignments (continued)

Name	Pin Number	Type
TRST	G19	Input
TDO DSDO	G17	Output
M_CRS	B7	Input
M_MDIO	H18	Bidirectional
M_TXEN	V15	Output
M_COL	H4	Input
KAPWR	R1	Power
GND	F6, F7, F8, F9, F10, F11, F12, F13, F14, G6, G7, G8, G9, G10, G11, G12, G13, G14, H6, H7, H8, H9, H10, H11, H12, H13, H14, J6, J7, J8, J9, J10, J11, J12, J13, J14, K6, K7, K8, K9, K10, K11, K12, K13, K14, L6, L7, L8, L9, L10, L11, L12, L13, L14, M6, M7, M8, M9, M10, M11, M12, M13, M14, N6, N7, N8, N9, N10, N11, N12, N13, N14, P6, P7, P8, P9, P10, P11, P12, P13, P14	Power
VDDL	A8, M1, W8, H19, F4, F16, P4, P16	Power
VDDH	E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P5, P15, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, T14	Power
N/C	D6, D13, D14, U2, V2	No-connect

¹ Classic SAR mode only

² ESAR mode only

14.2 Mechanical Dimensions of the PBGA Package

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to *Plastic Ball Grid Array Application Note* (order number: AN1231/D) available from your local Freescale sales office. [Figure 78](#) shows the mechanical dimensions of the PBGA package.