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Understanding Embedded - Microprocessors

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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (4), 10/100Mbps (1)
SATA	-
USB	·
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	·
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc862tzq80b

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



1 Overview

The MPC862/857T/857DSL is a derivative of Freescale's MPC860 PowerQUICC[™] family of devices. It is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC862/857T/857DSL provides enhanced ATM functionality over that of other ATM enabled members.

MPC862/857T/857DSL provides enhanced ATM functionality over that of other ATM-enabled members of the MPC860 family.

Table 1 shows the functionality supported by the members of the MPC862/857T/857DSL family.

Part	Ca	iche	Ethe	rnet		
	Instruction Cache	tion Data Cache 10T 10/100		SCC	SMC	
MPC862P	16 Kbyte	8 Kbyte	Up to 4	1	4	2
MPC862T	4 Kbyte	4 Kbyte	Up to 4	1	4	2
MPC857T	4 Kbyte	4 Kbyte	1	1	1	2
MPC857DSL	4 Kbyte	4 Kbyte	1	1	1 ¹	1 ²

Table 1. MPC862 Family Functionality

¹ On the MPC857DSL, the SCC (SCC1) is for ethernet only. Also, the MPC857DSL does not support the Time Slot Assigner (TSA).

² On the MPC857DSL, the SMC (SMC1) is for UART only.

2 Features

The following list summarizes the key MPC862/857T/857DSL features:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
 - The core performs branch prediction with conditional prefetch, without conditional execution
 - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1).
 - 16-Kbyte instruction cache (MPC862P) is four-way, set-associative with 256 sets; 4-Kbyte instruction cache (MPC862T, MPC857T, and MPC857DSL) is two-way, set-associative with 128 sets.
 - 8-Kbyte data cache (MPC862P) is two-way, set-associative with 256 sets; 4-Kbyte data cache (MPC862T, MPC857T, and MPC857DSL) is two-way, set-associative with 128 sets.
 - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
 - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
 - MMUs with 32-entry TLB, fully associative instruction and data TLBs
 - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
 - Advanced on-chip-emulation debug mode





Table 2. Maximum Tolerated Ratings (continued)

(GND = 0 V)

Rating	Symbol	Value	Unit	Max Freq (MHz)
Input voltage ²	V _{in}	GND-0.3 to VDDH	V	-
Temperature ³ (standard) ⁴	T _{A(min)}	0	°C	100
	T _{j(max)}	105	°C	100
Temperature ³ (extended)	T _{A(min)}	-40	°C	80
	T _{j(max)}	115	°C	80
Storage temperature range	T _{stg}	-55 to +150	٥	-

¹ The power supply of the device must start its ramp from 0.0 V.

² Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device. Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC862/857T/857DSL is unpowered, voltage greater

than 2.5 V must not be applied to its inputs).
³ Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as

junction temperature, T_j.

⁴ JTAG is tested only at ambient, not at standard maximum or extended maximum.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).



Thermal Characteristics

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC862/857T/857DSL.

Rating	Enviro	Symbol	Value	Unit	
Junction to ambient ¹	Natural Convection	onvection Single layer board (1s)		37	°C/W
	Four layer board (2s2p)		$R_{\theta JMA}^{3}$	23	
	Air flow (200 ft/min)) ft/min) Single layer board (1s)		30	
		Four layer board (2s2p)	$R_{\theta JMA}^{3}$	19	
Junction to board ⁴			$R_{\theta JB}$	13	
Junction to case ⁵			$R_{ extsf{ heta}JC}$	6	
Junction to package top ⁶	Natural Convection		Ψ_{JT}	2	
	Air flow (200 ft/min)		Ψ_{JT}	2	

Table 3. MPC862/857T/857DSL Thermal Resistance Data

¹ Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

- ² Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
- ³ Per JEDEC JESD51-6 with the board horizontal.

⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

- ⁵ Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
- ⁶ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5 **Power Dissipation**

Table 4 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice bus speed.

Die Revision	Frequency	Typical ¹	Maximum ²	Unit
0 50 MHz		656	735	mW
(TT Mode)	66 MHz	TBD	TBD	mW
A.1, B.0	50 MHz	630	760	mW
(1:1 Mode)	66 MHz	890	1000	mW

Table 4. Power Dissipation (P_D)

Thermal Calculation and Measurement

Characteristic	Symbol	Min	Мах	Unit
Output Low Voltage IOL = 2.0 mA (CLKOUT) IOL = 3.2 mA ³ IOL = 5.3 mA ⁴ IOL = 7.0 mA (TXD1/PA14, TXD2/PA12) IOL = 8.9 mA (TS, TA, TEA, BI, BB, HRESET, SRESET)	VOL	_	0.5	V

Table 5. DC Electrical Specifications (continued)

¹ $V_{IL}(max)$ for the I²C interface is 0.8 V rather than the 1.5 V as specified in the I²C standard.

² Input capacitance is periodically sampled.

 ³ A(0:31), TSIZ0/REG, TSIZ1, D(0:31), DP(0:3)/IRQ(3:6), RD/WR, BURST, RSV/IRQ2, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1 /PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/TOUT1/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, TOUT2/CLK4/PA4, TIN3/BRGO3/CLK5/PA3, BRGCLK2/L1RCLKB/TOUT3/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, L1TCLKB/TOUT4/CLK8/PA0, REJCT1/SPISEL/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB29, BRGO4/SPIMISO/PB28, SMSYN2/SDACK2/PB22, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/RTS1/PB19, L1ST2/RTS2/PB18, L1ST3/L1RQB/PB17, L1ST4/L1RQA/PB16, BRGO3/PB15, RSTRT1/PB14, L1ST1/RTS1/DREQ0/PC15, L1ST2/RTS2/DREQ1/PC14, L1ST3/L1RQB/PC13, L1ST4/L1RQA/PC12, CTS1/PC11, TGATE1/CD1/PC10, CTS2/PC9, TGATE2/CD2/PC8, CTS3/SDACK2/L1SYNCB/PC7, CD3/L1RSYNCB/PC6, CTS4/SDACK1/L1TSYNCA/PC5, CD4/L1RSYNCA/PC4, PD15/L1TSYNCA, PD14/L1RSYNCA, PD13/L1TSYNCB, PD12/L1RSYNCB, PD11/RXD3, PD10/TXD3, PD9/RXD4, PD8/TXD4, PD5/REJECT2, PD6/RTS4, PD7/RTS3, PD4/REJECT3, PD3, MII_MDC, MII_TX_ER, MII_EN, MII_MDIO, MII_TXD[0:3].

⁴ BDIP/GPL_B(5), BR, BG, FRZ/IRQ6, CS(0:5), CS(6)/CE(1)_B, CS(7)/CE(2)_B, WE0/BS_B0/IORD, WE1/BS_B1/IOWR, WE2/BS_B2/PCOE, WE3/BS_B3/PCWE, BS_A(0:3), GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A(2:3)/GPL_B(2:3)/CS(2:3), UPWAITA/GPL_A4, UPWAITB/GPL_B4, GPL_A5, ALE_A, CE1_A, CE2_A, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/STS, OP3/MODCK2/DSDO, BADDR(28:30).

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (VDD \times IDD) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

 $T_J = T_A + (R_{\theta JA} \times P_D)$

where:

 T_A = ambient temperature (°C)

 $R_{\theta IA}$ = package junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity T_J - T_A) are possible.



Thermal Calculation and Measurement

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_{J} = T_{B} + (R_{\theta JB} \times P_{D})$$

where:

 $R_{\theta JB}$ = junction-to-board thermal resistance (°C/W)

 T_{B} = board temperature (°C)

 P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

 Ψ_{IT} = thermal characterization parameter

 T_T = thermocouple temperature on top of package

 P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.



Num	Num		33 MHz		40 MHz		50 MHz		66 MHz	
NUM	Characteristic	Min	Max	Min	Max	Min	Мах	Min	Max	Unit
B8a	CLKOUT to TSIZ(0:1), REG, RSV, AT(0:3) BDIP, PTR valid (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B8b	CLKOUT to \overline{BR} , \overline{BG} , VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS Valid ⁴ (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3), TSIZ(0:1), REG, RSV, AT(0:3), PTR High-Z (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B11	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ assertion (MAX = 0.25 x B1 + 6.0)	7.60	13.60	6.30	12.30	5.00	11.00	3.80	11.30	ns
B11a	CLKOUT to \overline{TA} , \overline{BI} assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.30 ⁵)	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.80	ns
B12	CLKOUT to \overline{TS} , \overline{BB} negation (MAX = 0.25 x B1 + 4.8)	7.60	12.30	6.30	11.00	5.00	9.80	3.80	8.50	ns
B12a	CLKOUT to \overline{TA} , \overline{BI} negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B13	CLKOUT to $\overline{\text{TS}}$, $\overline{\text{BB}}$ High-Z (MIN = 0.25 x B1)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns
B13a	CLKOUT to \overline{TA} , \overline{BI} High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 x B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to TEA assertion (MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B15	CLKOUT to $\overline{\text{TEA}}$ High-Z (MIN = 0.00 x B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	\overline{TA} , \overline{BI} valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B16a	TEA, KR, RETRY, CR valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 4.5)	4.50	_	4.50	_	4.50	_	4.50	_	ns
B16b	$\overline{\text{BB}}$, $\overline{\text{BG}}$, $\overline{\text{BR}}$, valid to CLKOUT (setup time) ⁶ (4MIN = 0.00 x B1 + 0.00)	4.00	-	4.00	-	4.00	—	4.00	—	ns
B17	CLKOUT to \overline{TA} , \overline{TEA} , \overline{BI} , \overline{BB} , \overline{BG} , \overline{BR} valid (hold time) (MIN = 0.00 x B1 + 1.00 ⁷)	1.00	_	1.00	_	1.00	_	2.00	_	ns

Table 7. Bus Operation Timings (continued)



Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		11
NUM	Characteristic	Min	Max	Min	Max	Min	Мах	Min	Max	Unit
B27	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 x B1 - 2.00)	35.90		29.30		23.00		16.90		ns
B27a	A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	_	20.70	_	ns
B28	CLKOUT rising edge to $\overline{WE}(0:3)$ negated GPCM write access CSNT = 0 (MAX = 0.00 x B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, 1, CSNT = 1, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0,1, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	_	14.30	_	13.00	_	11.80	_	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0,1, CSNT = 1, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B28d	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0,1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	_	18.00	_	18.00	_	14.30	_	12.30	ns
B29	WE(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	_	1.80	—	ns
B29a	WE(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	_	10.50	_	8.00	_	5.60	_	ns
B29b	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3), High Z GPCM write access, ACS = 00, TRLX = 0,1 & CSNT = 0 (MIN = 0.25 x B1 - 2.00)	5.60	_	4.30	_	3.00	—	1.80	_	ns
B29c	$\overline{\text{CS}}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	_	10.50	_	8.00	_	5.60	_	ns

Table 7. Bus Operation	i Timings	(continued)
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Bus Signal Timing

Figure 15 through Figure 17 provide the timing for the external bus write controlled by various GPCM factors.



Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0,1 CSNT = 0)



Bus Signal Timing

Figure 26 provides the PCMCIA access cycle timing for the external bus read.



Figure 26. PCMCIA Access Cycles Timing External Bus Read







Figure 33. Reset Timing—Configuration from Data Bus

Figure 34 provides the reset timing for the data bus weak drive during configuration.



Figure 34. Reset Timing—Data Bus Weak Drive during Configuration



IEEE 1149.1 Electrical Specifications

Figure 35 provides the reset timing for the debug port configuration.



Figure 35. Reset Timing—Debug Port Configuration

10 IEEE 1149.1 Electrical Specifications

Table 13 provides the JTAG timings for the MPC862/857T/857DSL shown in Figure 36 though Figure 39.

Num	Characteristic	All Freq	Unit	
Num	Gharacteristic	Min	Мах	Onit
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	TRST assert time	100.00	—	ns
J91	TRST setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid		50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance		50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	_	ns
J96	TCK rising edge to boundary scan input invalid	50.00	_	ns

Table 13. JTAG Timing



CPM Electrical Characteristics



Figure 49. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA



CPM Electrical Characteristics





CPM Electrical Characteristics







11.9 SMC Transparent AC Electrical Specifications

Table 23 provides the SMC transparent timings as shown in Figure 65.

Num	Characteristic	All Freq	Unit	
Nulli	Characteristic	Min	Мах	Onit
150	SMCLK clock period ¹	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	_	ns

¹ SyncCLK must be at least twice as fast as SMCLK.



Figure 65. SMC Transparent Timing Diagram



CPM Electrical Characteristics

11.10 SPI Master AC Electrical Specifications

Table 24 provides the SPI master timings as shown in Figure 66 though Figure 67.

Table 24. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Мах	onit
160	MASTER cycle time	4	1024	t _{cyc}
161	MASTER clock (SCK) high or low time	2	512	t _{cyc}
162	MASTER data setup time (inputs)	15	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	10	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns



Figure 66. SPI Master (CP = 0) Timing Diagram

Num	Characteristic	Min	Мах	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	_	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	_	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	_	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	_	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period



Figure 76 shows the MII serial management channel timing diagram.



Figure 76. MII Serial Management Channel Timing Diagram

14 Mechanical Data and Ordering Information

Table 33 provides information on the MPC862/857T/857DSL derivative devices.

Table 33. MPC862/857T/857DSL Derivatives

Device	Number of SCCs ¹	Ethernet Support	Multi-Channel HDLC Support	ATM Support	Cache Size	
Device					Instruction	Data
MPC862T	Four	10/100 Mbps	Yes	Yes	4 Kbytes	4 Kbytes
MPC862P	Four	10/100 Mbps	Yes	Yes	16 Kbytes	8 Kbytes



Name	Pin Number	Туре
GPL_A5	D3	Output
PORESET	R2	Input
RSTCONF	Р3	Input
HRESET	N4	Open-drain
SRESET	P2	Open-drain
XTAL	P1	Analog Output
EXTAL	N1	Analog Input (3.3 V only)
XFC	Т2	Analog Input
CLKOUT	W3	Output
EXTCLK	N2	Input (3.3 V only)
TEXP	N3	Output
ALE_A MII-TXD1	К2	Output
CE1_A MII-TXD2	B3	Output
CE2_A MII-TXD3	A3	Output
WAIT_A SOC_Split ²	R3	Input
WAIT_B	R4	Input
IP_A0 UTPB_Split0 ² MII-RXD3	Т5	Input
IP_A1 UTPB_Split1 ² MII-RXD2	Т4	Input
IP_A2 IOIS16_A UTPB_Split2 ² MII-RXD1	U3	Input
IP_A3 UTPB_Split3 ² MII-RXD0	W2	Input
IP_A4 UTPB_Split4 ² MII-RXCLK	U4	Input
IP_A5 UTPB_Split5 ² MII-RXERR	U5	Input

Table 35. Pin Assignments (continued)



Name	Pin Number	Туре
IP_A6 UTPB_Split6 ² MII-TXERR	Т6	Input
IP_A7 UTPB_Split7 ² MII-RXDV	ТЗ	Input
ALE_B DSCK/AT1	J1	Bidirectional Three-state
IP_B[0:1] IWP[0:1] VFLS[0:1]	H2, J3	Bidirectional
IP_B2 IOIS16_B AT2	J2	Bidirectional Three-state
IP_B3 IWP2 VF2	G1	Bidirectional
IP_B4 LWP0 VF0	G2	Bidirectional
IP_B5 LWP1 VF1	J4	Bidirectional
IP_B6 DSDI AT0	кз	Bidirectional Three-state
IP_B7 PTR AT3	H1	Bidirectional Three-state
OP0 MII-TXD0 UtpClk_Split ²	L4	Bidirectional
OP1	L2	Output
OP2 MODCK1 STS	L1	Bidirectional
OP3 MODCK2 DSDO	M4	Bidirectional
BADDR30 REG	К4	Output
BADDR[28:29]	M3, M2	Output
ĀS	L3	Input

Table 35. Pin Assignments (continued)



Document Revision History

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