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What is "Embedded - Microcontrollers"?

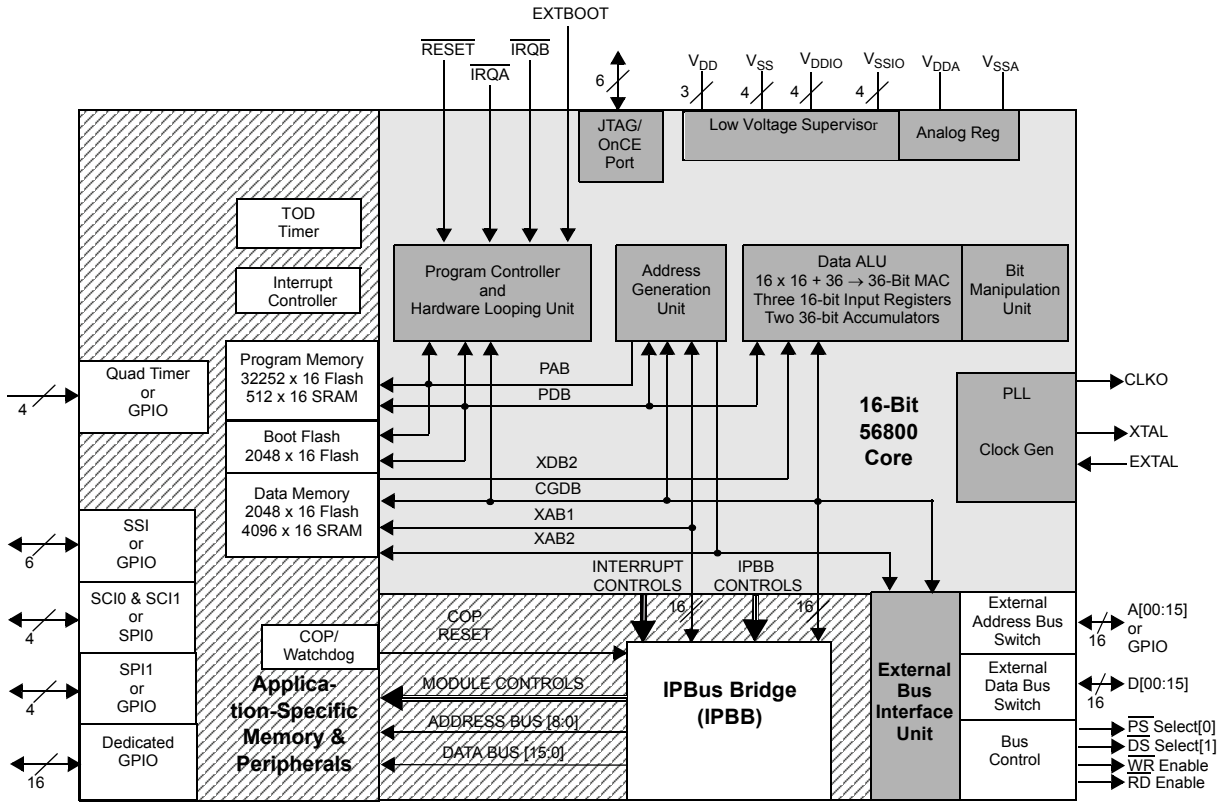
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800
Core Size	16-Bit
Speed	80MHz
Connectivity	EBI/EMI, SCI, SPI, SSI
Peripherals	POR, WDT
Number of I/O	46
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 2.75V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56f826bu80

56F826 General Description

- Up to 40 MIPS at 80MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- Hardware DO and REP loops
- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- 31.5K × 16-bit words (64KB) Program Flash
- 512 × 16-bit words (1KB) Program RAM
- 2K × 16-bit words (4KB) Data Flash
- 4K × 16-bit words (8KB) Data RAM
- 2K × 16-bit words (4KB) BootFLASH
- Up to 64K × 16-bit words each of external memory expansion for Program and Data memory
- One Serial Port Interface (SPI)
- One additional SPI or two optional Serial Communication Interfaces (SCI)
- One Synchronous Serial Interface (SSI)
- One General Purpose Quad Timer
- JTAG/OnCE™ for debugging
- 100-pin LQFP Package
- 16 dedicated and 30 shared GPIO
- Time-of-Day (TOD) Timer



56F826 Block Diagram

Part 1 Overview

1.1 56F826 Features

1.1.1 Processing Core

- Efficient 16-bit 56800 family controller engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators, including extension bits
- 16-bit bidirectional barrel shifter
- Parallel instruction set with unique processor addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C Compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE Debug Programming Interface

1.1.2 Memory

- Harvard architecture permits as many as three simultaneous accesses to Program and Data memory
- On-chip memory including a low-cost, high-volume Flash solution
  - 31.5K × 16-bit words of Program Flash
  - 512 × 16-bit words of Program RAM
  - 2K × 16-bit words of Data Flash
  - 4K × 16-bit words of Data RAM
  - 2K × 16-bit words of BootFLASH
- Off-chip memory expansion capabilities programmable for 0, 4, 8, or 12 wait states
  - As much as 64K × 16-bit Data memory
  - As much as 64K × 16-bit Program memory

1.1.3 Peripheral Circuits for 56F826

- One General Purpose Quad Timer totalling 7 pins
- One Serial Peripheral Interface with 4 pins (or four additional GPIO lines)
- One Serial Peripheral Interface, or multiplexed with two Serial Communications Interfaces totalling 4 pins
- Synchronous Serial Interface (SSI) with configurable six-pin port (or six additional GPIO lines)

This controller also provides a full set of standard programmable peripherals including one Synchronous Serial Interface (SSI), one Serial Peripheral Interface (SPI), the option to select a second SPI or two Serial Communications Interfaces (SCIs), and one Quad Timer. The SSI, SPI, and Quad Timer can be used as General Purpose Input/Outputs (GPIOs) if a timer function is not required.

1.3 Award-Winning Development Environment

- Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The Code Warrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, Code Warrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Product Documentation

The four documents listed in **Table 1-1** are required for a complete description and proper design with the 56F826. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at **www.freescale.com**.

Table 1-1 56F826 Chip Documentation

Topic	Description	Order Number
56800E Family Manual	Detailed description of the 56800 family architecture, and 16-bit core processor and the instruction set	56800EFM
DSP56F826/F827 User's Manual	Detailed description of memory, peripherals, and interfaces of the 56F826 and 56F827	DSP56F826-827UM
56F826 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56F826
56F826 Product Brief	Summary description and block diagram of the 56F826 core, memory, peripherals and interfaces	DSP56F826PB
56F826 Errata	Details any chip issues that might be present	DSP56F826E

Part 2 Signal/Connection Descriptions

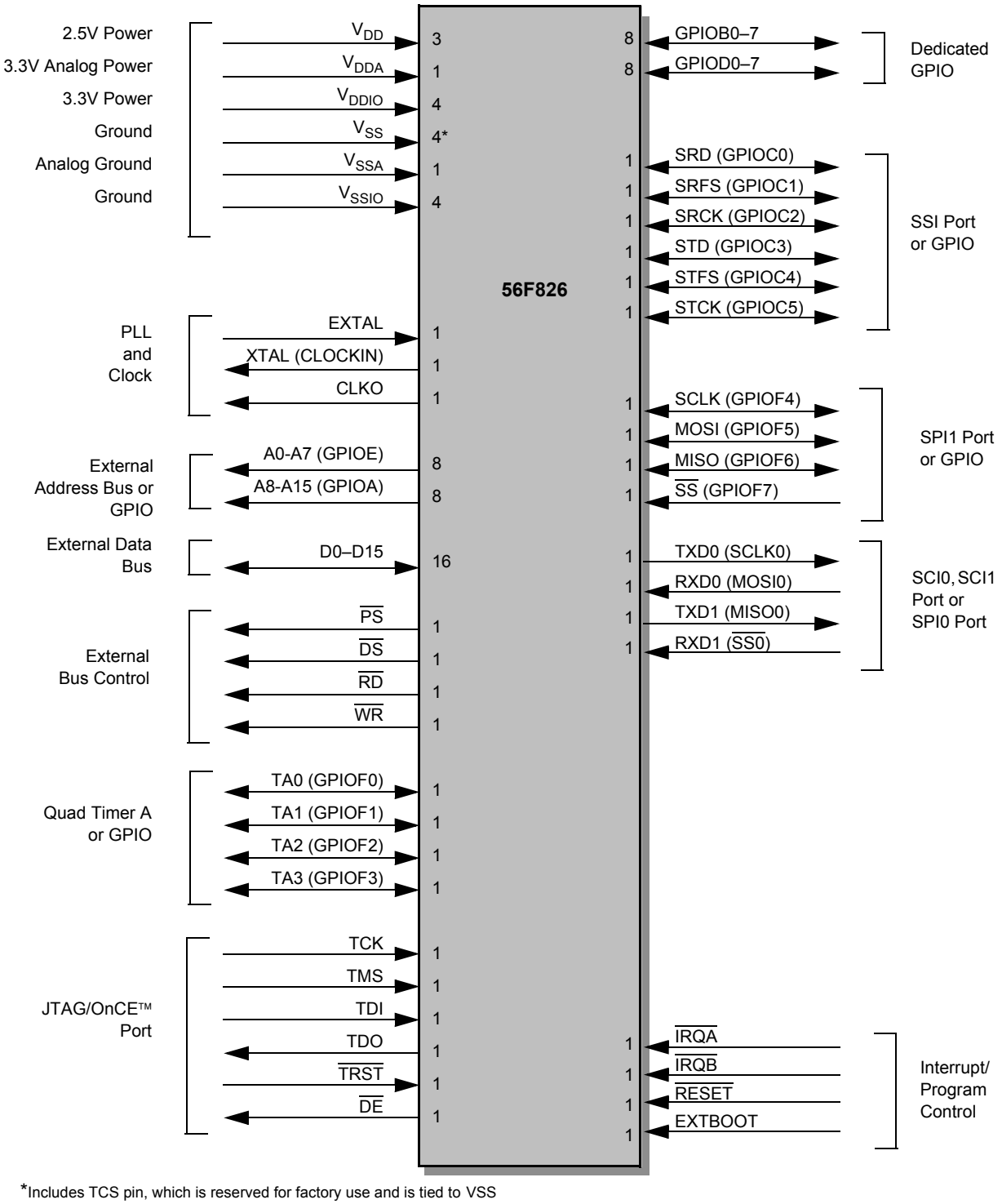
2.1 Introduction

The input and output signals of the 56F826 are organized into functional groups, as shown in **Table 2-1** and as illustrated in **Figure 2-1**. **Table 2-1** describes the signal or signals present on a pin.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins
Power (V_{DD}, V_{DDIO} or V_{DDA})	(3,4,1)
Ground (V_{SS}, V_{SSIO} or V_{SSA})	(3,4,1)
PLL and Clock	3
Address Bus[1]	16
Data Bus[1]	16
Bus Control	4
Quad Timer Module Ports[1]	4
JTAG/On-Chip Emulation (OnCE)	6
Dedicated General Purpose Input/Output	16
Synchronous Serial Interface (SSI) Port[1]	6
Serial Peripheral Interface (SPI) Port[1]	4
Serial Communications Interface (SCI) Ports	4
Interrupt and Program Control	5

1. Alternately, GPIO pins



*Includes TCS pin, which is reserved for factory use and is tied to VSS

Figure 2-1 56F826 Signals Identified by Functional Group[1]

1. Alternate pin functionality is shown in parentheses.

2.2 Signals and Package Information

All inputs have a weak internal pull-up circuit associated with them. These pull-up circuits are always enabled. Exceptions:

1. When a pin is owned by GPIO, then the pull-up may be disabled under software control.
2. TCK has a weak pull-down circuit always active.

Table 2-1 56F826 Signal and Package Information for the 100 Pin LQFP

Signal Name	Pin No.	Type	Description
V_{DD}	20	V_{DD}	**Power**—These pins provide power to the internal structures of the chip, and are generally connected to a 2.5V supply.
V_{DD}	64	V_{DD}	
V_{DD}	94	V_{DD}	
V_{DDA}	59	V_{DDA}	**Analog Power**—This pin is a dedicated power pin for the analog portion of the chip and should be connected to a low-noise 3.3V supply.
V_{DDIO}	5	V_{DDIO}	**Power In/Out**—These pins provide power to the I/O structures of the chip, and are generally connected to a 3.3V supply.
V_{DDIO}	30	V_{DDIO}	
V_{DDIO}	57	V_{DDIO}	
V_{DDIO}	80	V_{DDIO}	
V_{SS}	19	V_{SS}	**GND—**These pins provide grounding for the internal structures of the chip. All should be attached to V_{SS}.
V_{SS}	63	V_{SS}	
V_{SS}	95	V_{SS}	
V_{SSA}	60	V_{SSA}	**Analog Ground**—This pin supplies an analog ground.
V_{SSIO}	6	V_{SSIO}	**GND In/Out**—These pins provide grounding for the I/O ring on the chip. All should be attached to V_{SS}.
V_{SSIO}	31	V_{SSIO}	
V_{SSIO}	58	V_{SSIO}	
V_{SSIO}	81	V_{SSIO}	
TCS	99	Input/Output (Schmitt)	**TCS**—This pin is reserved for factory use. It must be tied to V_{SS} for normal use. In block diagrams, this pin is considered an additional V_{SS}.
EXTAL	61	Input	**External Crystal Oscillator Input**—This input should be connected to a 4MHz external crystal or ceramic resonator. For more information, please refer to Section 3.6.

Table 2-1 56F826 Signal and Package Information for the 100 Pin LQFP (Continued)

Signal Name	Pin No.	Type	Description
XTAL (CLOCKIN)	62	Output Input	**Crystal Oscillator Output**—This output connects the internal crystal oscillator output to an external crystal or ceramic resonator. If an external clock source over 4MHz is used, XTAL must be used as the input and EXTAL connected to V_{SS}. For more information, please refer to **Section 3.6.3**. **External Clock Input**—This input should be asserted when using an external clock or ceramic resonator.
CLKO	65	Output	**Clock Output**—This pin outputs a buffered clock signal. By programming the CLKO Select Register (CLKOSR), the user can select between outputting a version of the signal applied to XTAL and a version of the device master clock at the output of the PLL. The clock frequency on this pin can be disabled by programming the CLKO Select Register (CLKOSR).
A0 (GPIOE0)	24	Output	**Address Bus**—A0–A7 specify the address for external program or data memory accesses. **Port E GPIO**—These eight General Purpose I/O (GPIO) pins can be individually programmed as input or output pins. After reset, the default state is Address Bus.
A1 (GPIOE1)	23	Input/Output	
A2 (GPIOE2)	22		
A3 (GPIOE3)	21		
A4 (GPIOE4)	18		
A5 (GPIOE5)	17		
A6 (GPIOE6)	16		
A7 (GPIOE7)	15		

Table 3-1 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage, core	V_{DD}[1]	V_{SS} – 0.3	V_{SS} + 3.0	V
Supply voltage, IO Supply voltage, Analog	V_{DDIO}[2] V_{DDA}[2]	V_{SSIO} – 0.3 V_{SSA} – 0.3	V_{SSIO} + 4.0 V_{SSA} + 4.0	V
Digital input voltages Analog input voltages - XTAL, EXTAL	V_{IN} V_{INA}	V_{SSIO} – 0.3 V_{SSA} – 0.3	V_{SSIO} + 5.5 V_{DDA} + 0.3	V
Voltage difference V_{DD} to V_{DD_IO}, V_{DDA}	ΔV_{DD}	- 0.3	0.3	V
Voltage difference V_{SS} to V_{SS_IO}, V_{SSA}	ΔV_{SS}	- 0.3	0.3	V
Current drain per pin excluding V_{DD}, V_{SS}, V_{DDA}, V_{SSA}, V_{DDIO}, V_{SSIO}	I	—	10	mA
Junction temperature	T_J	—	150	°C
Storage temperature range	T_{STG}	–55	150	°C

1. V_{DD} must not exceed V_{DDIO}
2. V_{DDIO} and V_{DDA} must not differ by more that 0.5V

Table 3-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage, core	V_{DD}	2.25	2.5	2.75	V
Supply Voltage, IO and analog	V_{DDIO},V_{DDA}	3.0	3.3	3.6	V
Voltage difference V_{DD} to V_{DD_IO}, V_{DDA}	ΔV_{DD}	-0.1	-	0.1	V
Voltage difference V_{SS} to V_{SS_IO}, V_{SSA}	ΔV_{SS}	-0.1	-	0.1	V
Ambient operating temperature	T_A	–40	–	85	°C

Table 3-3 Thermal Characteristics[6]

Characteristic	Comments	Symbol	Value	Unit	Notes
			100-pin LQFP		
Junction to ambient Natural convection		$R_{\theta JA}$	48.3	°C/W	2
Junction to ambient (@1m/sec)		$R_{\theta JMA}$	43.9	°C/W	2
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$ (2s2p)	40.7	°C/W	1.2
Junction to ambient (@1m/sec)	Four layer board (2s2p)	$R_{\theta JMA}$	38.6	°C/W	1,2
Junction to case		$R_{\theta JC}$	13.5	°C/W	3
Junction to center of case		Ψ_{JT}	1.0	°C/W	4, 5
I/O pin power dissipation		$P_{I/O}$	User Determined	W	
Power dissipation		P_D	$P_D = (I_{DD} \times V_{DD} + P_{I/O})$	W	
Junction to center of case		P_{DMAX}	(TJ - TA) /RθJA	W	7

Notes:

1. Theta-JA determined on 2s2p test boards is frequently lower than would be observed in an application. Determined on 2s2p thermal test board.
2. Junction to ambient thermal resistance, Theta-JA ($R_{\theta JA}$) was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection. Theta-JA was also simulated on a thermal test board with two internal planes (2s2p, where “s” is the number of signal layers and “p” is the number of planes) per JESD51-6 and JESD51-7. The correct name for Theta-JA for forced convection or with the non-single layer boards is Theta-JMA.
3. Junction to case thermal resistance, Theta-JC ($R_{\theta JC}$), was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the “case” temperature. The basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.
4. Thermal Characterization Parameter, Psi-JT (Ψ_{JT}), is the “resistance” from junction to reference point thermocouple on top center of case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in steady state customer environments.
5. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
6. See Section 5.1 for more details on thermal design considerations.
7. TJ = Junction Temperature
   TA = Ambient Temperature

V_{DD} should not be allowed to rise early (1). This is usually avoided by running the regulator for the V_{DD} supply (2.5V) from the voltage generated by the 3.3V V_{DDIO} supply, see **Figure 3-3**. This keeps V_{DD} from rising faster than V_{DDIO}.

V_{DD} should not rise so late that a large voltage difference is allowed between the two supplies (2). Typically this situation is avoided by using external discrete diodes in series between supplies, as shown in **Figure 3-3**. The series diodes forward bias when the difference between V_{DDIO} and V_{DD} reaches approximately 1.4, causing V_{DD} to rise as V_{DDIO} ramps up. When the V_{DD} regulator begins proper operation, the difference between supplies will typically be 0.8V and conduction through the diode chain reduces to essentially leakage current. During supply sequencing, the following general relationship should be adhered to:
$V_{DDIO} \geq V_{DD} \geq (V_{DDIO} - 1.4V)$

In practice, V_{DDA} is typically connected directly to V_{DDIO} with some filtering.

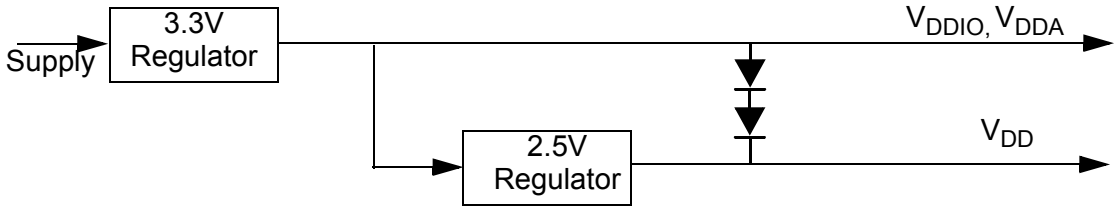
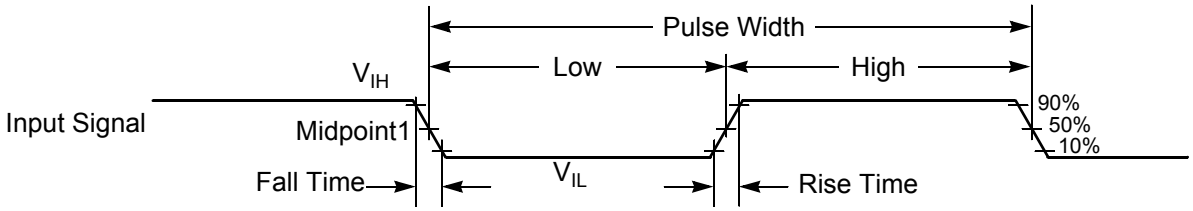


Figure 3-3 Example Circuit to Control Supply Sequencing

3.4 AC Electrical Characteristics

Timing waveforms in **Section 3.4** are tested using the V_{IL} and V_{IH} levels specified in the DC Characteristics table. The levels of V_{IH} and V_{IL} for an input signal are shown in **Figure 3-4**.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 3-4 Input Signal Measurement References

Figure 3-5 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

3.6.3 External Clock Source

The recommended method of connecting an external clock is given in **Figure 3-11**. The external clock source is connected to XTAL and the EXTAL pin is held $V_{DDA}/2$.

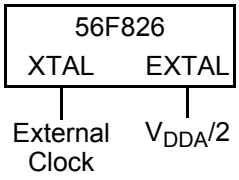


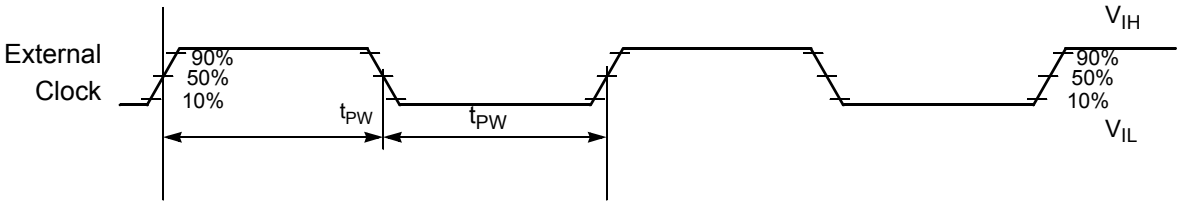
Figure 3-11 Connecting an External Clock Signal

Table 3-8 External Clock Operation Timing Requirements

Operating Conditions: V_{SSIO}=V_{SS} = V_{SSA} = 0V, V_{DDA} =V_{DDIO}=3.0–3.6V, V_{DD} = 2.25–2.75V, T_A = –40° to +85°C, $C_L \le$ 50pF, f_{op} = 80MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	0	4	80[2]	MHz
Clock Pulse Width[3, 4]	t_{PW}	6.25	—	—	ns

1. See **Figure 3-11** for details on using the recommended connection of an external clock driver.
2. When using Time of Day (TOD), maximum external frequency is 6MHz.
3. The high or low pulse width must be no smaller than 6.25ns or the chip will not function.
4. Parameters listed are guaranteed by design.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 3-12 External Clock Timing

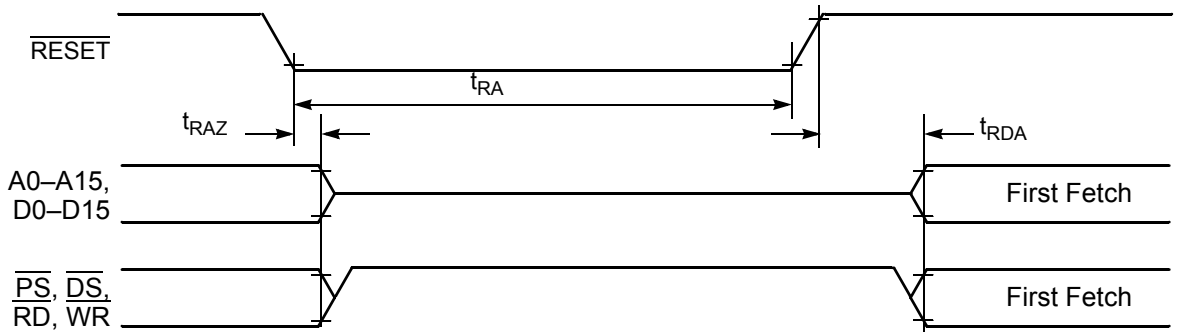


Figure 3-14 Asynchronous Reset Timing

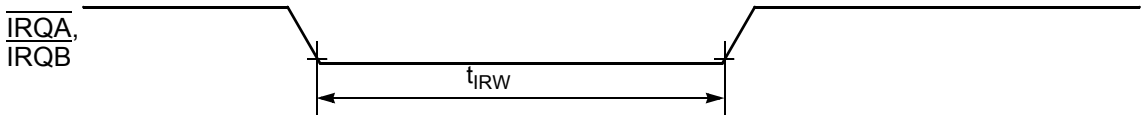
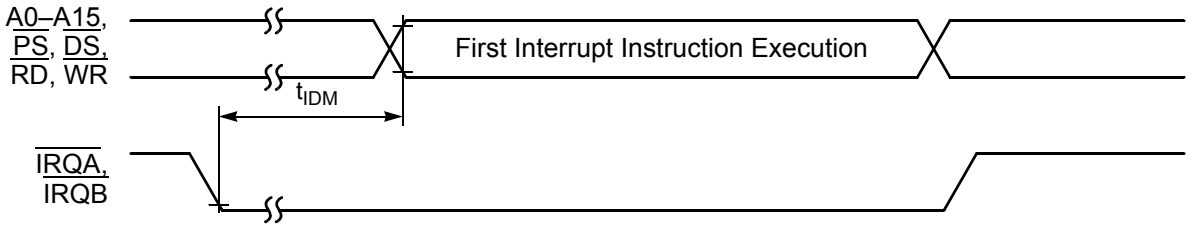
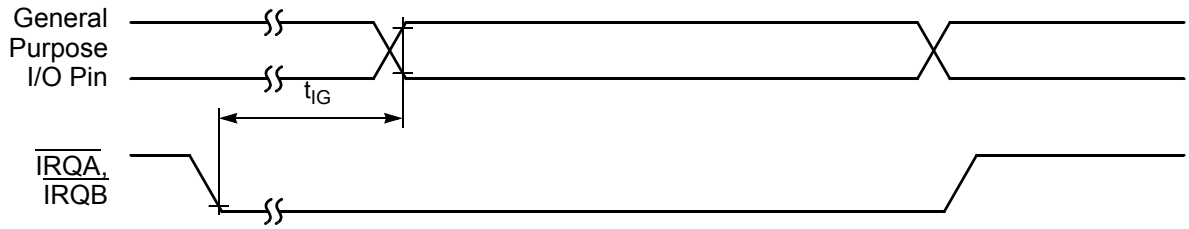


Figure 3-15 External Interrupt Timing (Negative-Edge-Sensitive)



a) First Interrupt Instruction Execution



b) General Purpose I/O

Figure 3-16 External Level-Sensitive Interrupt Timing

3.9 Serial Peripheral Interface (SPI) Timing

Table 3-12 SPI Timing[1]

Operating Conditions: V_{SSIO}=V_{SS} = V_{SSA} = 0V, V_{DDA} =V_{DDIO}=3.0–3.6V, V_{DD} = 2.25–2.75V, T_A = –40° to +85°C, C_L ≤ 50pF, f_{op} = 80MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 25	 — —	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	Figure 3-23
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	Figure 3-23
Clock (SCLK) high time Master Slave	t_{CH}	 24 12	 — —	ns ns	Figures 3-20, 3-21, 3-22, 3-23
Clock (SCLK) low time Master Slave	t_{CL}	 24.1 12	 — —	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Access time (time to data active from high-impedance state) Slave	t_A	 4.8	 15	 ns	Figure 3-23
Disable time (hold time to high-impedance state) Slave	t_D	 3.7	 15.2	 ns	Figure 3-23
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figures 3-20, 3-21, 3-22, 3-23

1. Parameters are guaranteed by design.

Table 3-14 SSI Slave Mode[1] Switching Characteristics

Operating Conditions: $V_{SSIO} = V_{SS} = V_{SSA} = 0V$, $V_{DDA} = V_{DDIO} = 3.0–3.6V$, $V_{DD} = 2.25–2.75V$, $T_A = –40°$ to $+85°C$, $C_L \leq 50pF$, $f_{op} = 80MHz$

Parameter	Symbol	Min	Typ	Max	Units
Synchronous Operation (in addition to standard external clock parameters)					
SRXD Setup time before STCK low - Slave	t_{TSS}	4	—	—	
SRXD Hold time after STCK low - Slave	t_{THS}	4	—	—	

1. Slave mode is externally generated clocks and frame syncs
2. Max clock frequency is IP_clk/4 = 40MHz / 4 = 10MHz for an 80MHz part.
3. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFSI=0 in SCR2 and RFSI=0 in SCSR). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS in the tables and in the figures.
4. 50% duty cycle
5. bl = bit length; wl = word length

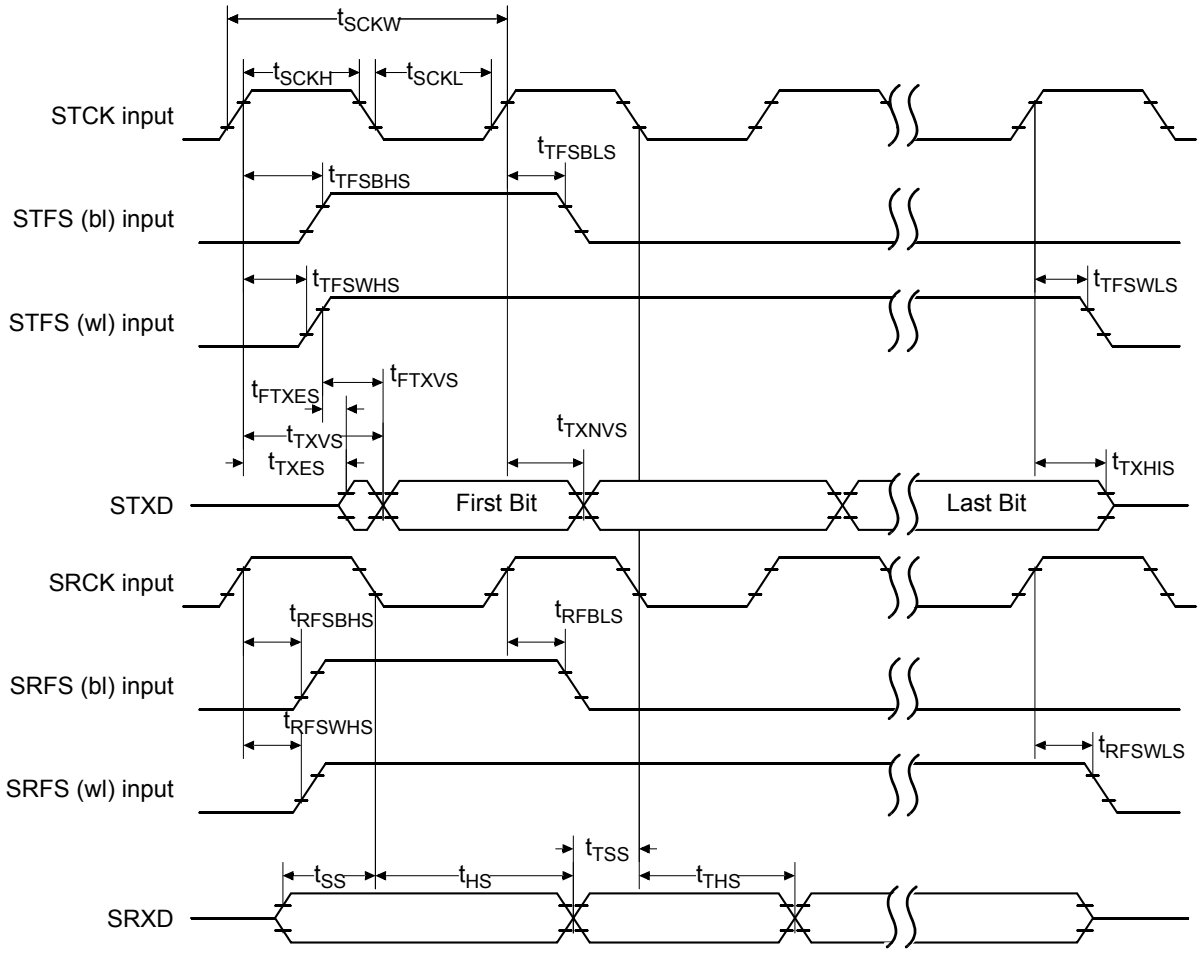


Figure 3-25 Slave Mode Clock Timing

3.11 Quad Timer Timing

Table 3-15 Timer Timing[1, 2]

Operating Conditions: $V_{SSIO} = V_{SS} = V_{SSA} = 0V$, $V_{DDA} = V_{DDIO} = 3.0–3.6V$, $V_{DD} = 2.25–2.75V$, $T_A = –40°$ to $+85°C$, $C_L \leq 50pF$, $f_{op} = 80MHz$

Characteristic	Symbol	Min	Max	Unit
Timer input period	P_{IN}	4T+6	—	ns
Timer input high/low period	P_{INHL}	2T+3	—	ns
Timer output period	P_{OUT}	2T	—	ns
Timer output high/low period	P_{OUTHL}	1T	—	ns

1. In the formulas listed, T = clock cycle. For 80MHz operation, T = 12.5ns.
2. Parameters listed are guaranteed by design.

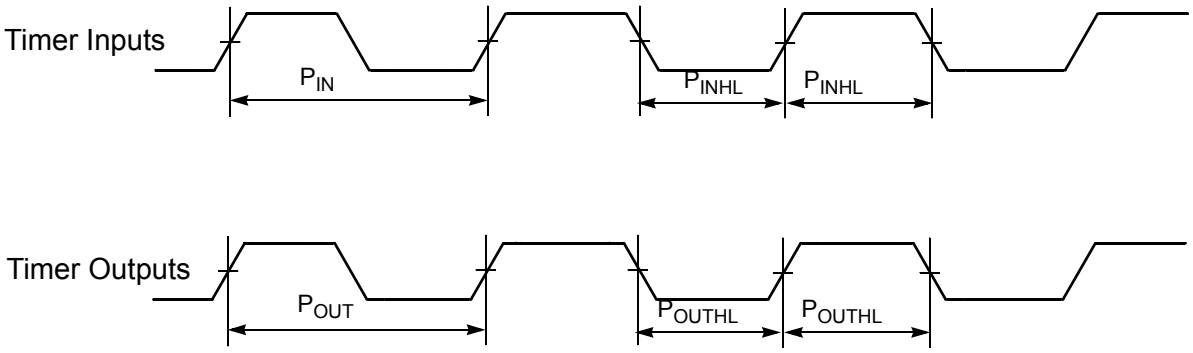


Figure 3-26 Quad Timer Timing

3.12 Serial Communication Interface (SCI) Timing

Table 3-16 SCI Timing[4]

Operating Conditions: V_{SSIO}=V_{SS} = V_{SSA} = 0V, V_{DDA} =V_{DDIO}=3.0–3.6V, V_{DD} = 2.25–2.75V, T_A = –40° to +85°C, C_L ≤ 50pF, f_{op} = 80MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate[1]	BR	—	(f_{MAX}*2.5)/(80)	Mbps
RXD[2] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns
TXD[3] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns

1. f_{MAX} is the frequency of operation of the system clock in MHz.
2. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
3. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.
4. Parameters listed are guaranteed by design.

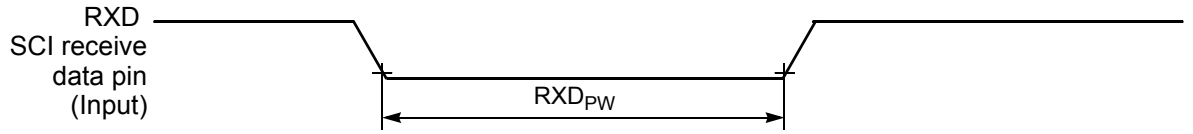


Figure 3-27 RXD Pulse Width

Table 4-1 56F826 Pin Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	TMS	26	$\overline{RD}$	51	SRD	76	GPIOD2
2	TDI	27	$\overline{WR}$	52	SRFS	77	GPIOD3
3	TDO	28	$\overline{DS}$	53	SRCK	78	GPIOD4
4	$\overline{TRST}$	29	$\overline{PS}$	54	STD	79	GPIOD5
5	V_{DDIO}	30	V_{DDIO}	55	STFS	80	V_{DDIO}
6	V_{SSIO}	31	V_{SSIO}	56	STCK	81	V_{SSIO}
7	A15	32	$\overline{IRQA}$	57	V_{DDIO}	82	GPIOD6
8	A14	33	$\overline{IRQB}$	58	V_{SSIO}	83	GPIOD7
9	A13	34	D0	59	V_{DDA}	84	SCLK
10	A12	35	D1	60	V_{SSA}	85	MOSI
11	A11	36	D2	61	EXTAL	86	MISO
12	A10	37	D3	62	XTAL	87	$\overline{SS}$
13	A9	38	D4	63	V_{SS}	88	TA3
14	A8	39	D5	64	V_{DD}	89	TA2
15	A7	40	D6	65	CLKO	90	TA1
16	A6	41	D7	66	GPIOB0	91	TA0
17	A5	42	D8	67	GPIOB1	92	RXD1
18	A4	43	D9	68	GPIOB2	93	TXD1
19	V_{SS}	44	D10	69	GPIOB3	94	V_{DD}
20	V_{DD}	45	$\overline{RESET}$	70	GPIOB4	95	V_{SS}
21	A3	46	D11	71	GPIOB5	96	RXD0
22	A2	47	D12	72	GPIOB6	97	TXD0
23	A1	48	D13	73	GPIOB7	98	$\overline{DE}$
24	A0	49	D14	74	GPIOD0	99	TCS
25	EXTBOOT	50	D15	75	GPIOD1	100	TCK

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